Mini System

CEM2100/00/98

Service

Service

Service Manual

TABLE OF CONTENTS

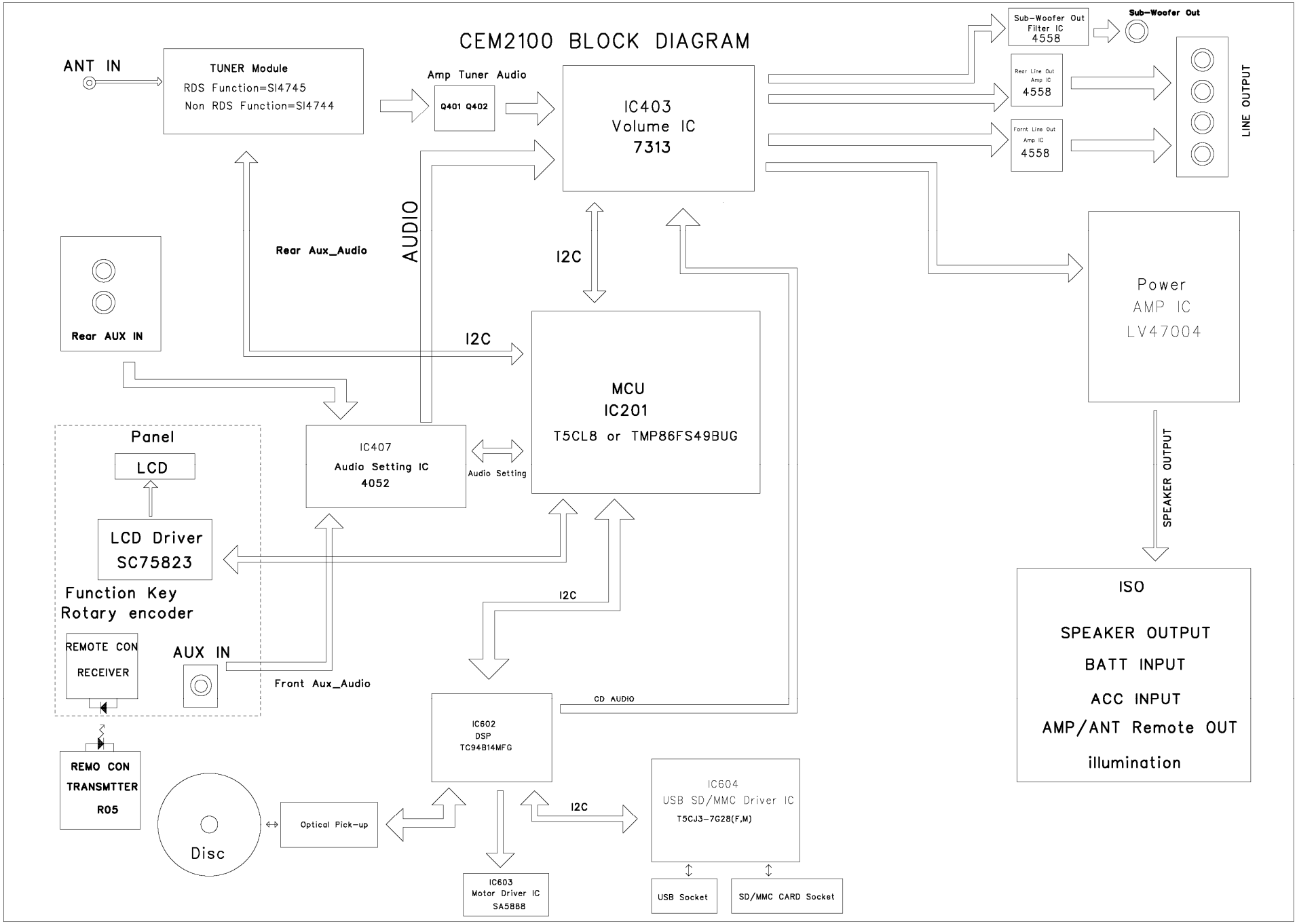
DISMANTLING INSTRUCTIONS..... 2
BLOCK DIAGRAM.....3
WIRING DIAGRAM.....4
CIRCUIT DIAGRAM MAIN BOARD.....5-7
CIRCUIT DIAGRAM PANEL BOARD.....8
CIRCUIT DIAGRAM REMOTE BOARD..... 9
CIRCUIT DIAGRAM TUNER BOARD.....10
MAIN PCB COMPONENT LAYOUT..... 11-12
PANEL PCB COMPONENT LAYOUT..... 13-14
REMOTE PCB COMPONENT LAYOUT..... 15-16
TUNER PCB COMPONENT LAYOUT.....17-18
SD PCB COMPONENT LAYOUT..... 19
CD CONNECTOR PCB COMPONENT LAYOUT.....20
ISO PCB COMPONENTLAYOUT..... 21
SET EXPLODER VIEW DRAWING..... 22

CLASS 1
LASER PRODUCT

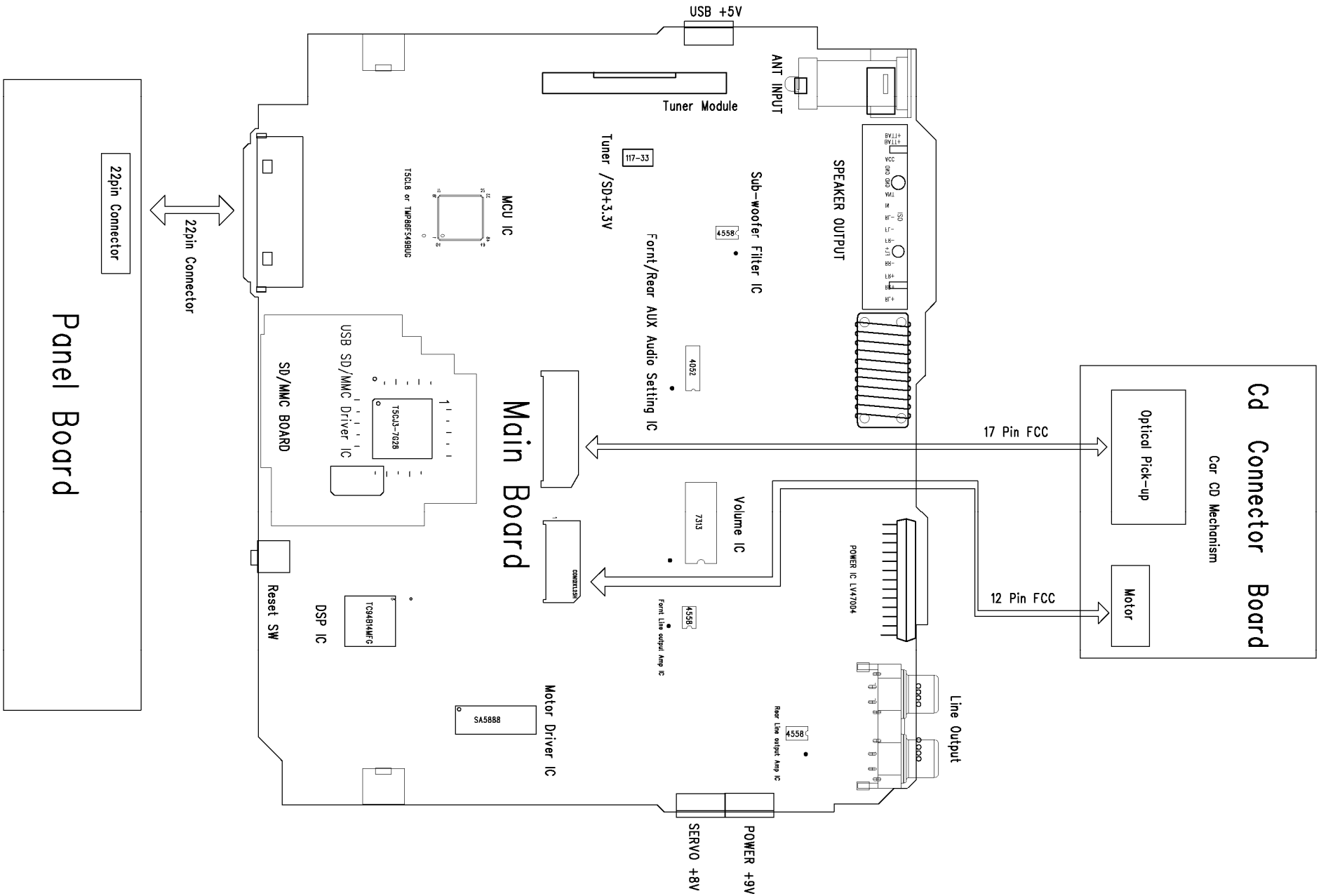
Version1.1

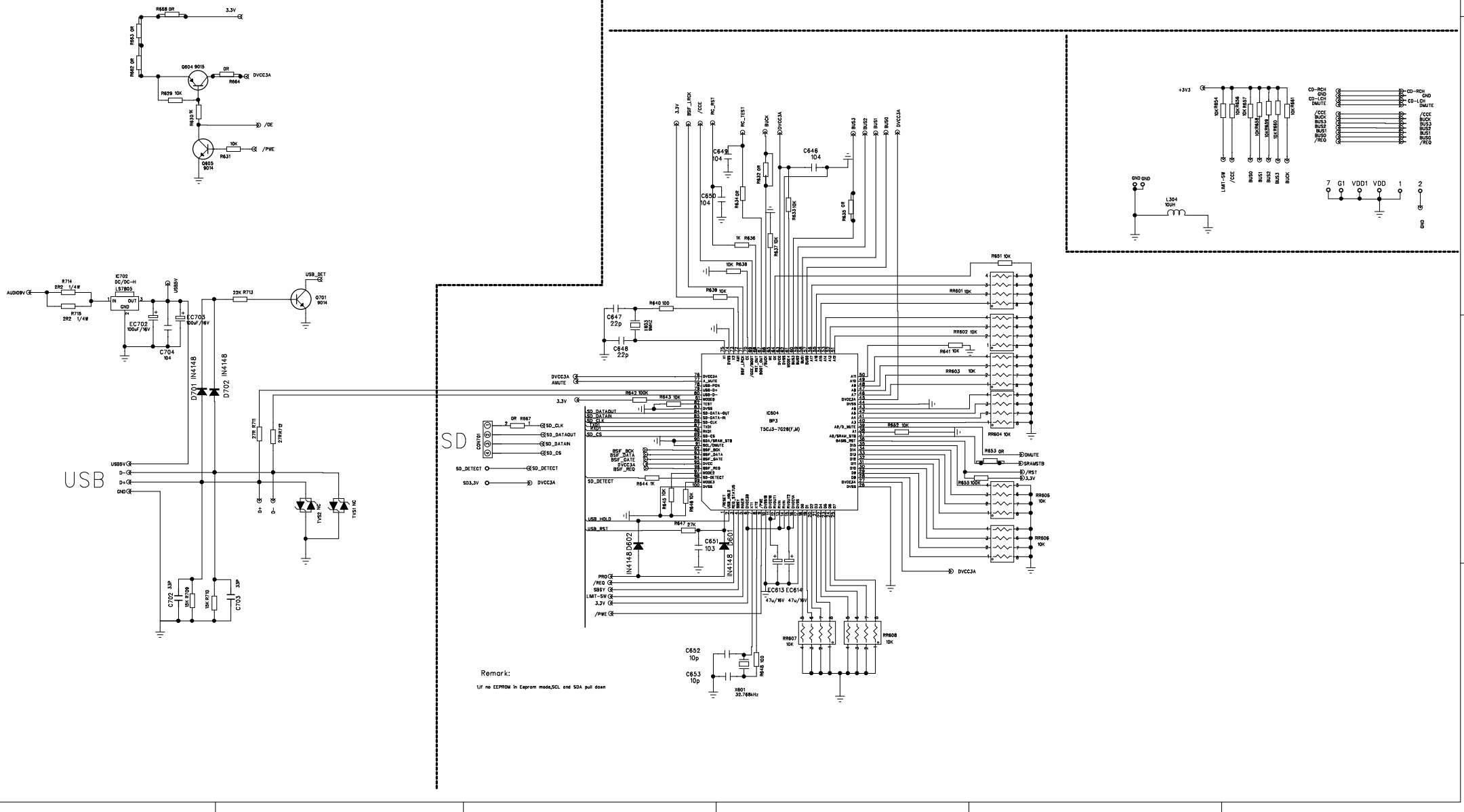
2011-6-29

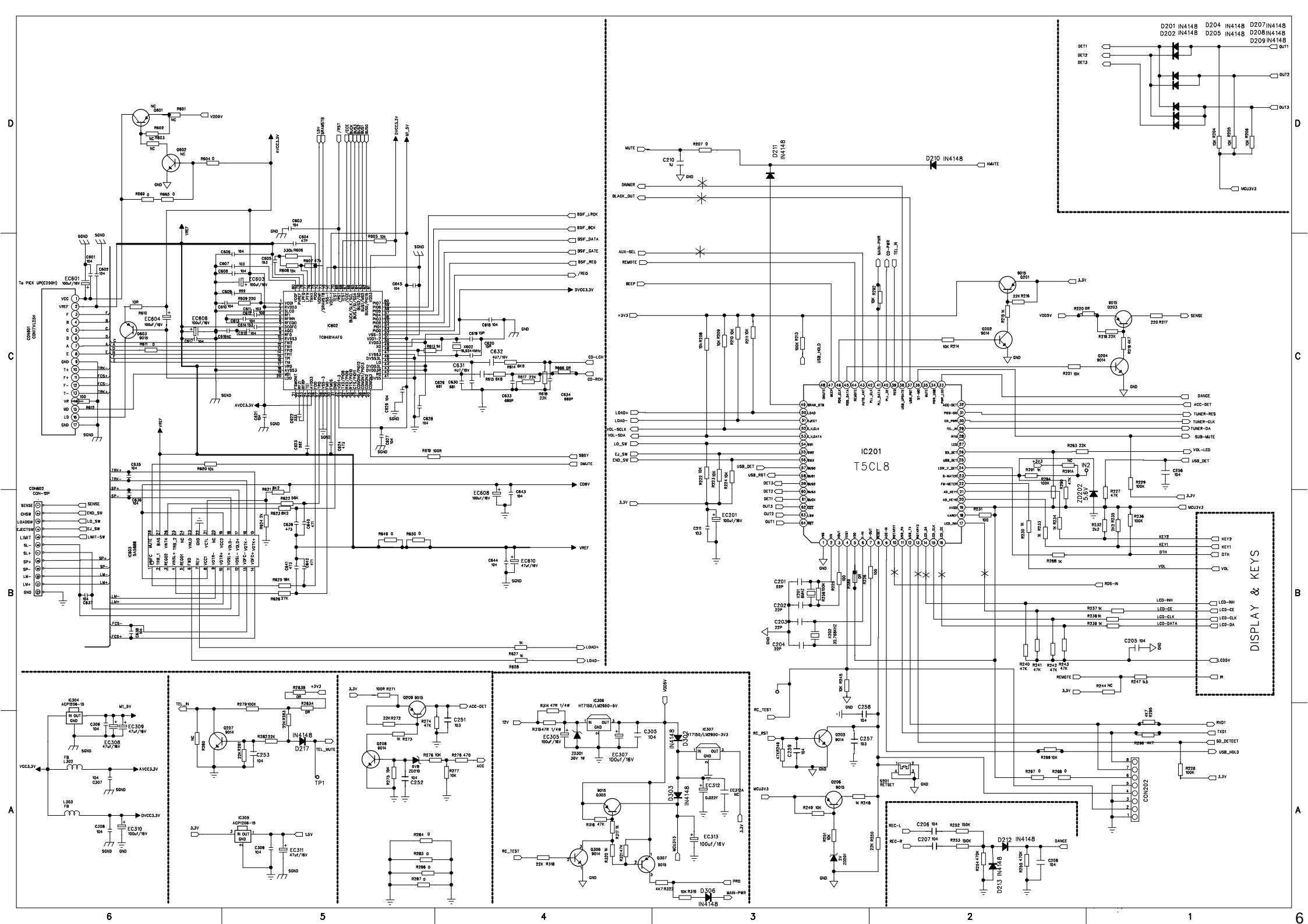
PHILIPS

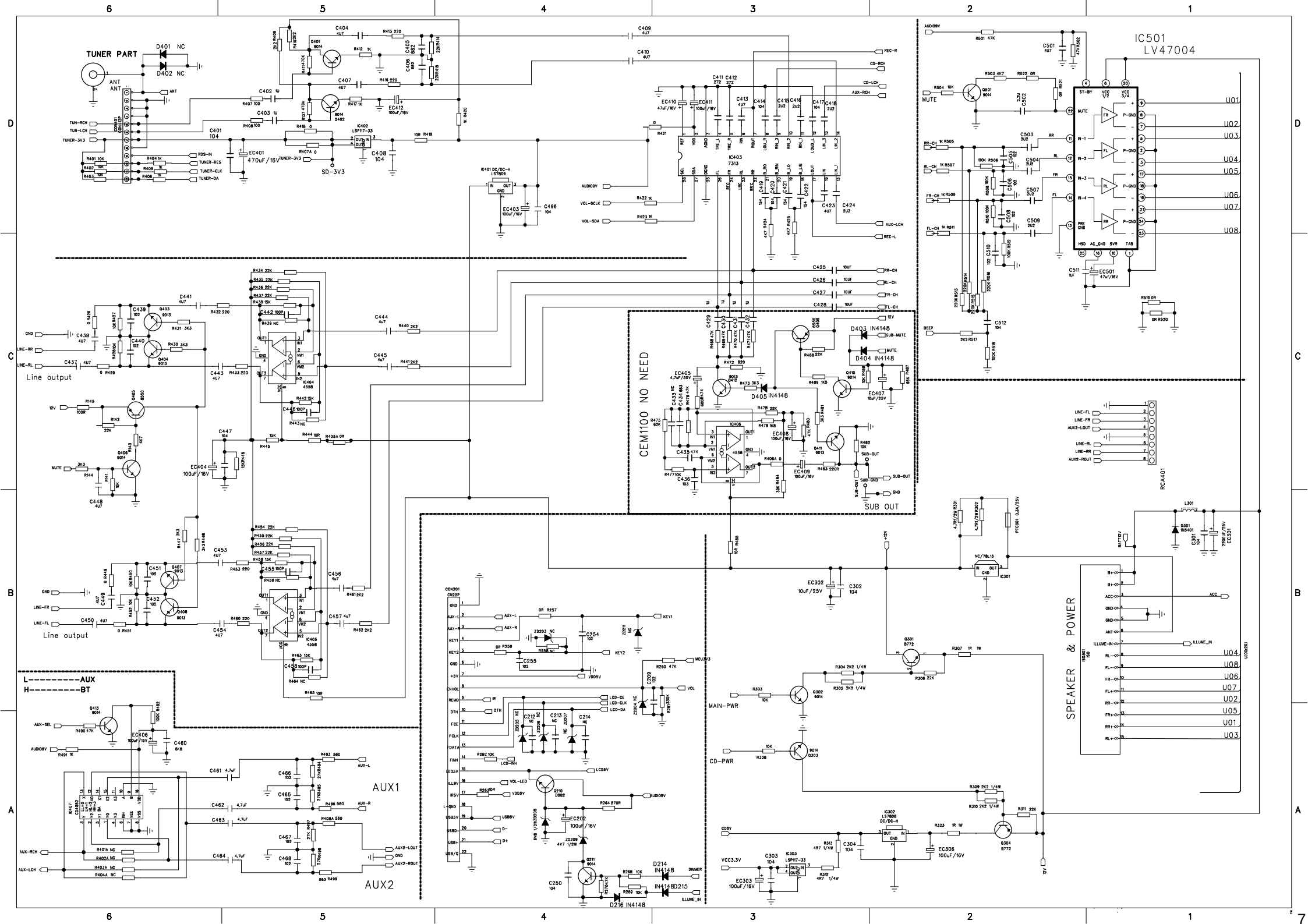

CEM2100 BLOCK DIAGRAM
ANT IN
TUNER Module
RDS Function=SI4745
Non RDS Function=SI4744
Amp Tuner Audio
Q401 Q402
IC403
Volume IC
7313
Sub-Woofer Out
Filter IC
4558
Sub-Woofer Out
Rear Line Out
Amp IC
4558
Fornt Line Out
Amp IC
4558
LINE OUTPUT
Rear AUX IN
Rear Aux_Audio
AUDIO
I2C
I2C
Power
AMP IC
LV47004
MCU
IC201
T5CL8 or TMP86FS49BUG
IC407
Audio Setting IC
4052
Audio Setting
SPEAKER OUTPUT
Panel
LCD
LCD Driver
SC75823
Function Key
Rotary encoder
REMOTE CON
RECEIVER
AUX IN
Front Aux_Audio
I2C
ISO
SPEAKER OUTPUT
BATT INPUT
ACC INPUT
AMP/ANT Remote OUT
illumination
CD AUDIO
IC602
DSP
TC94B14MFG
REMO CON
TRANSMTTER
R05
Disc
Optical Pick-up
I2C
IC604
USB SD/MMC Driver IC
T5CJ3-7G28(F,M)
IC603
Motor Driver IC
SA5888
USB Socket
SD/MMC CARD Socket

WIRING DIAGRAM

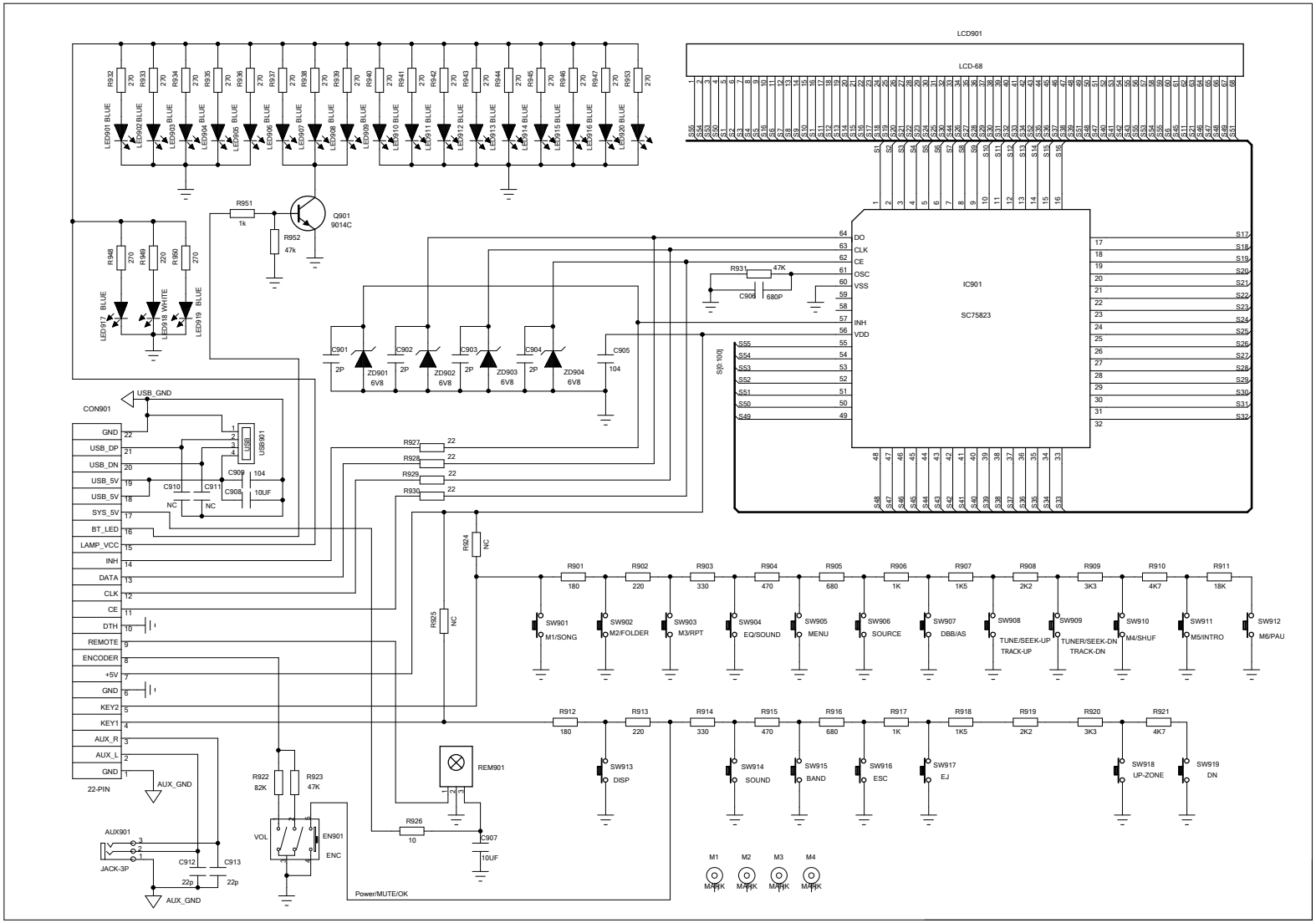



R668 0R
3.3V
R653 0R
R652 0R
Q604 9015
0R
R664
DVCC3A
R629 10K
R630 1K
/OE
10K
R631
/PWE
Q605
9014
IC702
DC/DC-H
L7805
AUDIO9V
R714
2R2 1/4W
R715
2R2 1/4W
IN
OUT
GND
USB5V
EC702
100uF/16V
EC703
100uF/16V
C704
104
22K R713
USB_DET
Q701
9014
D701 IN4148
D702 IN4148
USB
USB5V
D-
D+
GND
27R R711
27R R712
D+
D-
TVS1 NC
TVS2 NC
C702 33P
15K R709
10K R710
C703 33P
SD
CON701
SD_CLK
SD_DATAOUT
SD_DATAIN
SD_CS
SD_DETECT
SD3.3V
DVCC3A
OR R667
C649
104
C650
104
C646
104
R632 0R
R634 10R
R633 10K
R630 0R
R637 10K
1K R636
10K R638
R639 10K
R640 100
C647
22p
C648
22p
X603
8MHZ
IC604
BP3
TSC33-7G28(F,M)
R642 100K
R643 10K
R644 1K
R645 10K
R646 10K
R647 27K
C651
103
D602
IN4148
D601
IN4148
EC613
47u/16V
EC614
47u/16V
C652
10p
C653
10p
R648 10K
X601
32.768KHz
R651 10K
RR601 10K
RR602 10K
R641 10K
RR603 10K
R652 10K
RR604 10K
R653 0R
R655 100K
RR605
10K
RR606
10K
RR607
10K
RR608
10K
DMUTE
SRAMSTB
/RST
3.3V
DVCC3A
Remark:
1,if no EEPROM in Eeprom mode,SCL and SDA pull down
+3V3
10K/R654
10K R655
10K R656
10K R657
10K/R658
10K/R659
10K/R660
10K/R661
LIMT-SW
/CCE
BUS0
BUS1
BUS2
BUS3
BUCK
CD-RCH
GND
CD-LCH
DMUTE
/CCE
BUCK
BUS3
BUS2
BUS1
BUS0
/REQ
GND GND
L304
10UH
7
G1
VDD1
VDD
1
2
GND

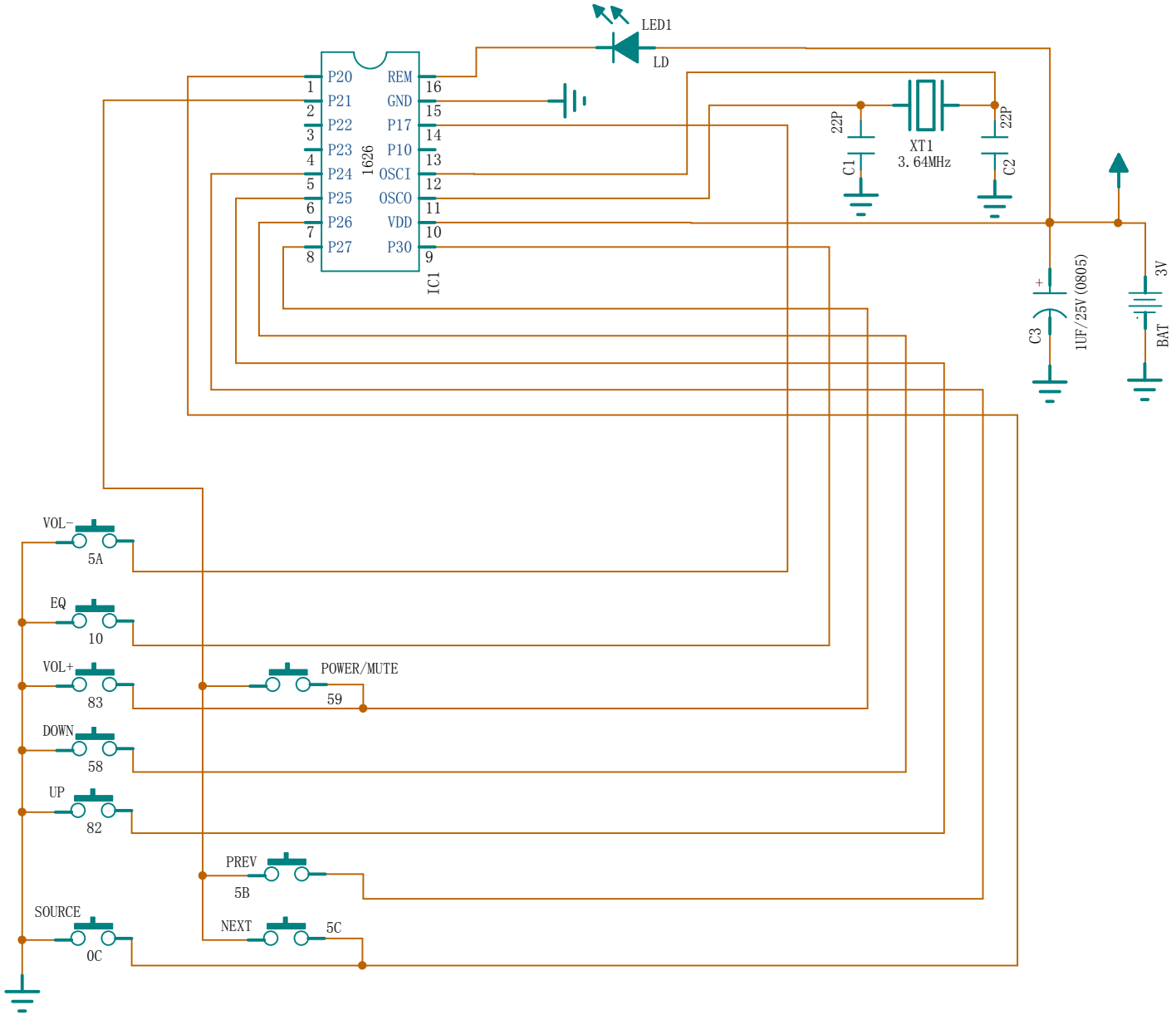

IC201
T5CL8
IC602
TC94B14AFG
IC603
SA5888
DISPLAY & KEYS
CON202
D201 IN4148
D202 IN4148
D204 IN4148
D205 IN4148
D207 IN4148
D208 IN4148
D209 IN4148
D210 IN4148
D211 IN4148
D212 IN4148
D213 IN4148
D217
D301
D302
D303
D306
IC304 ACP1206-15
IC305 ACP1206-15
IC306 HT7150/LM2950-5V
IC307 HT7150/LM2950-3V3
ZD202 5.6V
ZD301 30V 1W
ZD2051
X201 8MHZ
X202 32.768KHZ
X602 16.9344MHz
CON601 CON17A-125H
CON602 CON-12P
To PICK UP(CD50H)
BSF_LRCK
BSF_BCK
BSF_DATA
BSF_GATE
BSF_REQ
/REQ
DVCC3.3V
SBSY
DMUTE
CDBV
CD-LCH
CD-RCH
VREF
AVCC3.3V
DVCC3.3V
M1_5V
5.6V
3.3V
MCU3V3
VDD5V
ACC-DET
TEL_MUTE
TP1
MUTE
DIMMER
BLACK_OUT
AUX-SEL
REMOTE
BEEP
+3V3
AMUTE
MAIN-PWR
CD-PWR
TEL_IN
SENSE
LOAD+
LOAD-
VOL-SCLK
VOL-SDA
LO_SW
EJ_SW
END_SW
USB_DET
USB_RST
DANCE
ACC-DET
TUNER-RES
TUNER-CLK
TUNER-DA
SUB-MUTE
VOL-LED
USB_DET
KEY2
KEY1
DTH
VOL
LCD-INH
LCD-CE
LCD-CLK
LCD-DA
LCDSV
IR
REMOTE
RC_TEST
RC_RST
S201 RESET
RXD1
TXD1
SD_DETECT
USB_HOLD
REC-L
REC-R
LM+
LM-
FCS+
FCS-
TRK+
TRK-
SP+
SP-
LOAD
LOAD-
DET1
DET2
DET3
OUT1
OUT2
OUT3
MCU3V3


TUNER PART
D401 NC
D402 NC
ANT
IC501
LV47004
CEM1100 NO NEED
SUB OUT
Line output
Line output
AUX1
AUX2
SPEAKER & POWER
MAIN-PWR
CD-PWR
L----------AUX
H----------BT

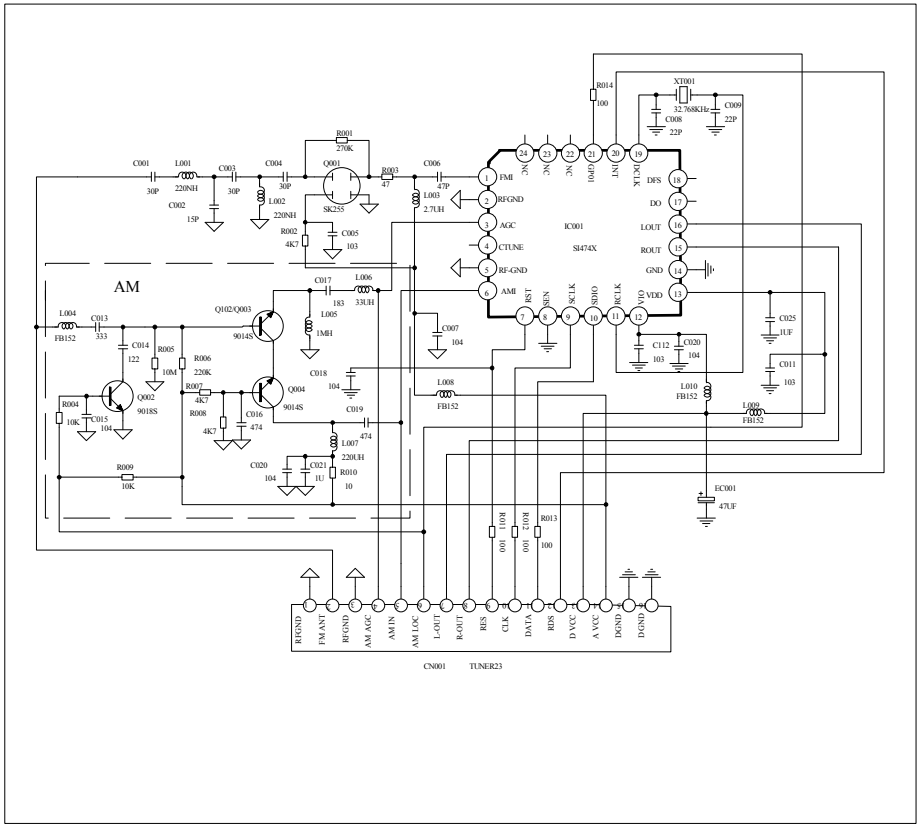
CIRCUIT DIAGRAM -PANEL BOARD



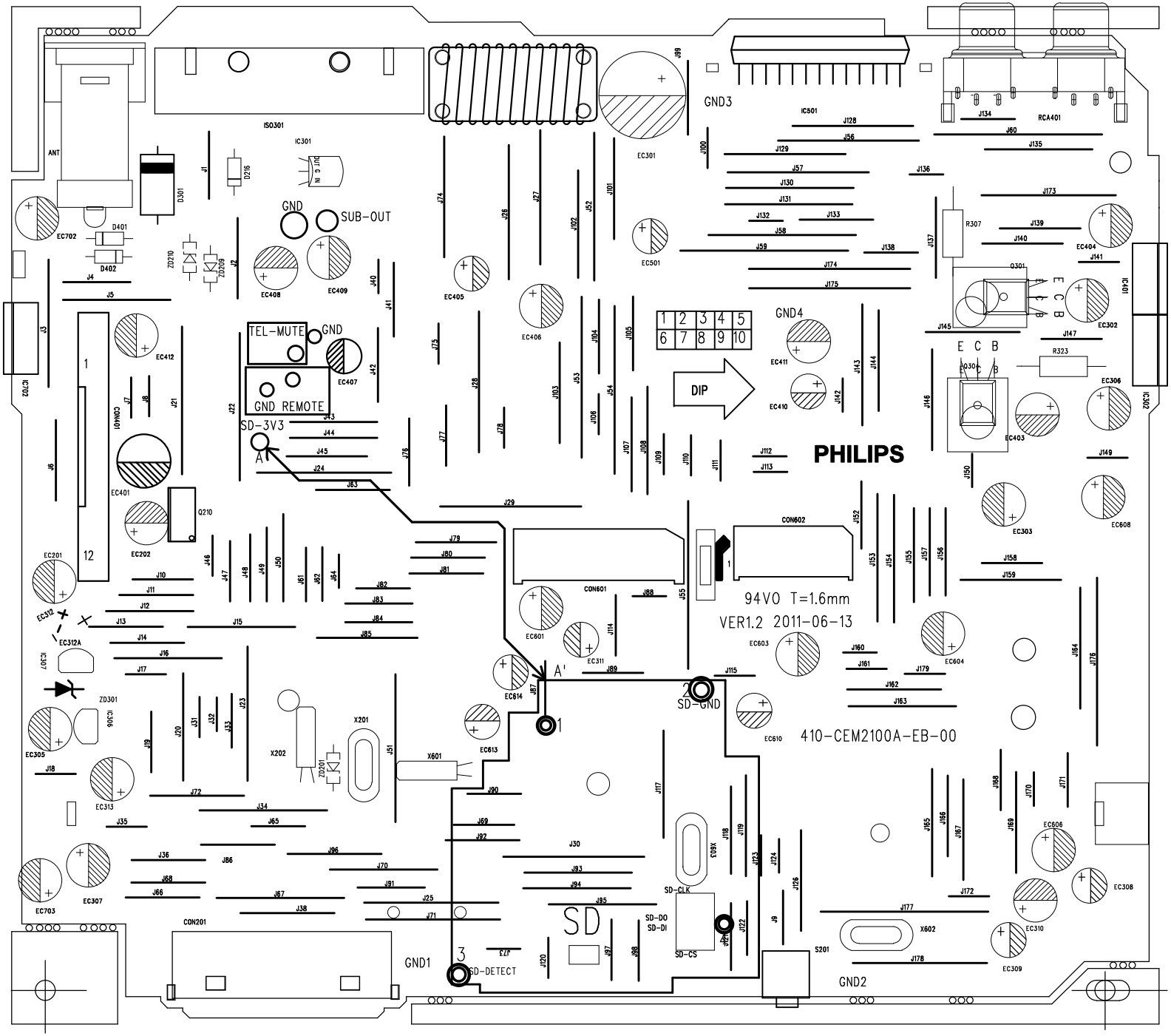
CIRCUIT DIAGRAM-REMOTE BOARD



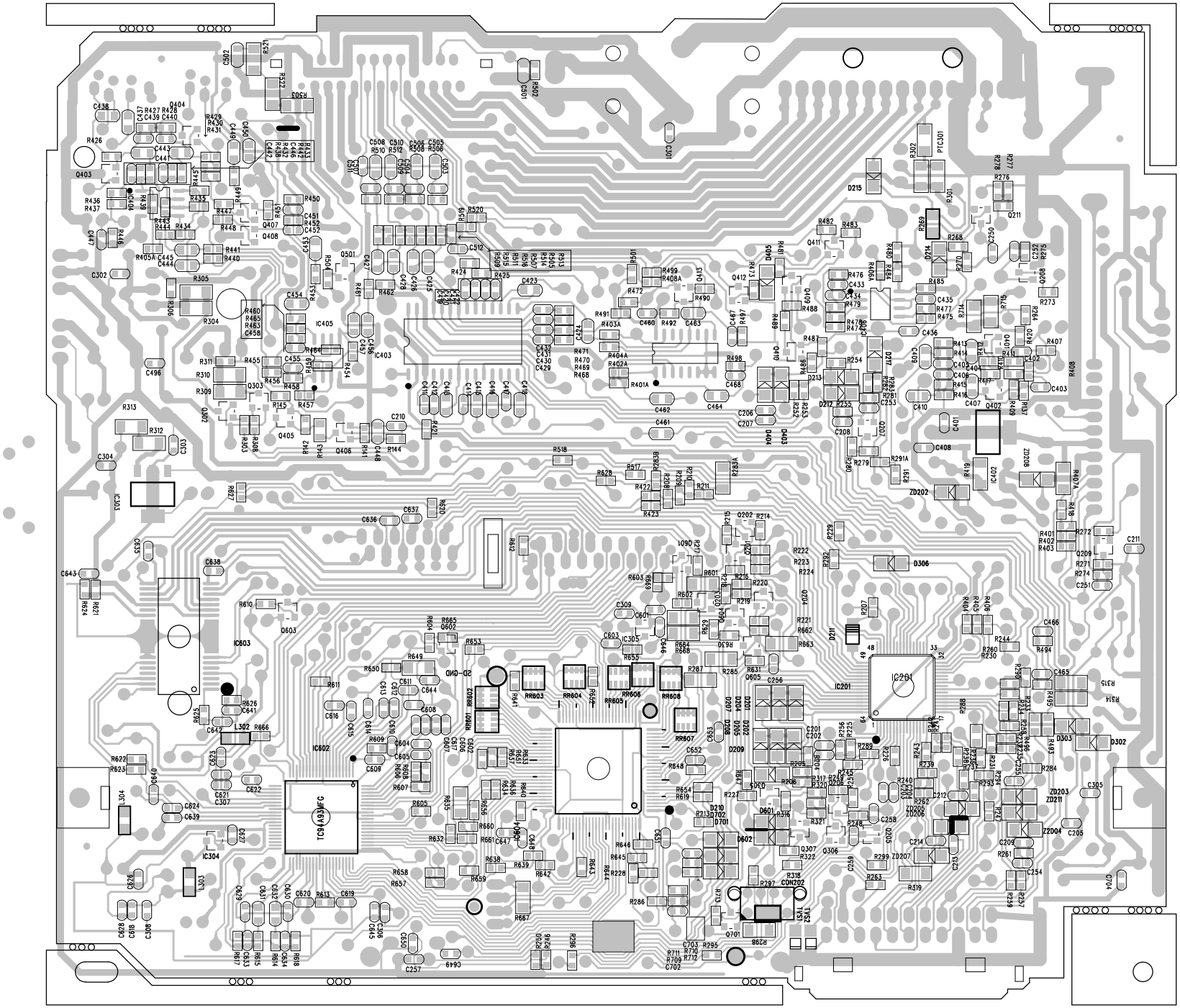
CIRCUIT DIAGRAM-TUNER BOARD



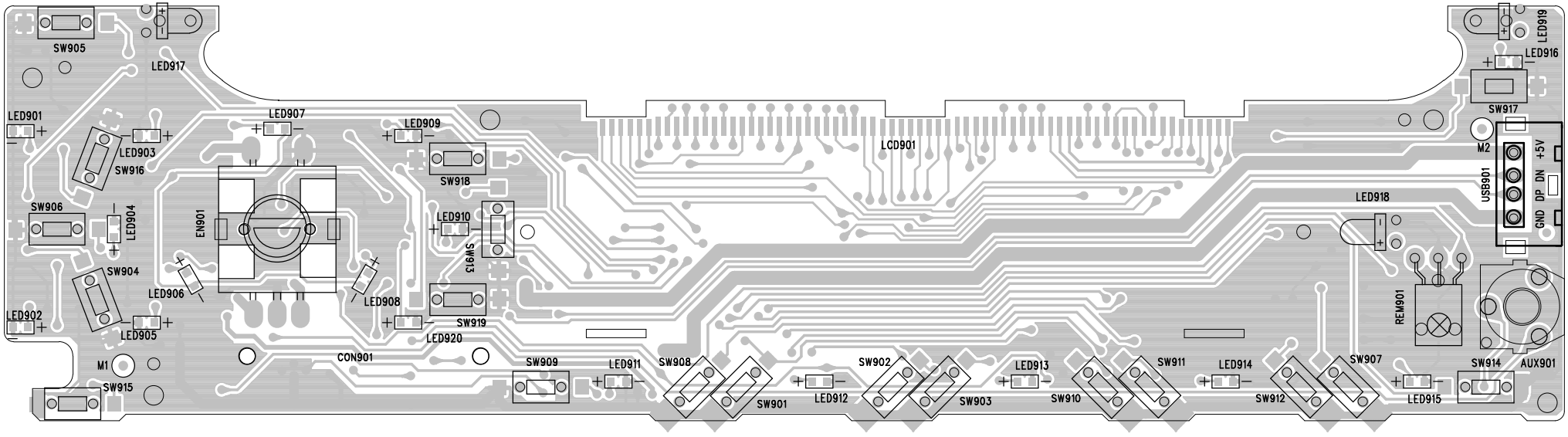
PCB LAYOUT-MAIN BOARD TOP SIDE VIEW



PCB LAYOUT-MAIN BOARD BOTTOM SIDE VIEW

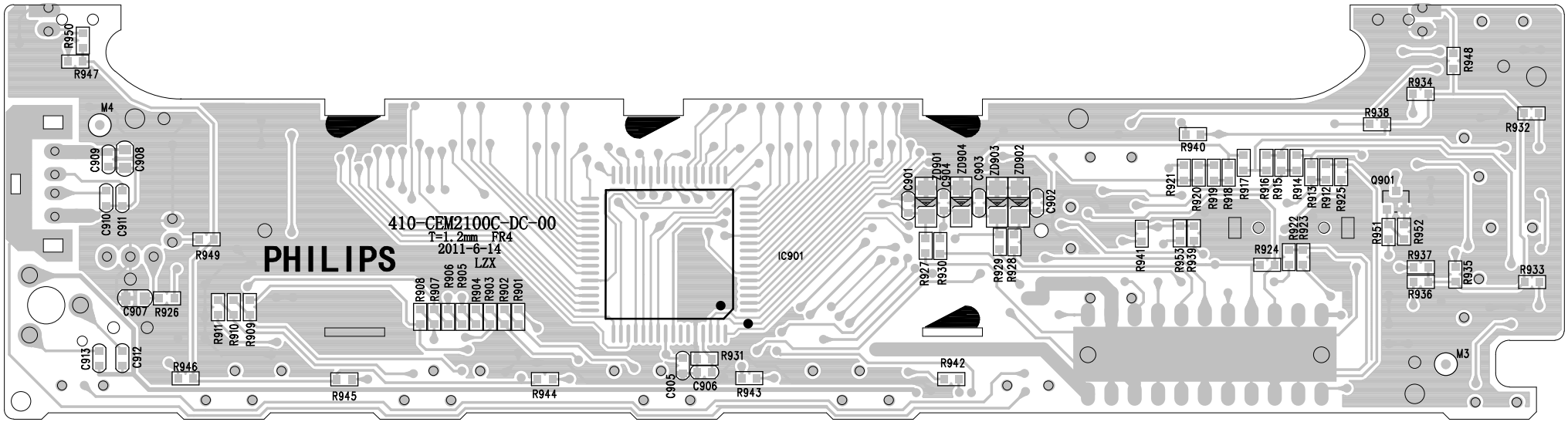


PCB LAYOUT -PANEL BOARD TOP SIDE VIEW

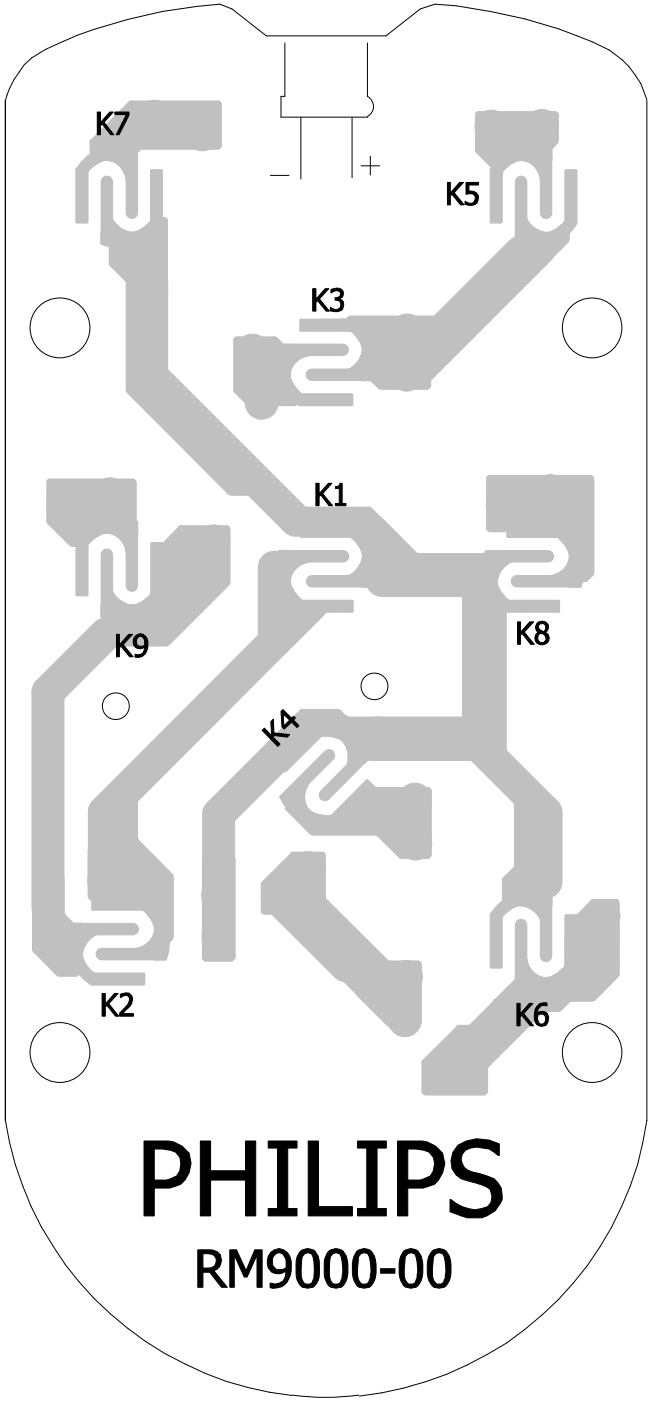


-

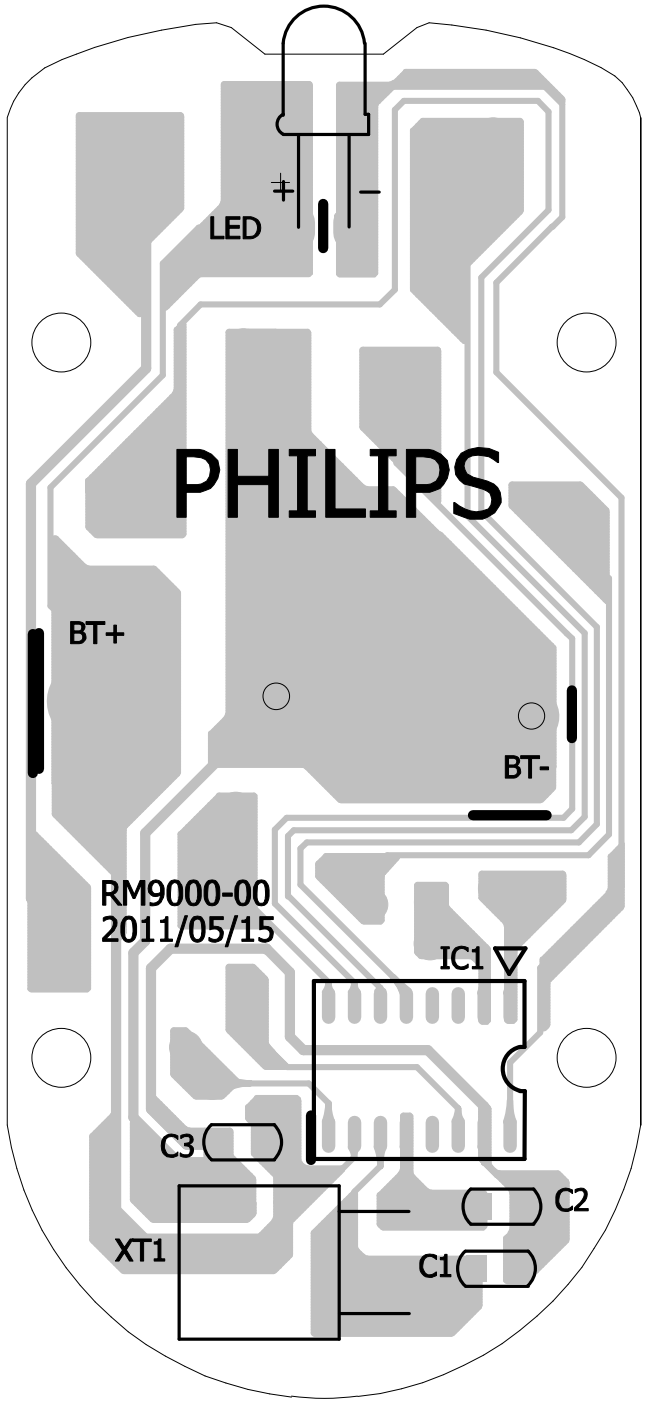
PCB LAYOUT -PANEL BOARD BOTTOM SIDE VIEW



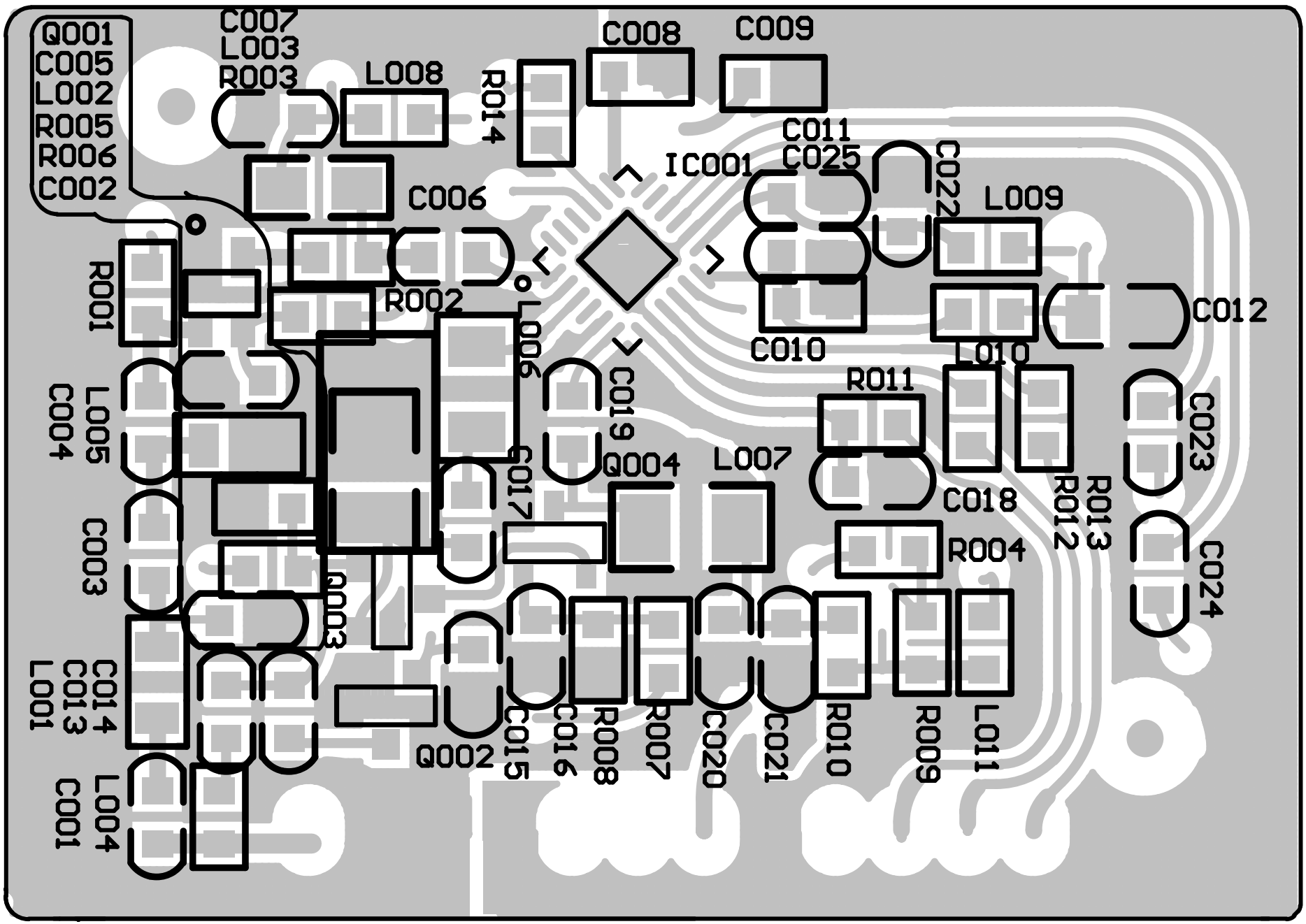
PCB LAYOUT-REMOTE BOARD TOP SIDE VIEW



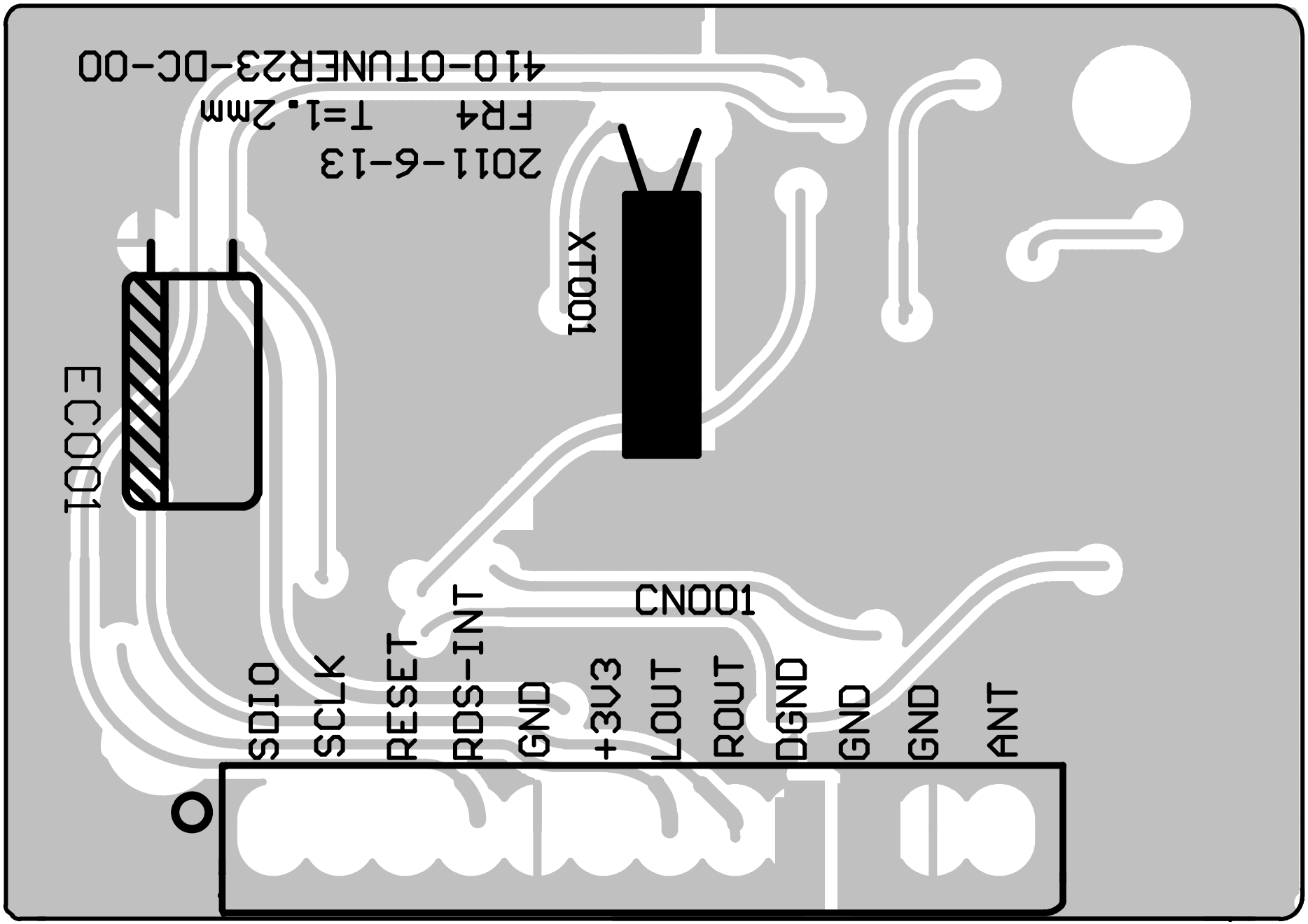
PCB LAYOUT-REMOTE BOARD BOTTOM SIDE VIEW



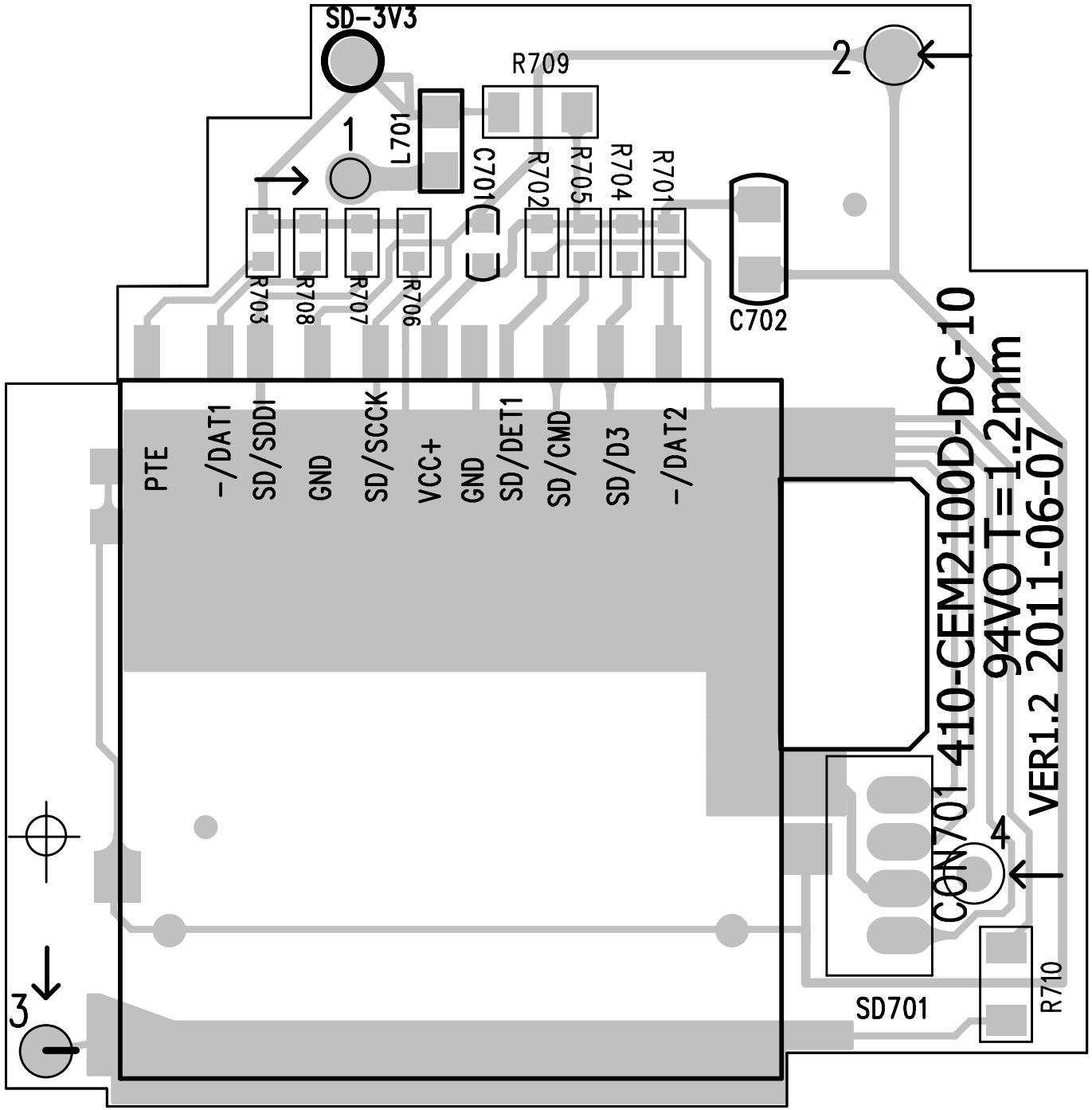
PCB LAYOUT -TUNER BOARD TOP SIDE VIEW



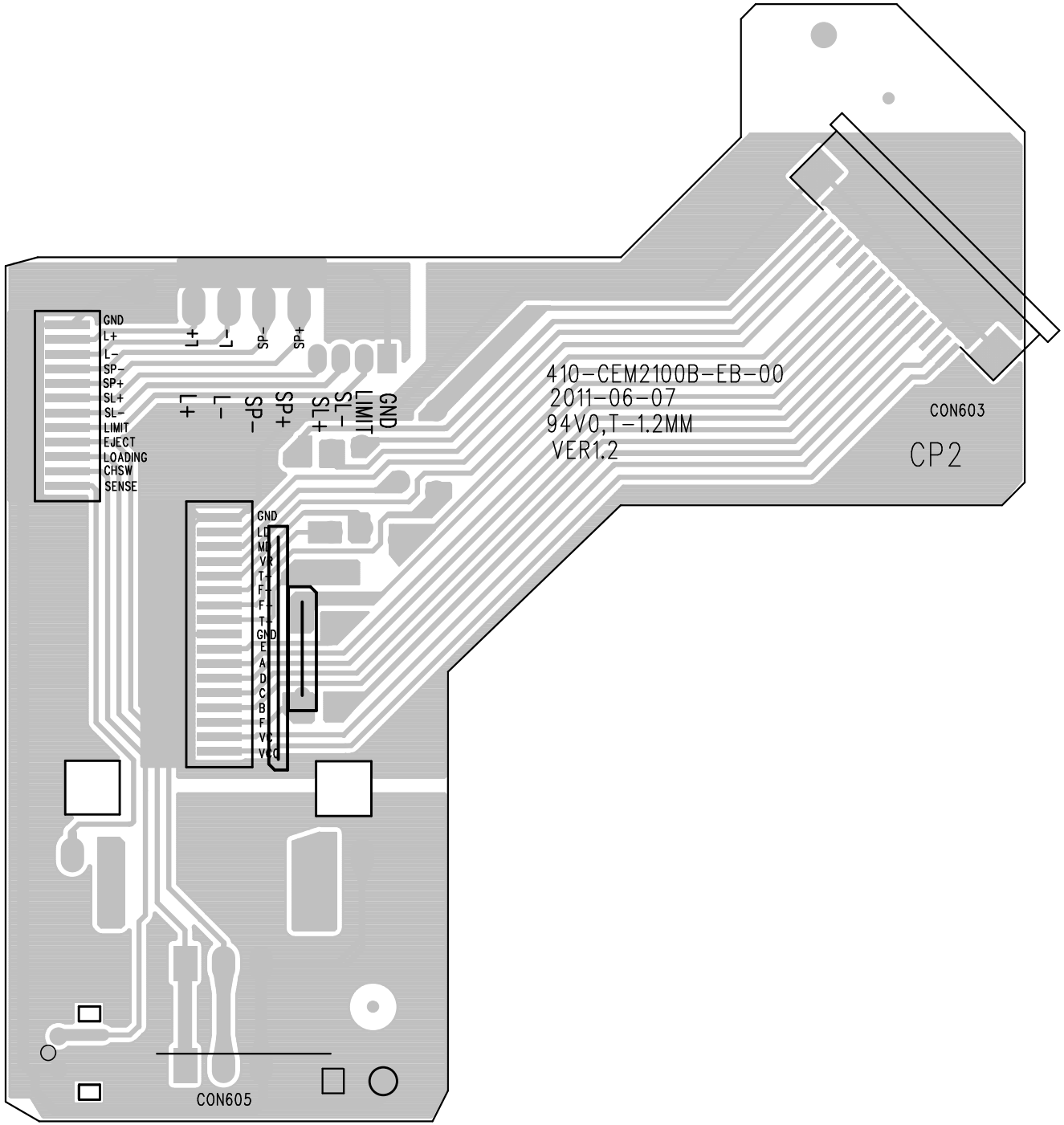
PCB LAYOUT -TUNER BOARD BOTTOM SIDE VIEW



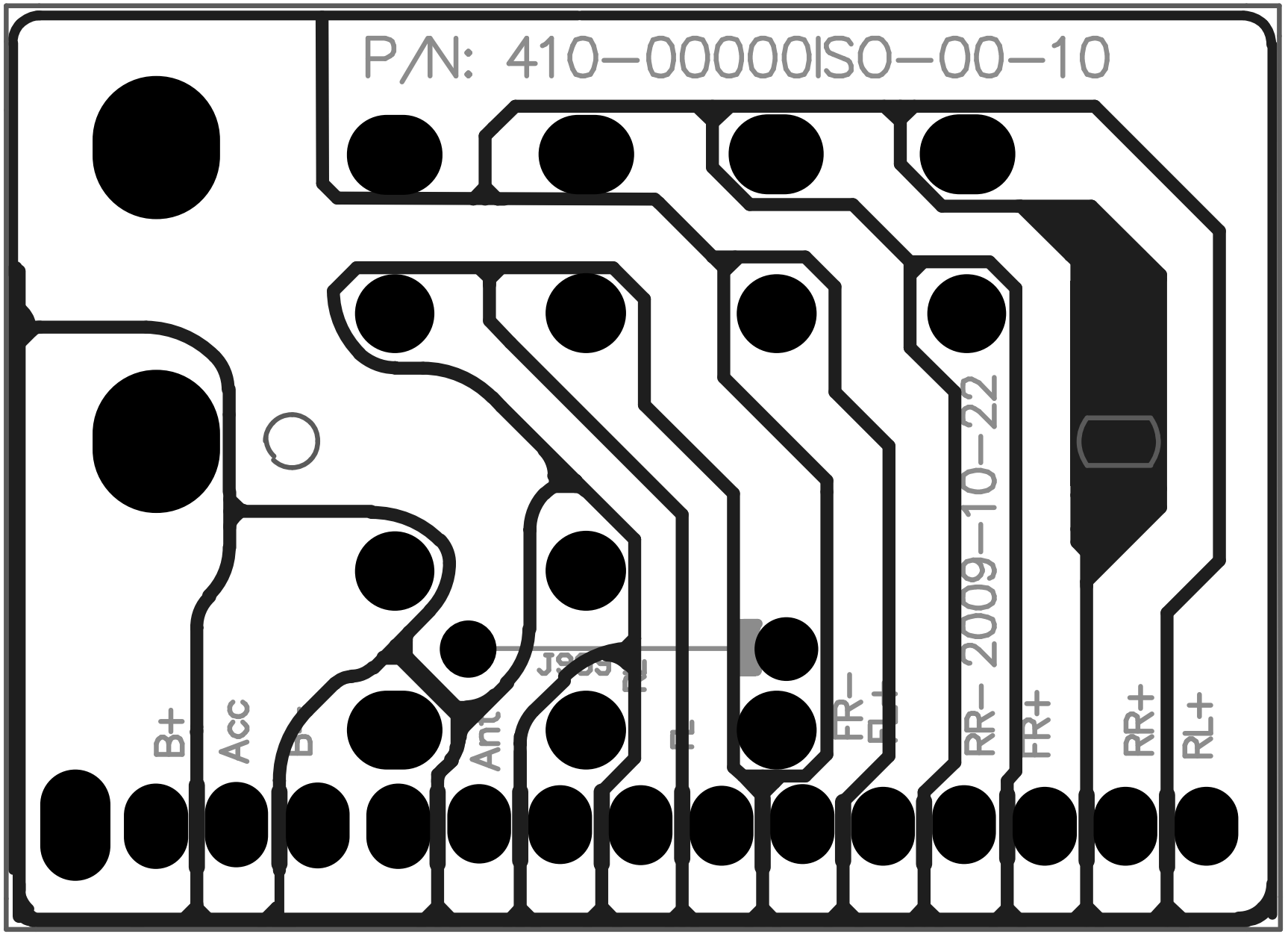
PCB LAYOUT-SD BOARD TOP SIDE VIEW

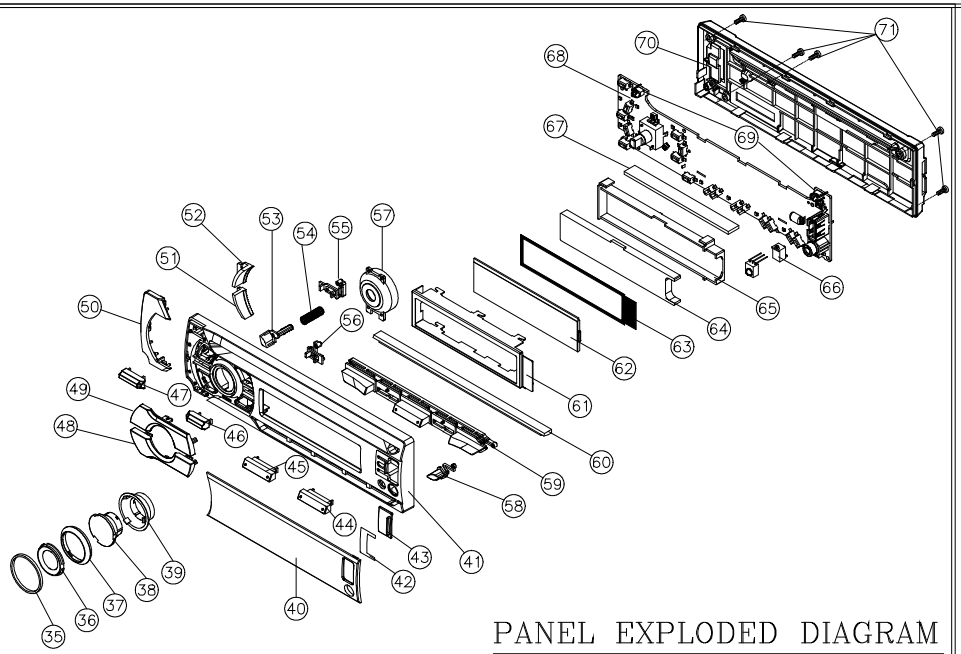


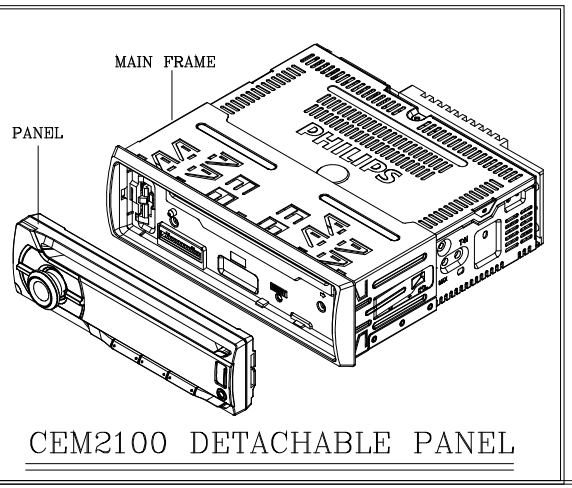
PCB LAYOUT CD CONNECTOR TOP SIDE VIEW

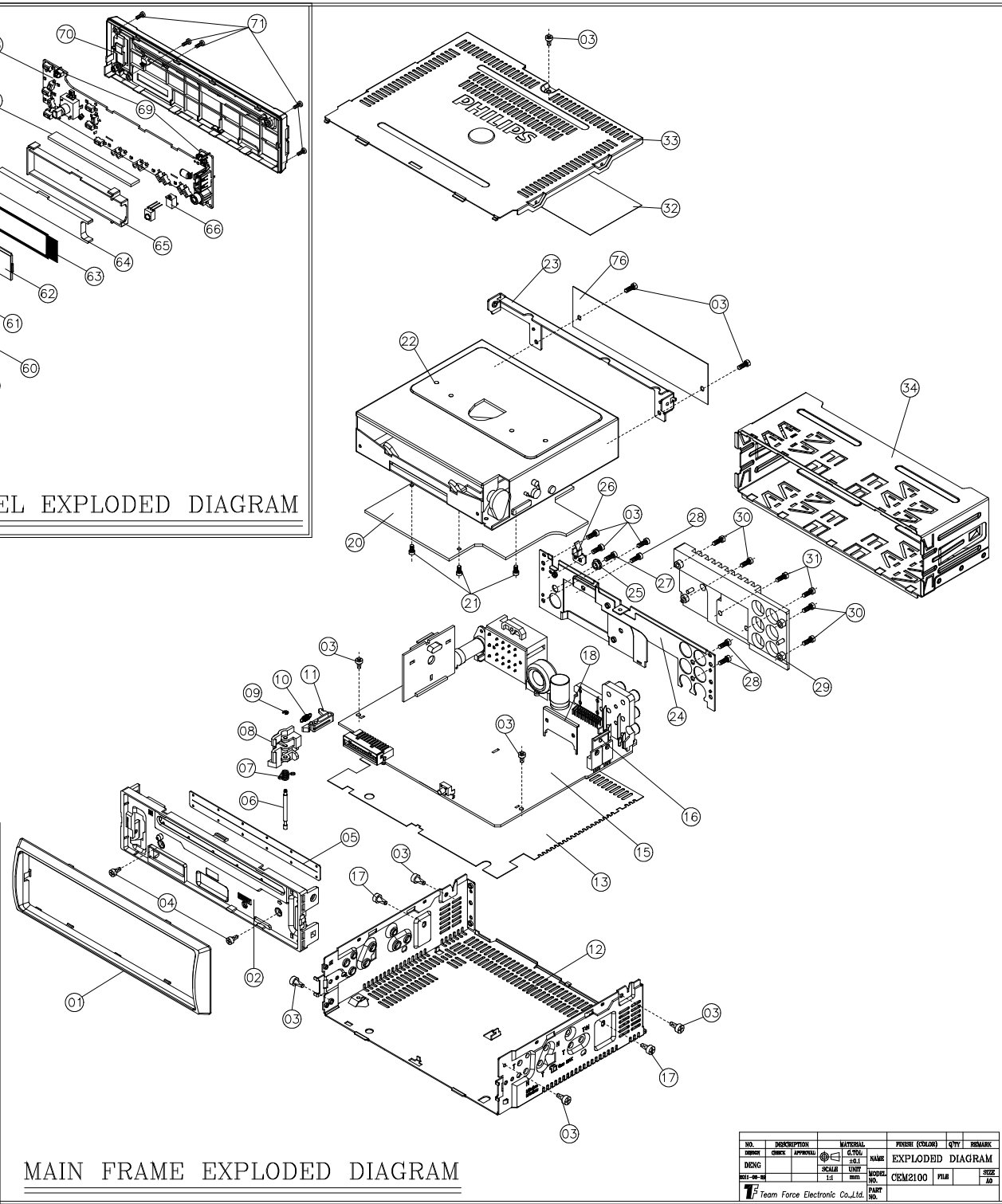


PCB LAYOUT-ISO BOARD BOTTOM SIDE VIEW









NO.	DESCRIPTION	MATERIAL	FINISH (COLOR)	Q'TY	REMARK
DESIGN	CHECK APPROVAL	0.70t			
DENG		±0.1	NAME	EXPLODED DIAGRAM	
		SCALE 1:1	UNIT mm	MODEL NO.	CEM2100
2011-09-16				FILE	SIZE A0
Team Force Electronic Co.,Ltd.				PART NO.	

NO.	PART NUBER	DESCRIPTION	QTY
77			
76	701-CEM310003-00-00	FIBRE SHEET	1
75			
74			
73			
72			
71	660-TBH20083-24-00	SCREW 2.0x8.0mm	5
70	600-CEM310007-00-00	BACK PANEL	1
69	600-CEM310032-00-00	LED BRACKET	2
68	410-CEM2100C-DC-00	PANEL PCB	1
67	443-82008220-00-00	RUBBER CONTACT	1
66	600-CEM310030-00-00	SENSOR-BRACKET	1
65	600-CEM200024-00-00	LCD HOLDER	1
64	600-CEM200025-00-00	LCD REFLECTOR	1
63	704-CEM200001-00-00	LCD DIFFUSION SHEET	1
62	440-0C352494-00-00	LCD	1
61	650-CEM200006-00-00	LCD BRACKET	1
60	600-CEM310011-00-00	CD-SLOT-ILLU.	1
59	600-CEM310023-00-00	SET BUTTON "D"	1
58	600-CEM310022-00-00	BUTTON CD Eject	1
57	600-CEM310012-00-00	VOL-REFLECTOR	1
56	600-CEM310027-00-00	BUTTON BRACKET"B"	1
55	600-CEM310026-00-00	BUTTON BRACKET"A"	1
54	650-CEM20011-00-00	PANEL RELEASE SPRING	1
53	600-CEM310029-00-00	BUTTON "RELEASE"	1
52	600-CEM310014-00-00	BUTTON ILLU.-A	1
51	600-CEM310015-00-00	BUTTON ILLU.-B	1
50	600-CEM310028-10-00	SET BUTTON "A"	1
49	600-CEM310020-00-00	SET BUTTON "B"	1
48	600-CEM310021-00-00	SET BUTTON "C"	1
47	600-CEM310018-00-00	BUTTON "A	1
46	600-CEM310019-00-00	BUTTON "B"	1
45	600-CEM310024-00-00	BUTTON "C"	1
44	600-CEM310025-00-00	BUTTON "D"	1
43	600-CEM310031-00-00	USB Cover	1
42	705-CEM200001-00-00	PC SHEET T=0.15mm	1
41	600-CEM310006-00-00	FRONT PANEL	1
40	600-CEM310008-00-00	LENS (USB)	1
39	600-CEM310016-00-00	KNOB-COVER-A	1
38	600-CEM310013-00-00	KNOB REFLECTOR	1
37	600-CEM310017-00-00	KNOB-COVER-B	1
36	600-CEM310010-00-00	KNOB-COVER-LENS	1
35	444-CEM310001-00-10	RUBBER Ring "A"	1
34	650-CEM200005-00-00	HALF-SLEEVE	1
33	650-CEM310002-00-00	TOP COVER	1
32	703-CEM310001-00-00	DUST PROOF WEB CLOTH	1
31	660-MPH30160-21-00	SCREW 3.0x16mm	2
30	660-EBH2608B-21-00	SCREW 2.6x10mm	4
29	650-CEM310006-05-00	HEAT SINK	1
28	660-TPH30101-21-00	SCREW 3.0x10mm	3
27	660-EBH2608B-21-00	SCREW 2.6x8mm	1
26	650-CEM310007-00-00	WIRE-CLAMP	1
25	600-FIX10031-00-00	Patch Plastic-PA-66	1
24	650-CEM310004-00-00	BACK-COVER (CD)	1
23	650-CEM310003-00-00	DECK BRACKET(BACK)	1
22	432-SCD300LK-00-31	CD MECHANISM	1
21	660-EPH2005B-27-00	SCREW 2.0x5mm	3
20	410-CEM2100B-EB-00	CD Connect PCB	1
19			
18	650-SM885A07-00-00	IC BRACKET	1
17	660-MPH30060-21-00	SCREW 3.0x6.0mm	2
16	650-000SL835-00-00	7808 IC BRACKET	2
15	410-CEM2100A-EB-00	MAIN PCB	1
14	410-CEM2100D-DC-10	SD PCB	
13	701-CEM310001-00-00	FIBRE SHEET	1
12	650-CEM310001-00-00	MAIN BRACKET	1
11	600-CEM310003-00-00	PANEL LOCKER B	1
10	650-CEM200010-00-00	SPRING "B"	1
09	661-ERM01500-04-00	"E" RING	1
08	600-CEM310002-00-00	PANEL LOCKER A	1
07	650-CEM200009-00-00	SPRING "A"	1
06	650-CEM200011-00-00	PIN	1
05	703-CEM200002-00-00	CD DUSTPROOF FELT	1
04	660-EBH2606B-24-00	SCREW 2.6x6	2
03	660-EBH2605B-21-00	SCREW 2.6x5	12
02	600-CEM310001-00-00	BASE PANEL (SD)	1
01	600-CEM310005-00-00	TRIM PLATE	1

CEM2100

Trouble shooting

CEM2100 Trouble shooting

Product Model	**CEM2100**	Area	All Area	Date	2011-11-14

NO.	failure phenomena	failure cause	remark
1	NO Power	a. To check whether it is connect well of the ISO connector (4PIN power input). Whether it is loose of the 15A fuse of the ISO connector, or insert non in place	
		b. To check whether the reset button Sw201 is long term functional then caused short circuit and no power	
		c. To check whether there is any contamination and bad contact on the 22 Pin male/female connector on the panel and main board	
		d. To check the power supply of main board B+、ACC should be +12V; The voltage of stabilivolt of ACC power supply wire ZD210 (6V8) should be 6V8	
		e. To check the voltage of the 19 pin (AVDD) of MCU (T5CL8) should be +3V3; The output voltage of IC307 (LM2950) should be +3V3	
		f. To check the oscillation frequence of crystal X201 , shuold be 8MHz, and for the crystal X202 should be 32.768KHZ	
		g. To check Panel LED +5V voltage , should be normal	
2	NO audio output	a. To check whether the volume knob is turn to the minimum position	
		b. To check whether the unit is at MUTE mode, press SOURCE button and check whether it is effective of the input sound source	
		c. To check whether the connection of 8PIN audio output wire of ISO connector is correct; wrong connection or short circuit to the ground will caused the protection of the power amplifier(no voltage output)	
		d . To check the circuit of power amplifier IC501 (LV47004) and VOL IC403 (PT7313E)	
		e. To check the normal voltage of 22 PIN(MUTE) of power amplifier IC501(LV47004) , normally should be 4V	
		f. To check the voltage of control PIN SDA、SCL（the 27、28pin）of audio processor IC403（PT7313E）, should be +3V3	
3	Radio abnormal	a. To check the antenna of the tuner	
		b. To check whether the strength of then input signal of the tuner is too weak	
		c. To check the voltage of the 7 pin(VDD) of the tuner , should be +3V3	
		d. To check the voltage of the 10 pin(RES) of the tuner, should be +3V6; the 11 pin(CLK) should be +3V1; the 12 pin(date) should be +2V8	
		e. To check the oscillation frequence of crystal XT001 of the tuner, should be 32.768KHZ	
		f. To check the L output voltage of the 5 pin of tuner should be 1V5, the 6 pin R output voltage , should be 1V5	

NO.	failure phenomena	failure cause	remark
4	CD defective	a. To check whether the signal format of the disc is correspond to the request of the unit, whether there is any contamination or damage or light leakage on the surface of the disc	
		b. To check whether there is any abnormal of the rotation of the deck mecahnism, or whether the disc is enter in position	
		c. To check whether it is normal when reading USB?	
		d. To check whether the 17 P FFC of laser pick up is inserted in place, whether the socket of it is loose	
		e. To check whether there is any contamination or foreign body on the surface of the laser pick up	
		f. To check the servo connector of CON601、CON602	
		g. To check the oscillation frequence of crystal X602 , should be 16.9344M	
		h. To check the oscillation frequence of crystal X603 , should be 9MHZ	
		i. To check the voltage of the 50 pin of IC 602, should be 3.3V	
		j. To check the switch S601 on the servo board	
		k. To check the rotation mechanism of CD deck mechanism	
		l. To check the voltage of the 8 pin of IC 603, should be +8V	
		m. To check whether the rotation belt of deck mechanism is dislocation or loose	
5	USB defective	a. To check whether the USB signal format is correspond to the request of the unit	
		b. To check the voltage of the the uppermost pin of the USB connector, should be +5V	
		c. To check the voltage of the first pin of main board IC604 , should be +3V3, when insert USB, the voltage of the second pin should be +3V, if no insert the USB, the voltege should be 0V	
		d. To check whether there is any wearing and scratch of the shrapnel and pin of the USB.	
		e. To check the oscillation frequence of the 7 pin of main board IC604, should be 32.768KHZ	
		f. To check whether there is any contamination and bad contact on the male/female connector of the panel and main board. If necessary, can exchange the panel to test whether the defective is occurred by the unit or panel.	
6	AUX defective	a. To check the SOURCE shoule be in MP3-LINK mode	
		b. To check the AUX IN input signal	
		c. To check whether there is any contamination and bad contact on the male/female connector of the panel and main board. If necessary, can exchange the panel to test whether the defective is occurred by the unit or panel.	

CD/SD/USB MP3/WMA/ESP player system

T5CJ3-7G28(F,M)

Technical Specification

Ver 1.0

2010-4-7

This product is a strategic material (or service) as defined by the Foreign Exchange and Trade Control Laws.
Permission must be gained under these laws before the product is exported.

Toshiba Corp.

- The contents of this specification are subject to change without notice.
- The technical information provided in this document is for describing typical operations and applications of the product and does not guarantee the intellectual or other property rights of Toshiba Corp. or third parties, nor constitutes an approval of the right of execution.

Contents

1 Introduction 4
2 System feature 4
3 Function outline 6
4 System composition 7
4.1 System configuration 7
4.2 System block diagram 8
4.3 BlackPepper3 pin layout 9
4.4 BlackPepper 3 pin assignment and description 10
5 Communication and command 12
5.1 Communication protocol 12
5.2 Command list 13
5.3 Command data field detals 17
6 Function details 27
6.1 Reset and select your pick-up 27
6.2 Get firmware version and set firmware feature 27
6.3 Detect USB device and SD card 29
6.4 Select a mode 30
6.5 Read USB/SD/CD(without CD-TEXT) 31
6.6 Play/up/down/dir up/dir down/track number auto change 33
6.7 Get play information 35
6.8 Play/Pause/FF/FR playing status change 36
6.9 Stop 39
6.10 Play end 40
6.11 About BlackPepper3 status 41
6.12 Get File name 42
6.13 Get Folder name 42
6.14 Get ID3 information 43
6.15 Get bitrate and sample frequency informaiton 44
6.16 Set repeat/intro/random play mode 47
6.17 MSF play function(CD-DA only) 49
6.18 Select folder or file 50
6.18.1 Select a folder and inside file to get their name 51
6.18.2 Select a file to get its located folder number 52
6.18.3 Select a folder to get folder inside information 53
6.19 Bookmark setting and play 53
6.20 A-B repeat setting and play 54
6.21 CD-TEXT analysis and reading 55
6.22 CD/USB/SD mode switch 58
6.23 About audio mute pin 60

6.24 About driver mute pin 61
6.25 Flash upgrading 61
6.26 Host MCU upgrading 63
6.27 About error code 64
6.28 About standby and resume play 65
6.29 Set play position and recovery play 66
6.30 Transfering cofficient data 68
6.31 About E2PROM function 71
7 Recommanded flow chart for host side software 74
7.1 Reset/get firmware version/set software feature flow 75
7.2 Mode switch/auto play/resume/recovery play flow 76
7.3 Play/track change/up/down/dir up/dir down flow 77
7.4 A-B repeat play flow 78
7.5 Host MCU upgrading flow 79
7.6 Flash upgrading flow 80
7.7 Program play flow 81
8 About characters coding 84

1 Introduction

T5CJ3-7G28(F,M) realizes a CD/USB/SD audio player system. It support audio track in CD and mp3,wma file in CD-ROM, USB mass storage device, MTP device, and SD card. It is composed of one TOSHIBA 32-bit high speed MCU with a USB host controller inside and one TOSHIBA audio DSP which integrated MP3/WMA decoder and CD servo controller.

* Term and Abbreviation

T5CJ3-7G28(FM) is also called BlackPepper3 in this specification. BlackPepper3 is a term in software scope. T5CJ3-7G28(FM) is the masking product name of BlackPepper3. BP3 is abbreviation of BlackPepper3.

2 System feature

Compatiable disc type

Audio CD:	support(sigle session)
CD-ROM:	support(single session or multi session)
MIX-CD:	support(single session, first track is data track, and other tracks are audio track)
CD-EXTRA	support(first session is audio session, second session is data session)

CD-ROM decoder

Format:	Compliant with ISO9660 level 1 and 2(mode 1 and 2, form 1)
PVD(SVD) management:	Analyze the PVD and SVD, and stores folder and file information in SRAM
Dir+File maximum number:	1024(B14) or 512(B13)
Dir maximum number:	511(B14) or 256(B13)
Folder names and file names:	Level1,2 and Remeo/Joliet are supported
Folder name, File name length:	64bytes(maximum)

USB and SD file management

Support format type:	FAT12, FAT16, FAT32
Long file name support:	VFAT
Maximum cluster size:	64KB
Maximum sector size:	4KB
Max folder number support :	128
Max file in one folder:	512
Max file in device :	65535
Max directory depth:	8.
Folder name, File name length:	64bytes(maximum)
ID3 title/artist/album:	The max number of bytes of title/artist/album is 30/30/30

MP3 decoder

File	MPEG1,2,2.5 Layer3
File extension	[.MP3]/ [.mp3]
Folder name, File name length:	64bytes(maximum)
ID3 TAG	Version2.4, Version2.3, Version2.2, Version1.1.Version1.0
ID3 title/artist/album	The max number of bytes of title/artist/album is 60/60/60.
Sampling rate (kHz)	48, 44.1, 32, 24, 22.05, 16, 11.025, 8
Bit rate (kbps)	8, 16, 24, 32, 40, 48, 56, 64, 80, 96, 112, 128, 144, 160, 192, 224, 256, 320 Variable bit-rates

WMA decoder

File	Windows Media Audio 9
File extension	[.WMA]/ [.wma]
Folder name, File name length:	64bytes(maximum)
ID3 title/artist/album	The max number of bytes of title/artist/album is 60/60/60.
Sampling rate (kHz)	48, 44.1, 32

Bit rate (kbps)	32 to 192

CD-TEXT

Language code	English(0x09)
Album	Maximum 64 bytes
Title	Maximum 64 bytes
Artist	Maximum 64 bytes

ESP feature

Only B14 has ESP feature.

3 Function outline

System function

- Internal pick-up or mechanism selection
- Update PUH COEF data from HOST or E2PROM
- Update PRAM for decoder from E2PROM
- Rom correction from E2PROM
- Standby in and low power comsumption
- Can connect a external flash and upgrading flash from USB memory
- Upgrade host MCU softare from USB memory

MP3/WMA play function

- Play, Pause,FF,FR and Stop
- Play by selecting file or selecting folder
- File up/down, Folder up/down
- Get folder or file info
- Resume play from standby
- Resume play from mode switch(CD/USB/SD mode switch)
- Repeat (1 /folder/all) Play
- Random play, folder random play(depend on repeat area)
- Intro play
- Repeat play A-B within one song
- Bookmark play

CD audio track play function

- Play, Pause, FF, FR and Stop
- Play by selecting track
- Track up/down
- Resume play from standby
- Resume play from USB/SD mode
- CD-TEXT function
- MSF play
- Bookmark play
- Repeat (1/All) Play
- Random play
- Intro play
- Repeat play A-B with in one song
- Data track will be auto skipped

4 System composition

4.1 System configuration

- 32-bit MCU with USB host controller

  T5CJ3-7G28(F,M)

- CD processor, MP3/WMA decoder, and audio DAC system

  B13: TC94B13FG-002

  B14: TC94B14MFG-202

- Pickup and CD mechanism

  Sanyo DA11(1x speed or 2x speed)

  Sany DA23(1x speed or 2x speed)

  Samsung B55(1x speed or 2x speed)

  Tanashin 2002(2x speed)

  Tanashin 2007(2x speed)

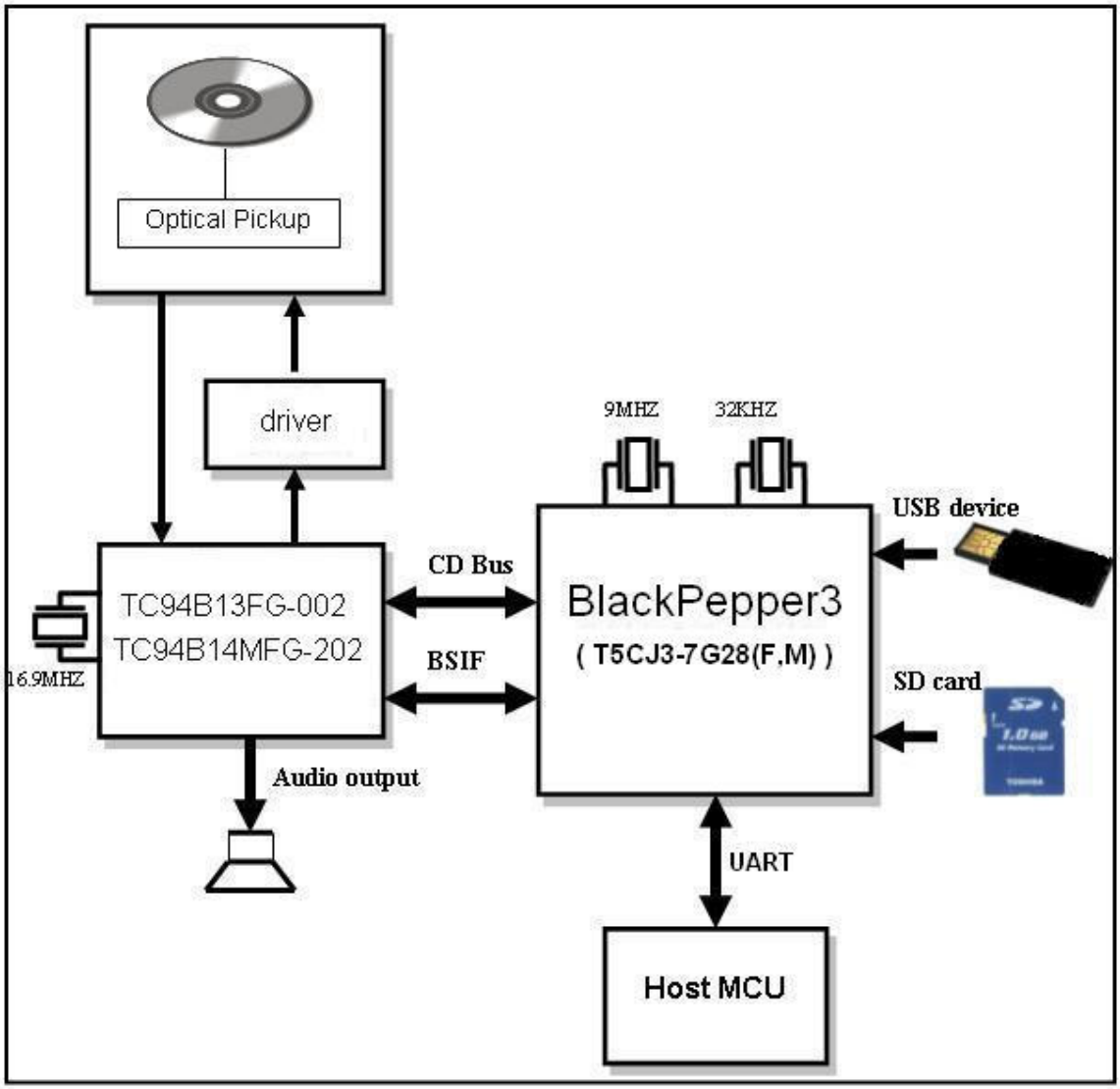
  Shinny IS68(2x speed)

  Shinwa CLC01(2x speed)

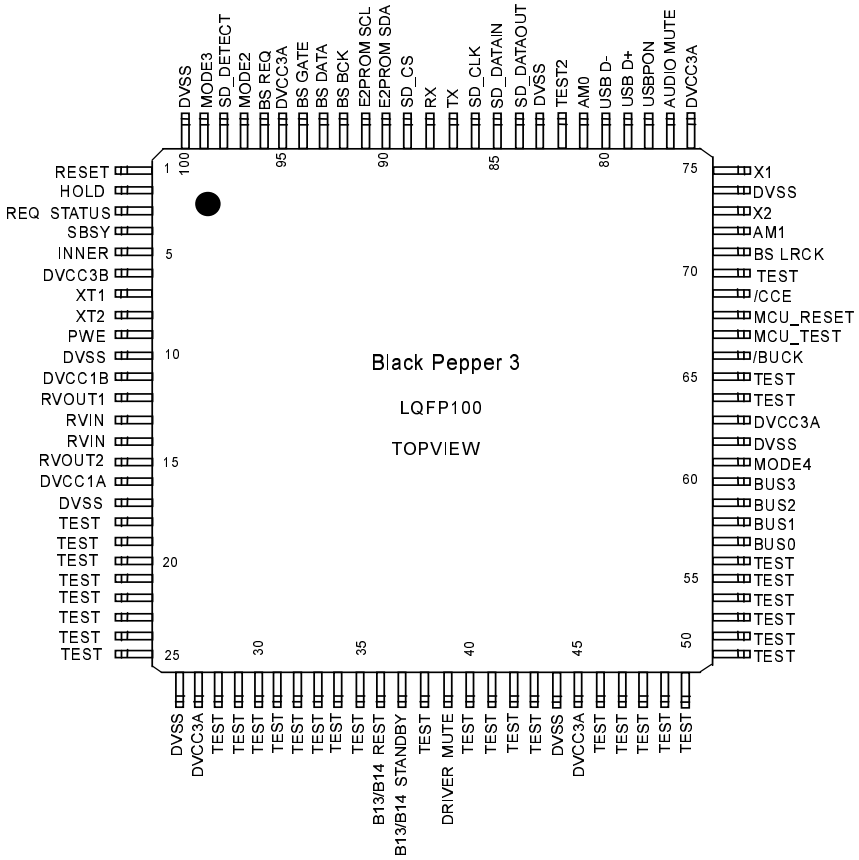
  Shinwa CLC08(2x speed)

  CP2(2x speed)

4.2 System block diagram



4.3 BlackPepper3 pin layout



4.4 BlackPepper 3 pin assignment and description

#of pins	Pin name	Input/output	Function
1	RESET	-	Chip reset
2	HOLD	I	System standby in or standby out control
3	REQ STATUS	I	Request from B13/B14
4	SBSY	I	SBSY input from B13/B14
36	B13/B14 RESET	O	RESET to B13/B14
37	B13/B14 STANDBY	O	Standby control B13/B14
57~60	BUS0,1,2,3	I/O	Command bus with B13/B14
66	/BUCK	O	Command clock to B13/B14
69	/CCE	O	Command CCE to B13/B14
67	MCU TEST	I/O	Connect to MCU TEST pin for MCU upgrade
68	MCU RESET	I/O	Connect to MCU RESET pin for MCU upgrade
71	BS LRCK	O	BSIF
92	BS BCK	O	BSIF
93	BS DATA	O	BSIF
94	BS GATE	O	BSIF
96	BS REQ	I	BSIF
5	INNER	I	Pick-up inner switch
39	DRIVER MUTE	O	Output to driver
77	AUDIO MUTE	O	Audio mute output
78	USB PON	O	USB power control
79	USB D+	I/O	USB data bus
80	USB D-	I/O	USB data bus
84	SD DATA OUT	O	SD data bus(out)
85	SD DATA IN	I	SD data bus(in)
86	SD CLK	O	SD data bus(clock)
89	SD CS	O	SD CS signal
98	SD DETECT	I	SD detect signal
87	TX	O	TX
88	RX	I	RX
90	E2PROM SDA	I/O	SDA, connect to E2PROM
91	E2PROM SCL	O	SCL, connect to E2PROM
7,8	XT1,XT2	-	32KHZ OSC connect
73,75	X1,X2	-	9MHZ OSC connect
9	PWE	O	Power control in standby mode
10,17,26,44,627 4,83,100	DVSS	-	Ground

6	DVCC3B	-	Power supply(3.3V)
27,45,63,76,95	DVCC3A	-	Power supply(3.3V)
11	DVCC1B	-	Power supply(1.5V)
16	DVCC1A	-	Power supply(1.5V)
12,15	RVOUT1,RVOUT2	O	1.5V output from Internal Regulator
13,14	RVIN	I	Power supply pin for Internal Regulator
18~25,28~35 38,40~43,46~56 ,64~65,70	TEST	O	Connect to ground or open
82	TEST2	I	Connect to ground
97	MODE2	I	Software mode(refer to notes)
99	MODE3	I	Software mode(refer to notes)
61	MODE4	I	Software mode(refer to notes)
72	AM1	I	Hardware mode(refer to notes)
81	AM0	I	Hardware mode(need to be pull-up) (refer to notes)

NOTES:

AM0

"1" fixed

AM1

"1": run program in internal rom

"0": run program in external flash

MODE2

"1": enable external flash and disable E2PROM function. Need connection with a 4Mbit flash.

"0": disable external flash and enable E2PROM function

MODE3

"1": disable the SD function,

"0": enable the SD function

MODE4

"1": B14(TC94B14MFG-202) connection

"0": B13(TC94B13FG-002) connection

5 Communication and command

5.1 Communication protocol

BlackPepper3 communicates with HOST MCU by the UART interface(pin 87, 88). Bellow is UART feature:

Baudrate	19200 kbps
Data width	8 bit
Stop bit	Yes
Parity bit	None

BlackPepper3 receving and transmitting command by a packet. Bellow is packet fomat:

Byte number	Value	Comment
0x00	0xFF	Sync byte
0x01	XX	Command length
0x02	XX	Command ID
0x03	XX	Command data
…	XX	Command data
Last byte	NN	Checksum

Command length = length from byte of command ID to last byte of command data.

Checksum = Sum of value from byte of command length to last byte of command data.

If there is no command data, command length = 1, and Checksum = command ID + command length.

5.2 Command list

PARTI: Command list send from host MCU to BlackPepper3:

command name	sync	length	value	data	checksum	description	note
MSF_PLAY	0xff	4	0x00	DATA	0xNN	start msf play	C1
SEL_FOLDER1	0xff	4	0x05	DATA	0xNN	select folder with folder analyze, to get folder inside information and foldre name	C2
SEL_FOLDER2	0xff	4	0x05	DATA	0xNN	select folder without folder analyze, to get folder inside information	c1
SEL_FILE1	0xff	3	0x06	DATA	0xNN	select file to get file name	c2
SEL_FILE2	0xff	3	0x07	DATA	0xNN	select file to get folder inside information	c1
EJECT	0xff	1	0x10	none	0xNN	eject disc(cd mode only)	-
READ_DEVICE	0xff	2	0x12	DATA	0xNN	start read process	-
PLAY	0xff	4	0x14	DATA	0xNN	start play	c1
STOP	0xff	2	0x18	DATA	0xNN	start stop	-
PAUSE	0xff	1	0x19	none	0xNN	start pause	c3
PAUSE_RELEASE	0xff	1	0x1a	none	0xNN	release pause	c3
FF	0xff	2	0x1b	DATA	0xNN	start FF play	c3
FR	0xff	2	0x1c	DATA	0xNN	start FR play	c3
FF/FR_RELEASE	0xff	1	0x1d	none	0xNN	release FF or FR play	c3
BOOKMARK_SET	0xff	2	0x1e	0x00	0xNN	set bookmark point	c3
BOOKMARK_CLEAR	0xff	2	0x1e	0x01	0xNN	clear bookmark point	c1
POSITION_PLAY	0xff	7	0x20	DATA	0xNN	set position and play	c1
SELECT_MODE	0xff	2	0x30	DATA	0xNN	select mode	-
TRACK_UP	0xff	1	0x31	none	0xNN	track up and play	c3
TRACK_DOWN	0xff	1	0x32	none	0xNN	track down and play	c3
DIR_UP	0xff	1	0x33	none	0xNN	folder up and play	c3
DIR_DOWN	0xff	1	0x34	none	0xNN	folder down and play	c3
MUTE	0xff	2	0x35	DATA	0xNN	mute on or mute off by mute pin	-
RESUME	0xff	1	0x36	none	0xNN	resume play after select mode	-
INTRO_MODE	0xff	2	0x38	DATA	0xNN	set intro mode	c1
REPEAT_MODE	0xff	2	0x39	DATA	0xNN	set repeat mode	c1
RANDOM_MODE	0xff	2	0x3a	DATA	0xNN	set random mode	c1
BOOKMARK_PLAY	0xff	1	0x3c	none	0xNN	play from bookmark point	c1
A-B_REPEAT	0xff	2	0x3f	DATA	0xNN	set or clear A-b repeat mode	c3
PICK-UP_SELECT	0xff	2	0x40	DATA	0xNN	select pick-up sequence number	c4
SEND_INIT_CMD	0xff	x	0x41	DATA	0xNN	send initial command of pick-up	c4
SEND_EQ_DATA	0xff	x	0x42	DATA	0xNN	send EQ data of pick-up	c4
SEND_RF_DATA	0xff	x	0x43	DATA	0xNN	send RF data of pick-up	c4

SEND_OK	0xff	1	0x44	none	0xNN	pick-up data send finish	c4
EXT_FLASH_UPGRADE	0xff	1	0x45	none	0xNN	upgrade external flash program	-
MCU_UPGRADE	0xff	2	0x46	DATA	0xNN	upgrade host mcu program	-
SYSTEM_ON_OFF	0xff	2	0x4f	DATA	0xNN	system on or system off	-
GET_INFO_TITLE(ID3)	0xff	2	0x80	0x00	0xNN	get id3 title information of mp3/wma file	c3
GET_INFO_ARTIST(ID3)	0xff	2	0x80	0x01	0xNN	get id3 artist information of mp3/wma file	c3
GET_INFO_ALBUM(ID3)	0xff	2	0x80	0x02	0xNN	get id3 album information of mp3/wma file	c3
GET_INFO_FILE_NAME	0xff	2	0x80	0x03	0xNN	get file name of mp3/wma file	c3
GET_INFO_DIR_NAME	0xff	2	0x80	0x04	0xNN	get folder name of mp3/wma file	c3
GET_INFO_STREAM	0xff	2	0x80	0x05	0xNN	get stream information of mp3/wma file	c3
GET_CD-TEXT	0xff	3	0x81	DATA	0xNN	get cd-text information	c1
GET_CD_TRACK_INFO	0xff	2	0x82	DATA	0xNN	get cd track information	c1
SET_FIRMWARE	0xff	2	0x83	DATA	0xNN	set firmware feature	-
GET_FIRM_VERSION	0xff	2	0x80	0x07	0xNN	get firmware version	-

Note:

c1: valid when read process is finished and device is play available.

c2: valid when read process is finished, device is play available, and current state is stop.

c3: valid in just play state(include play,pause,FF,FR)

c4: valid just after BP2 request pick-up selection

About DATA details please refer to 5.3 PART I.

PARTII: Command list send from BlackPepper3 to host MCU:

command name	sync	length	value	data	checksum	function description	note
MODE_SEL_OK	0xff	1	0x80	none	0xNN	ack to select mode command	
DEVICE_TYPE	0xff	2	0x82	DATA	0xNN	device type information	
ERROR_CODE	0xff	2	0x83	DATA	0xNN	toc error, play error information	
ERROR_CODE(UPGRADE)	0xff	2	0x83	DATA	0xNN	upgrade error information	
PLAY_STATUS	0xff	2	0x84	DATA	0xNN	play status	
COMMAND_FAIL	0xff	1	0x8b	none	0xNN	current command can not be accpeted.	
MUTE_STATUS	0xff	2	0x8c	DATA	0xNN	sound mute on or off status. ack to mute on/off command	
SYS_ON_OFF_STATUS	0xff	2	0x8d	DATA	0xNN	syste on or off status. ack to system on/off command	
EX_FLASH_UPGRADE_OK	0xff	1	0x8e	none	0xNN	external flash upgrade is finished and no problem.	
CD_TOC_INFO	0xff	5	0x90	DATA	0xNN	first track, final track, total time information of CDDA/MIXCD disc	
TTL_FILE_DIR_NUMBER	0xff	5	0x94	DATA	0xNN	total file number, total folder number of MIXCD,CDROM,USB,SD,MTP…	
PLAY_STREAM_INFO	0xff	4	0x97	DATA	0xNN	bitrate information, sample frequency information	
PLAY_FILE_TYPE	0xff	2	0x99	DATA	0xNN	file type(mp3,wma,cdda track…)	
STREAM_UNKNOW	0xff	1	0x9b	none	0xNN	stream info is unknow. ack to stream request command	
ID3_BUSY	0xff	1	0x9b	none	0xNN	id3 analyze is busy. ack to id3 request command	
PLAY_TO_END	0xff	1	0x9e	none	0xNN	all songs playing is finished.	
PLAY_CD_TRACK_INDEX	0xff	2	0x9f	DATA	0xNN	index number of CDDA track	
PLAY_FILE_DIR_NUMBER	0xff	9	0xa0	DATA	0xNN	play file number, play folder number, folder inside information	
PLAY_TIME	0xff	4	0xa2	DATA	0xNN	playing time	
PLAY_FILE_NAME	0xff	length+2	0xaa	DATA	0xNN	file name of playing file	
PLAY_DIR_NAME	0xff	length+2	0xab	DATA	0xNN	folder name of playing folder	
PLAY_ID3_INFO	0xff	length+3	0xac	DATA	0xNN	id3 information of playing file	
MSF_PLAY_NG	0xff	2	0xb3	0x01	0xNN	msf play is ng	
RESUME_CHK_STATUS	0xff	2	0xb4	DATA	0xNN	resume check result is ok or ng	
RESET(POWER)	0xff	2	0xb5	0x00	0xNN	system reset out(power on reset)	
RESET(STANDBY)	0xff	2	0xb5	0x01	0xNN	system reset out(from standby out)	
PICK-UP_REQUEST	0xff	1	0xb6	none	0xNN	request host side select pick-up or send pick-up coefficient data	
REPEAT_MODE	0xff	2	0xb7	DATA	0xNN	repeat mode	*1
INTRO_MODE	0xff	2	0xb8	DATA	0xNN	intro mode	*1

RANDOM_MODE	0xff	2	0xb9	DATA	0xNN	random mode	*1
ID3_NONE	0xff	1	0xbb	none	0xNN	there is no id3 information. ack to id3 request command	
CD-TEXT_RESULT	0xff	3	0xbc	DATA	0xNN	cd-text information found or not	
CD-TEXT_INFO	0xff	length+3	0xbd	DATA	0xNN	cd-text title or artist information	
A-B_REPEAT_STATUS	0xff	2	0xbf	DATA	0xNN	A-B repeat status	
FILE_NAME(SELECTED)	0xff	length+2	0xc0	DATA	0xNN	file name of selected file, ack to 0x06(select file1) command	
DIR_NAME(SELECTED)	0xff	length+2	0xc1	DATA	0xNN	folder name of selected folder	
DIR_INSIDE_INFO	0xff	5	0xc2	DATA	0xNN	inside info of selected folder	
DIR_INFO_OF_FILE	0xff	7	0xc3	DATA	0xNN	folder info of selected file, ack to 0x07(select file2) command	
SELECT_WRONG	0xff	2	0xc6	DATA	0xNN	select file or folder number is wrong	
PLAY_CD_TRACK_ATIME	0xff	3	0xd0	DATA	0xNN	A-time of CDDA track	
PLAY_SONG_TOTAL_TIME	0xff	4	0xd2	DATA	0xNN	mp3/wma file total time, or total msf time of CDD track	
CD_TRACK_INFO	0xff	7	0xd5	DATA	0xNN	track start msf time, total msf time	
BOOKMARK_STATUS	0xff	2	0xde	DATA	0xNN	bookmark set ok or ng	*2
BOOKMARK_PLAY_STATUS	0xff	2	0xdf	DATA	0xNN	bookmark play ok or ng	
USB/SD_DET_STATUS	0xff	2	0xe0	DATA	0xNN	USB and SD card detecting status	
PLAY_POSITION	0xff	7	0xea	DATA	0xNN	play position.	
FIRMWARE_VERSION	0xff	3	0xf7	DATA	0xNN	firmware version information	
FIRMWARE_FEATURE	0xff	3	0xf7	DATA	0xNN	return firmware feature parameter. ack to 0x83 command	
DISC_BRAKE_ERR	0xff	1	0xfa	none	0xNN		

Note:

*1: if status changed from play to any other, the setting will be cleared. And read, stop command also can clear the setting.

*2: read command can clear bookmark setting.

About DATA details please refer to 5.3 PART II.

5.3 Command data field detals

PARTI:

MSF_PLAY(0x00)	byte 0	MSF play minute setting
	byte 1	MSF play second setting
	byte 2	MSF play frame setting

SEL_FOLDER1(0x05)	byte 0	folder number(high byte)
	byte 1	folder number(low byte)
	byte 2	0x00(need analyze folder and get folder name)

SEL_FOLDER2(0x05)	byte 0	folder number(high byte)
	byte 1	folder number(low byte)
	byte 2	0x01(don't need analyze folder,don't get folder name)

SEL_FILE1(0x06)	byte 0	relative file number in selected folder(high byte)
	byte 1	relative file number in selected folder(low byte)

SEL_FILE2(0x07)	byte 0	file number(high byte)
	byte 1	file number(low byte)

READ_DEVICE(0x12)	byte 0	0x00: read and stop after read process. 0x01: read an play after read process. 0x80: TOC read, CD-TEXT read, and stop after read(CD only). 0x81: TOC read, CD-TEXT read, and play after read(CD only).

PLAY(0x14)	byte 0	0x01: play by file number 0x02: play by folder number
	byte 1	file number or folder number(high byte)
	byte 2	file number or folder number(low byte)

STOP(0x18)	byte 0	For USB or SD mode, this command just issue a stop operation and ignore this byte value. For CD mode, this byte value define the pick-up moving after stop. 0x00: stop. If it is CD mode, move pick-up to inner side after stop. 0x01: stop. If it is CD mode, keep pick-up position after stop.

FF(0x1b)	byte 0	0x00: start FF at normal speed 0x01: start FF at high speed 0x80: start FF at normal speed(mute pin output H)

		0x81: start FF at high speed(mute pin output H)

FR(0x1c)	byte 0	0x00: start FR at normal speed 0x01: start FR at high speed 0x80: start FR at normal speed(mute pin control) 0x81: start FR at high speed(mute pin control)

POSITION_PLAY(0x20)	byte 0	position parameter 1
	byte 1	position parameter 2
	byte 2	position parameter 3
	byte 3	position parameter 4
	byte 4	position parameter 5
	byte 5	position parameter 6

SELECT_MODE(0x30)	byte 0	0x01: select CD mode 0x02: select USB mode 0x03: select SD mode

MUTE(0x35)	byte 0	0x00: mute on(mute pin control) 0x01: mute off(mute pin control)

INTRO_MODE(0x38)	byte 0	0x00: intro on 0x01: intro off

REPEAT_MODE(0x39)	byte 0	0x00: repeat off 0x01: repeat 1 0x02: repeat dir 0x03: repeat all

RANDOM_MODE(0x3a)	byte 0	0x00: random on 0x01: random track(iPod only) 0x02: random album(iPod only) 0x03: cancel random mode

A-B_REPEAT(0x3f)	byte 0	0x00: cancel A-B repeat 0x01: set start point 0x02: set end point

PICK-UP_SELECT(0x040)	byte 0	

0: Sanyo DA11(1x)	1: Sanyo DA23(1x)	2: SamsungB55(1x)	3: default
4: default	5: Sanyo DA11(2x)	6: Sanyo DA23(2x)	7: SamsungB55(2x)
8: Tanashin 2007(2x)	9: Shinny IS68(2x)	10: CP2(2x)	11: Shinwa CLC01(2x)
12 ShinwaCLC08(2x)	13: TN2002	14: default	15: default
16~254: reserved			
255: read coefficient data from E2PROM			

SEND_INIT_CMD(0x41)	byte 0	1st byte of initial command
	byte 1	2nd byte of initial command
	byte 2	3rd byte of initial command
	…	
	byte n	

SEND_EQ_DATA(0x42)	byte 0	1st byte of EQ data
	byte 1	2nd byte of EQ data
	byte 2	3rd byte of EQ data
	…	
	byte n	

SEND_RF_DATA(0x43)	byte 0	1st byte of RF data
	byte 1	2nd byte of RF data
	byte 2	3rd byte of RF data
	…	
	byte n	

MCU_UPGRADE(0x46)	byte 0	MCU sequence number 0:Redchili 1:TMP91FW27 2:TMP91FY42 3:TMP91FW60 4:TMP91FU62

SYSTEM_ON_OFF(0x4f)	byte 0	0x00: system off 0x01: system on

GET_CD-TEXT(0x81)	byte 0	0x00: get title content 0x01: get artist content
	byte 1	track number

GET_CD_TRACK_INFO(0x82)	byte 0	track number

SET_FIRMWARE(0x83)	byte 0	feature parameter(default is 0000_0000b) 0000_0001b:USB/SD reading method setting. set 0: search folder by directory path. set 1: search folder by parent/child.(recommend) 0000_0010b: CD-ROM reading method setting set 0: path table sort order(CD-ROM) set 1: parent/child sort order(CD-ROM) 0000_0100b:SPDIF setting set 0:don't output SPDIF set 1:output SPDIF 0000_1000b:use PRAM from E2PROM set 0:use internal PRAM set 1:use PRAM from E2PROM 0001_0000b:enable or disable read iPod as MSC device set 0:don't read iPod as MSC device set 1:read iPod as MSC device

PARTII:

DEVICE_TYPE(0x82)	byte 0	0x01: mixed disc, 0x02: CDDA, 0x03: CD-ROM 0x04: SD card, 0x05: USB device(MSC) 0x06: USB device(MTP,partial device), 0x07: USB device(iPod) 0x16: USB device(MTP,not partial device) Note: for MTP partial device, FF/FR/bookmark/AB repeat/resume play/set position and play are supported.

ERROR_CODE(0x83)	byte 0	0x00: no disc, 0x01: disc toc read error, 0x02: disc not support 0x03: disc play error, 0x04: no definition 0x05: no SD card insert, 0x06: SD card read error 0x07: no USB device insert, 0x08: USB read error 0x09: no mp3/wma file in SD card 0x0a: no mp3/wma file in USB device(MSC) 0x0b: no mp3/wma file in USB device(MTP) 0x0c: no mp3/wma file in USB device(iPod)

ERROR_CODE(UPGRADE)(0x83)	byte 0	0x30: USB is not ready(external flash upgrade, mcu upgrade) 0x31: h16/s24 file open failed(external flash upgrade, mcu upgrade) 0x32: h16/s24 file format error(external flash upgrade only) 0x33: flash write error(external flash upgrade only)

PLAY_STATUS(0x84)	byte 0	0x00: play mode 0x01: stop mode 0x02: pause mode 0x03: pause mode is released 0x04~0x07: FF mode 0x04: FF(normal speed) 0x05: FF(high speed) 0x06: FF(normal speed, mute on control) 0x07: FF(high speed, mute on control) 0x08~0x0b: FR mode 0x08: FR(normal speed) 0x09: FR(high speed) 0x0a: FR(normal speed, mute on control) 0x0b: FR(high speed, mute on control) 0x0c: FF/FR mode is released

MUTE_STATUS(0x8c)	byte 0	0x00: mute on 0x01: mute off

SYS_ON_OFF_STATUS(0x8d)	byte 0	0x00: system is off 0x01: system is on

CD_TOC_INFO(0x90)	byte 0	first track number of CD
	byte 1	final track number of CD
	byte 2	disc all time(minute) of CD

	byte 3	disc all time(second) of CD

TTL_FILE_DIR_NUMBER(0x94)	byte 0	USB/SD/CD-ROM/mixed disc total folder number(high byte)
	byte 1	USB/SD/CD-ROM/mixed disc total folder number(low byte)
	byte 2	USB/SD/CD-ROM/mixed disc total file number(high byte)
	byte 3	USB/SD/CD-ROM/mixed disc total file number(low byte)

PLAY_STREAM_INFO(0x97)	byte 0	mp3: it is mpeg version value wma: it is bitrate(high byte)
	byte 1	mp3: it is bitrate value wma: it is bitrate(low byte)
	byte 2	mp3/wma: it is sample frequency value.

PLAY_FILE_TYPE(0x99)	byte 0	0x01: mp3, 0x02: wma, 0x03: audio track, 0x04: data track

PLAY_CD_TRACK_INDEX(0x9f)	byte 0	track index number

PLAY_FILE_DIR_NUMBER(0xa0)	byte 0	playing file number(high byte)
	byte 1	playing file number(low byte)
	byte 2	playing folder number(high byte)
	byte 3	playing folder number(low byte)
	byte 4	local total file number in folder(high byte)
	byte 5	local total file number in folder(low byte)
	byte 6	local start file number in folder(high byte)
	byte 7	local start file number in folder(low byte)

PLAY_TIME(0xa2)	byte 0	playing time(minute)(high byte)
	byte 1	playing time(minute)(low byte)
	byte 2	playing time(second)

PLAY_FILE_NAME(0xaa)	byte 0	character coding type 0x00: ISO-8859-1 0x01: Unicode(USB/SD mode is UTF-16, CD mode is UTF-16BE)
	byte 1	file name(first byte)
	byte 2	file name
	…	
	byte n	file name(last byte)

PLAY_DIR_NAME(0xab)	byte 0	character coding type 0x00: ISO-8859-1 0x01: Unicode(USB/SD mode is UTF-16, CD mode is UTF-16BE)
	byte 1	folder name(first byte)
	byte 2	folder name
	…	
	byte n	folder name(last byte)

PLAY_ID3_INFO(0xac)	byte 0	0x00: title info 0x01: artist info 0x02: album info
	byte 1	(mp3 file) 0x00: ISO-8859-1 0x01: UTF-16 0x02: UTF-16BE 0x03: UTF-8 (wma file) 0x00: UTF-16
	byte 2	info data(first byte)
	byte 3	info data
	…	
	byte n	info data(last byte)

RESUME_CHK_STATUS(0xb4)	byte 0	0x00:resume check ok 0x01:resume check ng

RESET(0xb5)	byte 0	0x00:system reset is ok(power on reset) 0x01:system reset is ok(standby out reset)

REPEAT_MODE(0xb7)	byte 0	0x00: no repeat 0x01: repeat 1 0x02: repeat dir 0x03: repeat all

INTRO_MODE(0xb8)	byte 0	0x00: intro on 0x01: intro off

RANDOM_MODE(0xb9)	byte 0	0x00: random on mode 0x01: random track(iPod)(don't use) 0x02: random album(iPod)(don't use) 0x03: random off

CD-TEXT_RESULT(0xbc)	byte 0	0x00: CD-TEXT not found 0x01: CD-TEXT found
	byte 1	CD-TEXT character set code 0x00: ISO-8859-1(8bits) 0x01: ISO646, ASCII(7bits) 0x80: Shif JIS (Japanese character) 0x81: Korean character 0x82: Chinese character

CD-TEXT_INFO(0xbd)	byte 0	0x00: title, 0x01: artist
	byte 1	track number
	byte 2	info data(first byte)
	byte 3	info data
	…	
	byte n	info data(last byte)

A-B_REPEAT_STATUS(0xbf)	byte 0	0x00: A-B repeat is cancel 0x10: A-B repeat start point set OK 0x11: A-B repeat start point set NG 0x1F: Replay start 0x20: A-B repeat end point set OK 0x21: A-B repeat end point set NG

FILE_NAME(SELECTED)(0xc0)	byte 0	character coding type 0x00: ISO-8859-1 0x01: Unicode(USB/SD mode is UTF-16, CD mode is UTF-16BE)
	byte 1	select file name(first byte)
	byte 2	select file name
	…	
	byte n	select file name(last byte)

DIR_NAME(SELECTED)(0xc1)	byte 0	character coding type 0x00: ISO-8859-1 0x01: Unicode(USB/SD mode is UTF-16, CD mode is UTF-16BE)

	byte 1	select folder name(first byte)
	byte 2	select folder name
	…	
	byte n	select folder name(last byte)

DIR_INSIDE_INFO(0xc2)	byte 0	local total file number in selected folder(high byte)
	byte 1	local total file number in selected folder(low byte)
	byte 2	local start file number in selected folder(high byte)
	byte 3	local start file number in selected folder(low byte)

DIR_INFO_OF_FILE(0xc3)	byte 0	folder number of selected file(high byte)
	byte 1	folder number of selected file(low byte)
	byte 2	local total file number in this folder(high byte)
	byte 3	local total file number in this folder(low byte)
	byte 4	local start file number in this folder(high byte)
	byte 5	local start file number in this folder(low byte)

SELECT_WRONG(0xc6)	byte 0	0x00: file number is wrong 0x01: folder number is wrong

PLAY_CD_TRACK_ATIME(0xd0)	byte 0	A-time(minute)
	byte 1	A-time(second)

PLAY_SONG_TOTAL_TIME(0xd2)	byte 0	(mp3/wma): minute(high byte) (cd_track): minute
	byte 1	(mp3/wma): minute(low byte) (cd_track): second
	byte 2	(mp3/wma): second (cd_track): frame

CD_TRACK_INFO(0xd5)	byte 0	track type 0x00: audio track, 0x01: data track
	byte 1	track number
	byte 2	track start MSF(minute)
	byte 3	track start MSF(second)
	byte 4	track total time(minute)
	byte 5	track total time(second)

BOOKMARK_STATUS(0xde)	byte 0	0x00: bookmark set ok 0x01: bookmark set NG

BOOKMARK_PLAY_STATUS(0xdf)	byte 0	0x00: bookmark play ok 0x01: bookmark play NG

USB/SD_DET_STATUS(0xe0)	byte 0	0x02: SD card is removed 0x03: SD card is inserted 0x05: SD card detect ready 0x07: SD card detect error 0x10: USB bus is stoped 0x11: USB bus is initializing 0x12: USB device is removed 0x13: USB device is inserted 0x14: USB class is under checking 0x15: USB device detect ready 0x16: USB fatal error(need hardware reset) 0x17: USB detect error 0x18: USB class is not support 0x19: USB is not ready 0x1a: Limited USB device(if don't read iPod as MSC) other: reserved

PLAY_POSITION(0xea)	byte 0	position parameter 1
	byte 1	position parameter 2
	byte 2	position parameter 3
	byte 3	position parameter 4
	byte 4	position parameter 5
	byte 5	position parameter 6

FIRMWARE_VERSION(0xf7)	byte 0	0x01(firmware version case, this byte is fixed to 0x01)
	byte 1	version value

FIRMWARE_FEATURE(0xf7)	byte 0	0x00(firmware feature case, this byte is fixed to 0x00)
	byte 1	feature parameter

6 Function details

This chapter describes all of function about BlackPepper3.

6.1 Reset and select your pick-up

After system is reseted, BlackPepper3 will send PICK-UP_REQUEST command first. This command will be sent every 200ms until host side return PICK-UP_SELECT command. If host side doesn't want to use BlackPepper3 inside coefficient, he can send command(0x41,0x42,0x43,0x44) to start a coefficient transmission process. This process will be told you in 6.34. Anyway, BlackPepper3 will return a RESET(POWER)(0xB500) command eventually, so reset process is finished.

Relevant commands are listed bellow:

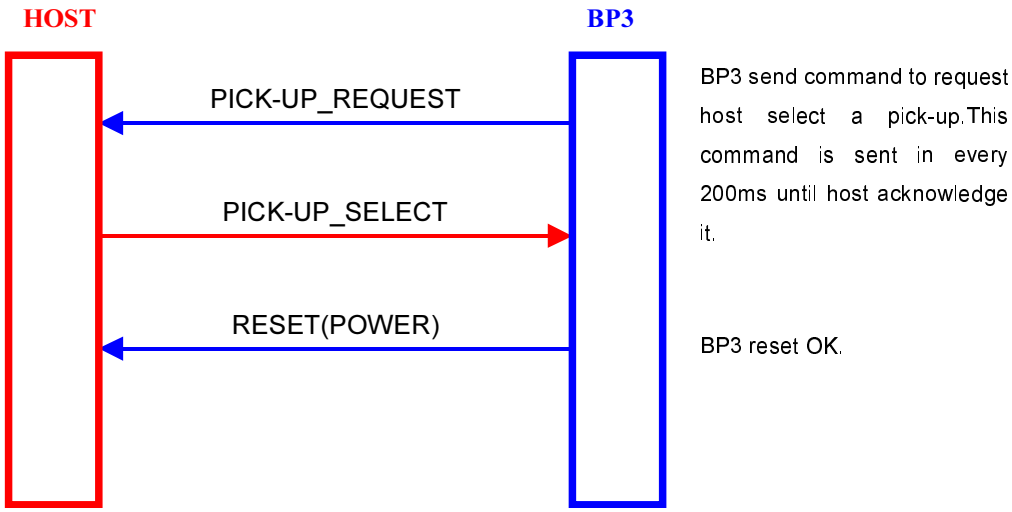
HOST->BlackPepper3

PICK-UP_SELECT(0x40)	This command is valid only when BP3 sent 0xb6 command.

BlackPepper3->HOST

RESET(POWER)(0xb5)	Byte0 of data filed = 0x00, in case of hardware reset.	It means BP3 finished his reset process.
PICK-UP_REQUEST(0xb6)	This is the first command after hardware reset. Use this command to synchronaize your system. This command will not be sent again after standby out.	

Command sequence



6.2 Get firmware version and set firmware feature

After reset ok, host can get firmware version and set firmware feature. This process can only be done before any reading process.

Relevant commands are listed bellow:

HOST->BlackPepper3

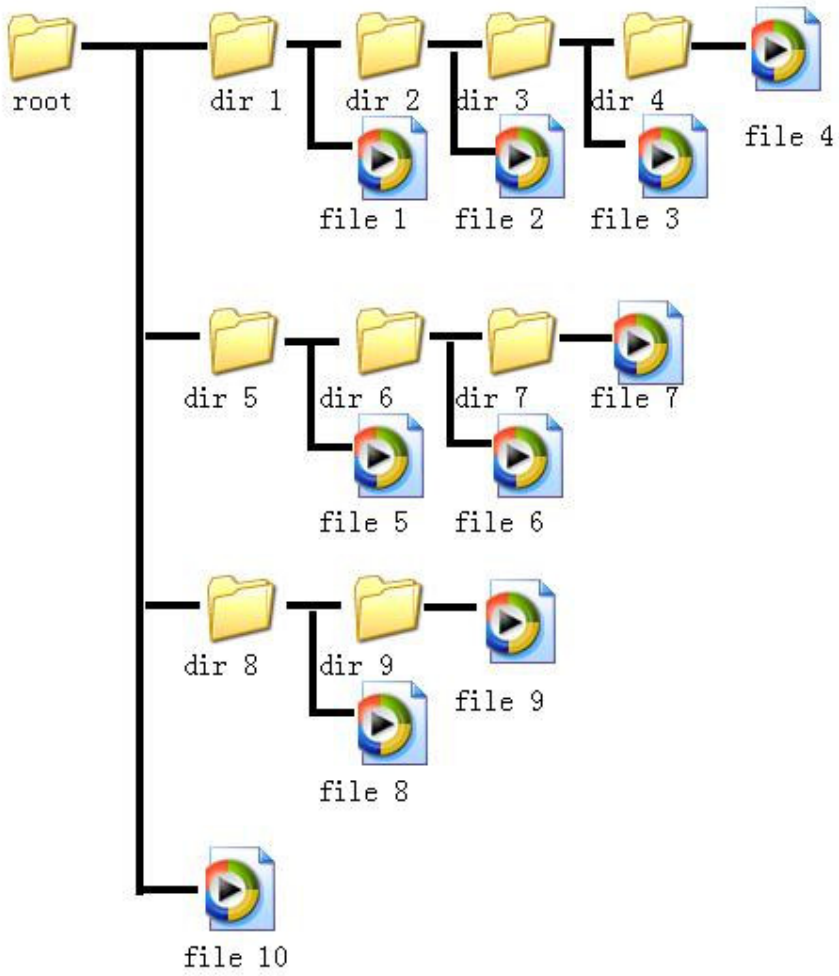
GET_FIRM_VERSION(0x8007)	byte0 of data field = 0x07.
SET_FIRMWARE(0x83)	Set firmware feature before starting reading process. Host side can check BP3 receiving is right or not by comparing with FIRMWARE_FEATURE command received.

BlackPepper3->HOST

FIRMWARE_VERSION(0xF701)	Byte0 of data field =0x01.
FIRMWARE_FEATURE(0xF700)	Byte0 of data field=0x00.

About USB/SD folder searching order, in command **SET_FIRMWARE(0x83),** there is 1 bit to select the searching order. About the explanation of searching order, refer to bellow example:

This is the original structure:



After BlackPepper3 reading, the folder number assigned refer to bellow table:

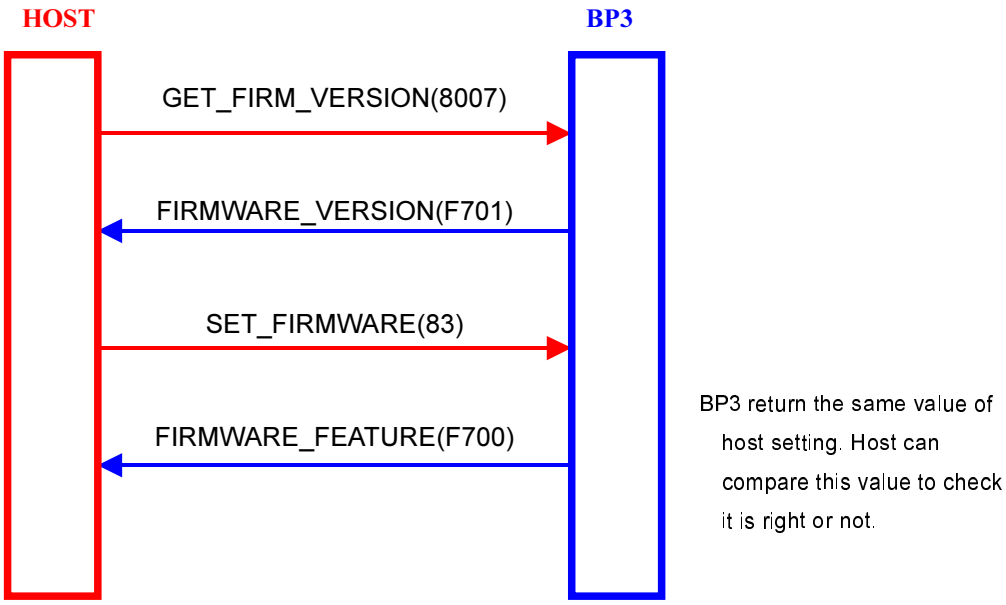
folder name	Assign folder number (Set bit to 0)	Assign folder number (Set bit to 1)
Root	Folder number 1	Folder number 1
Dir 1	Folder number 2	Folder number 2
Dir 2	Folder number 5	Folder number 3
Dir 3	Folder number 8	Folder number 4
Dir 4	Folder number 10	Folder number 5

Dir 5	Folder number 3	Folder number 6
Dir 6	Folder number 6	Folder number 7
Dir 7	Folder number 9	Folder number 8
Dir 8	Folder number 4	Folder number 9
Dir 9	Folder number 7	Folder number 10

Another point need to be clarified is that empty folder is also counted in driver layer if set bit to 0, but BlackPepper3 doesn't show you these folders. If set to 1, empty folder is excluded.

About CD-ROM directory sort, please refer to B13/B14 datasheet.

Command sequence



6.3 Detect USB device and SD card

BP3 etecting B evice an car realtime an return their status automaticall an separatel . fter reset B us start orking. hen B us is orking an event from B evice ill e return to host. But B us ill e stoppe if ou select or mo e. o B plug in or out event can not e etecte BP3 BP3 ust keet status at B us stop. please e note this point. But car status is kept etecting all along.

elevant comman s are liste ello

BlackPepper3 H

USB/SD_DET_STATUS(0xE0)	eturn B or status separatel .

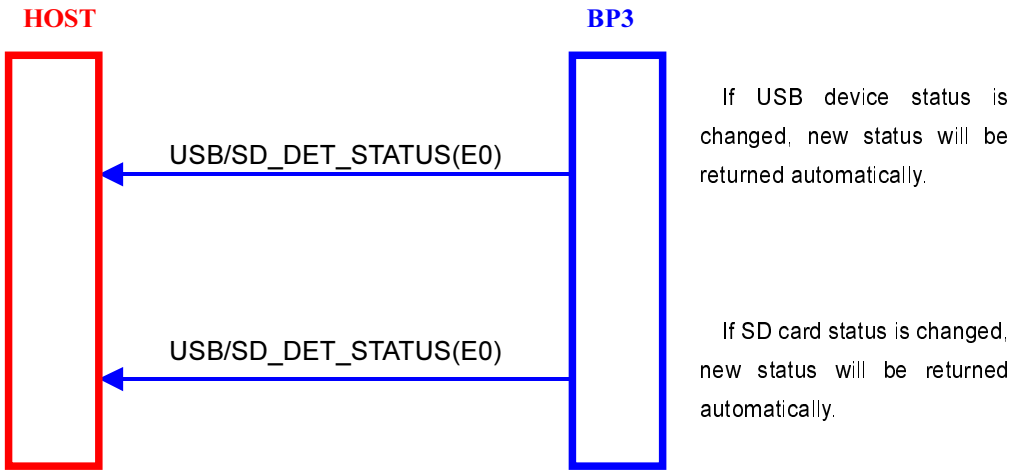
out B status meaning an its action is liste ello

Status code	**Explanation**	**Action**
	car is remove	ispla "no car "

3	car is inserte	ust keep aiting
	car is rea	tart rea process
	car etecting is error	ispla “car error“
	B us is stoppe	o nee o an action.
	B us start initiali ing	ust keep aiting
	B evice is remove	ispla “no B“
3	B evice is inserte	ust keep aiting
	B evice class t pe checking	ust keep aiting
	B evice is rea	tart rea process
	B river encounters fatal error or over current	Har are reset BlackPepper3
	B evice etecting is error	ispla “ B error“
	B class t pe is not e supporte	ispla “unkno n B“
	B memor is not rea . ccurs hen car is remove from car rea er.	ust keep aiting or ispla “no B“
a	t is iPo an can not e supporte .	ispla “not support“
others	o efinition	

ove ispla characters in action column is ust a e ample for reference.

omman se uence


HOST
BP3
USB/SD_DET_STATUS(E0)
USB/SD_DET_STATUS(E0)
If USB device status is changed, new status will be returned automatically.
If SD card status is changed, new status will be returned automatically.

6.4 Select a mode

Different with , host should select wor mode before reading rocess, because B need re are something before start reading.

elevant commands are listed bellow

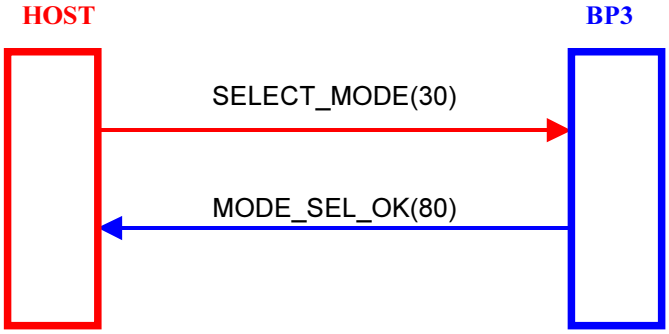
S Blac e er

SELECT_MODE(0x30)	Select a wor mode in D, USB or SD.

Blac e er S

MODE_SEL_OK(0x80)	he ac nowledgement for S D command.

ommand se uence



Select a mode before start reading in this mode.

6.5 Read USB/SD/CD(without CD-TEXT)

fter selecting a mode then start a reading rocess b send a command. has t o selection one is to set if start a to la one is to set if read . reading is st alid for mode b t host can send it in S or S mode. e ill disc ss reading later.

or a oid error and eas ing rogramming in host soft are it s better sending command after S or S is read stat s if start to read S or S . bo t S or S stat s refer to chat er . .

lease be noted that de ice has t o ind. ne is artial de ice one is b t not artial de ice. or b t not artial de ice nctions of boo mar re eat res me la osition la all are na ailable.

ele ant commands are listed bello

S lac e er

READ_DEVICE(0x12)	ere st disc ss first b te of data field or . means sto after read. means a to la from first song after read. and ha e reading re st disc ss it later.

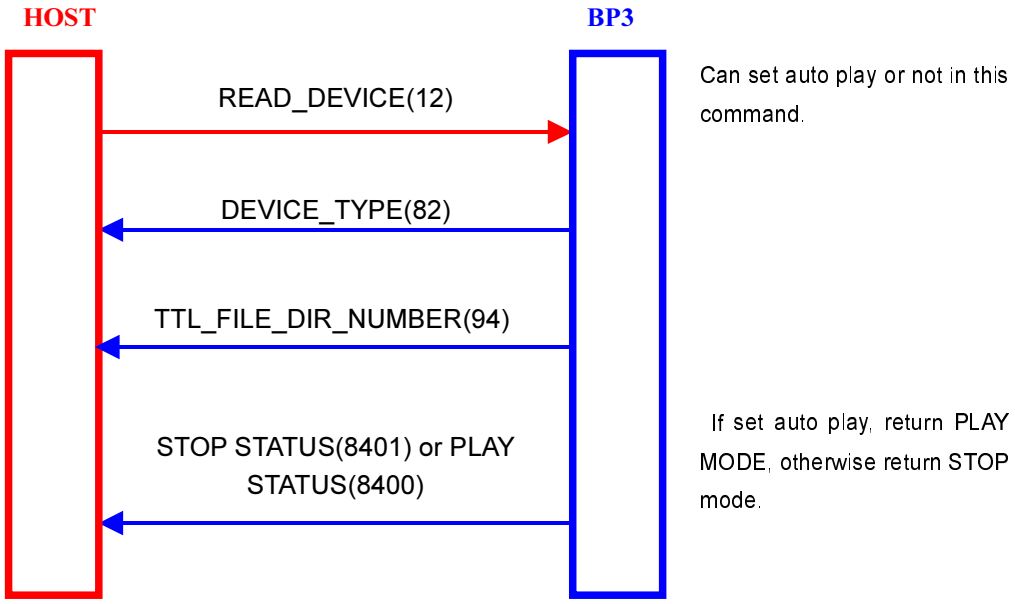
lac e er S

DEVICE_TYPE(0x82)	f de ice is la a ailable ret rn this command. etailed infomation lease refer to command cha ter.
ERROR_CODE(0x83)	f error occ r in reading rocess or de ice is la na ailable ret rn this command to re ort a error. bo t reading error b te of data field is in mode in S mode a b c in S mode. etailed infomation lease refer to command cha ter.
CD_TOC_INFO(0x90)	et rns first trac n mber final trac n mber and disc total time if it is disc.

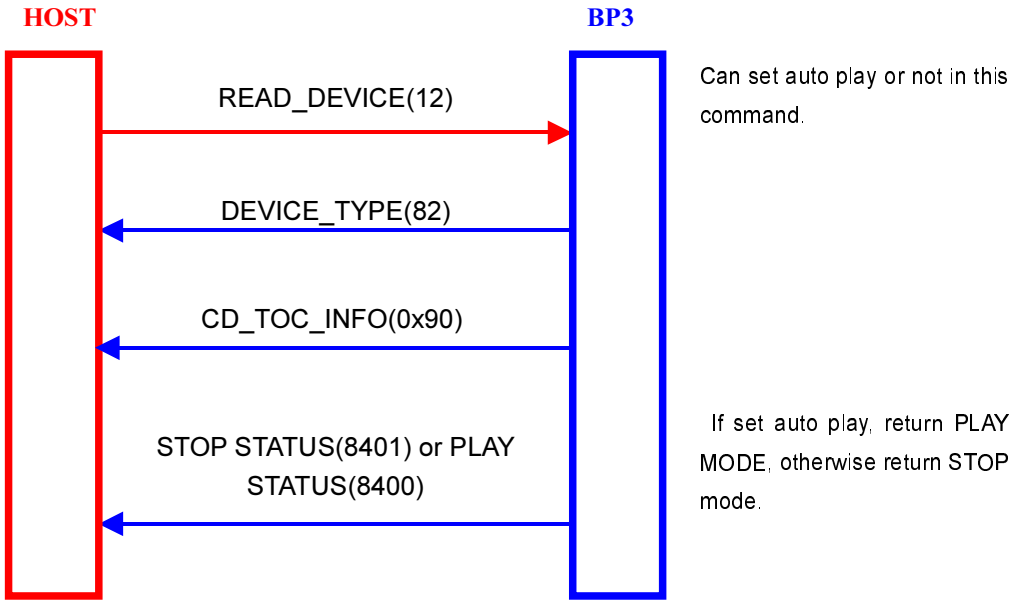
TTL_FILE_DIR_NUMBER(0x94)	et rns total file n mber total folder n mber fo nd in the de ice S S etc . or disc the total folder n mber is .
PLAY_STATUS(0x84) **STOP STATUS(0x8401)** **PLAY STATUS(0x8400)**	**STOP STATUS** te of data field . **PLAY STATUS** te of data field . f set a to la ith command **PLAY STATUS** command ret rns other ise **STOP STATUS** ret rns.

ommand se ence

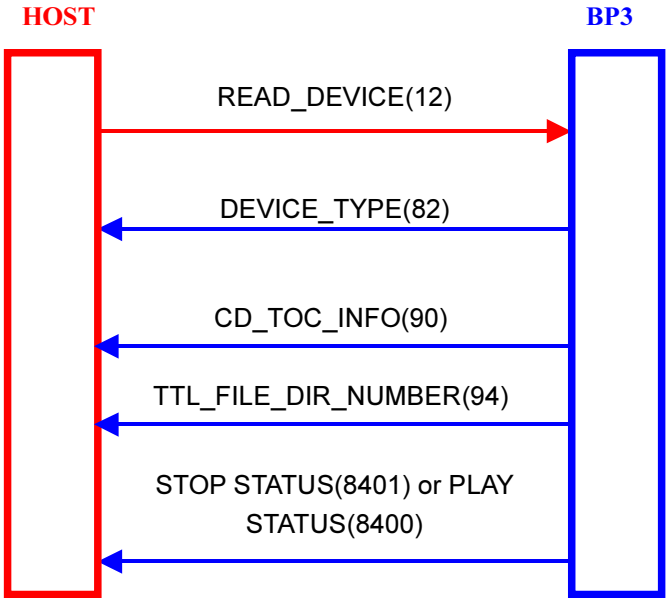
CD-ROM/USB/SD case:



CD-DA case



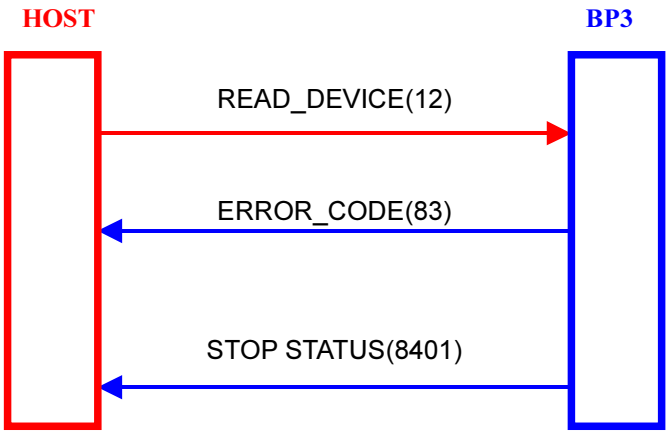
MIX-CD case:



Can set auto play or not in this command.

If set auto play, return PLAY MODE, otherwise return STOP mode.

ERROR case:



Can set auto play or not in this command.

In error case, STOP STATUS return.

6.6 Play/up/down/dir up/dir down/track number auto change

Command li e P A T AC UP T AC O I UP I O can cause P o into play process and P return a playin trac num er. hen playin , i current trac playin inished, P ill start ne t trac play. hich trac ne t to play, it s depend on repeat intro random settin . And i this is the last trac in repeat none mode, it ill o to stop mode, and return P A TO command. A out P A TO command and play status ill e disscuss later.

erytime play process is start to oin , the irst returned command must e P A I I U command, and then P A I T P command. So P A I I U can tell you a ne playin is started. In some occasion, the trac num er isn t chan e, ut ne playin is started, it is same. or e ample, in repeat mode, a ter this son is played, then P start to play this son a ain, P A I I U ill also e returned at playin e innin .

So P A I I U command is la that in orm host side last son playin inished and ne son playin ill e started.

ele ant commands are listed ello

OST lac Pepper

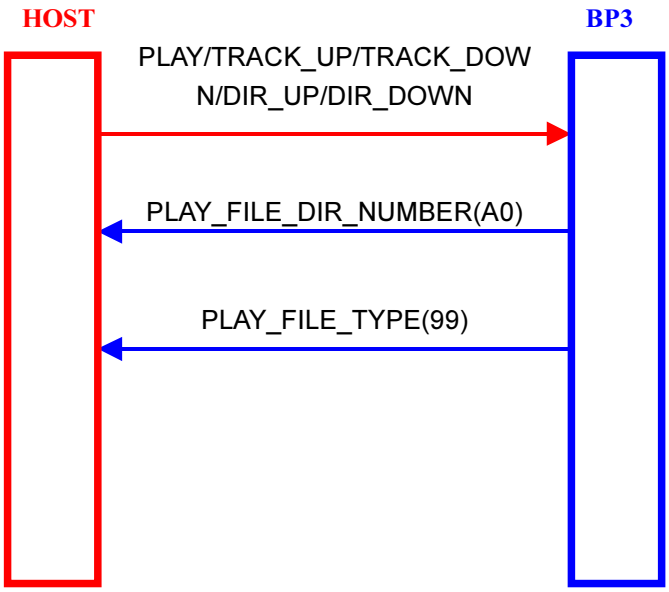
PLAY(0x14)	Play a ile y speci yin a num er. ost send this command in any status as lon as readin process is inished and de ice is play a aila le. The num er is the se uence in this de ice.
TRACK_UP(0x31)	Send this command in playin state play pause r
TRACK_DOWN(0x32)	Send this command in playin state play pause r
DIR_UP(0x33)	Send this command in playin state play pause r
DIR_DOWN(0x34)	Send this command in playin state play pause r

lac Pepper OST

PLAY_FILE_DIR_NUMBER(0xa0)	eturns this command, i P detects playin trac num er is chan ed.
PLAY_FILE_TYPE(0x99)	ery command ill e ollo ed a command , to tell host the type o current playin , P ile, A ile, audio trac , or other thin .

Command se uence

PLAY/TRACK_UP/TRACK_DOWN/DIR_UP/DIR_DOWN command case:

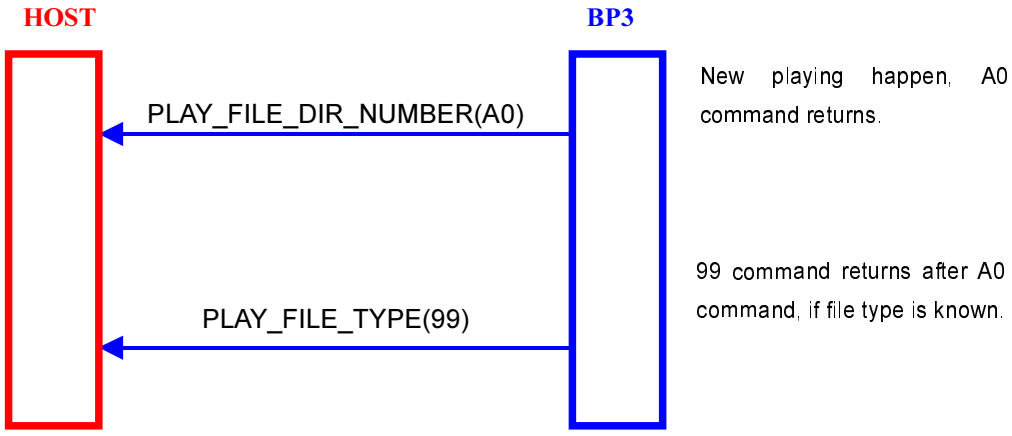


These command will issue a A0 command from BP3, even track number is the same, for example, in repeat 1 mode.

Every A0 command will be followed this command. A0 command return very quickly, even playing is not start genuinely. But 99 command is returned after the file/dir name is got, but before ID3 reading process

playing track number is auto changed case:

Please be noted that this case include that playing track number is no change, but begin another playing, for example in repeat 1 mode.



6.7 Get play information

The play information includes file name, folder name, ID3 info title/artist/album , bitrate info, sample frequency info, playing time, playing total time of song, play position used for resume play and some infomation only be available in auio track playing, like track index number, track playing Atime. The file name, folder, ID3 info, bitrate info, sample frequency info need a request command first, but others info can be return automatically, if BP3 thinks they are changed. These info are playing time, playing total time of song, play position, track index number, track playing Atime. ere discuss them.

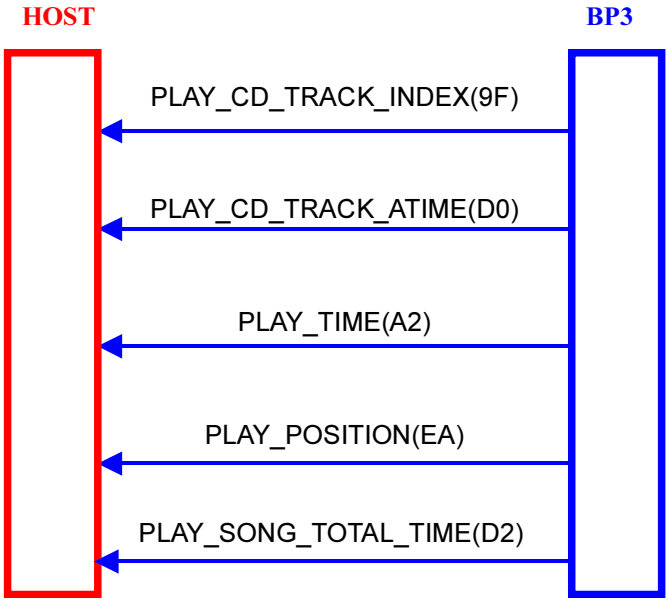
elevant commands are listed bellow

otes playing total time of song means the total time the song can be played, this info is not fixed for ever. ometimes, this information maybe change, so host need to check this info in playing status all along.

BlackPepper3 T

PLAY_CD_TRACK_INDEX(0x9f)	or track in D DA, I D only. If track number change, returns it.
PLAY_TIME(0xa2)	It is playing elapsed time. eturns it in every 1 second.
PLAY_CD_TRACK_ATIME(0xd0)	or track in D DA, I D only. It includes Aminute and Asecond. eturns it in every 1 second.
PLAY_SONG_TOTAL_TIME(0xd2)	It is total time of this file. eturns it if BP3 thinks this infomaition is changed. oted that track in D and the P3/ A file have different format in this command.
PLAY_POSITION(0xea)	This command returning goes along with P A TI E command. Every 1 second, returns it once. This command includes bytes parameters, save it. If BP3 is hardware reset, use these parameters to resume play from last position again.

ommand sequence



9F and D0 command is for track in D-DA or IX- D only.

6.8 Play/Pause/FF/FR playing status change

After playing is started, play/pause/FF/F change is available. se pertinent command to reali e these operation. After these command sent, BP3 playing status will be change quickly, but sometimes it need a moment.

For FF/F operation, there is a high speed or low speed selection. They are invalid for B or D device in fact. Even for mp3/wma file in D- , speed is changed only after current song playing is finished, the speed becomes effective at next song playing. But for audio track playing in D-DA or IX- D, it becomes effective any time. Please be careful this issue.

For FF/F operation, there is another selection about mute sound or –1 db outputing audio. But please be noted that, the sound mute is control by A DI TE pin. About A DI TE pin will be described later. If hos want this function, he need to connect this pin.

And please be noted that, F status can be release automatically in some case, like F to the first song header, F to song header in repeat 1 mode, etc.

About the status change, more detailed information is available later.

elevant commands are listed bellow

T- BlackPepper3

PAUSE(0x19)	tart pause
PAUSE_RELEASE(0x1a)	elease pause condition.
FF(0x1b)	tart FF playing
FR(0x1c)	tart F playing
FF/FR_RELEASE(0x1d)	elease FF or F condition.

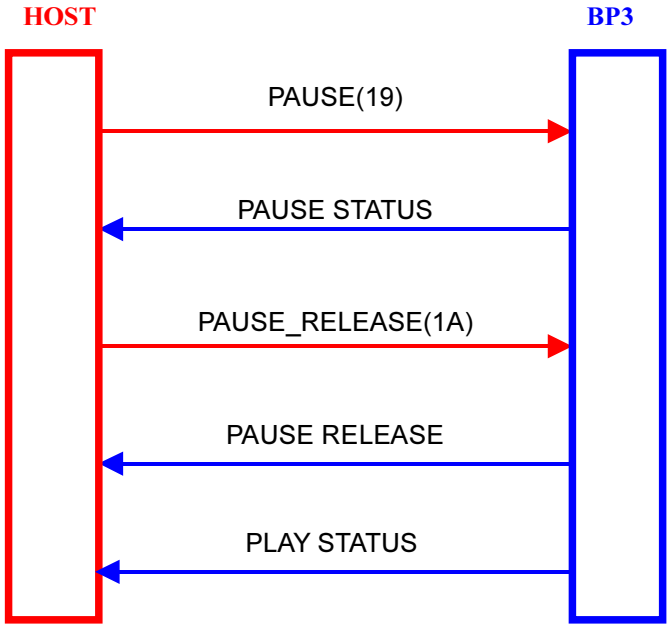
BlackPepper3- T

PLAY_STATUS(0x84)	0x00 **PLAY STATUS**; 0x01 **STOP STATUS**; 0x0 **PAUSE STATUS**; 0x03 **PAUSE RELEASE**; 0x0 0x0 **FF STATUS**; 0x0 0x0b **FR STATUS**; 0x0d **FF release** or **FR release**.

ommand sequence

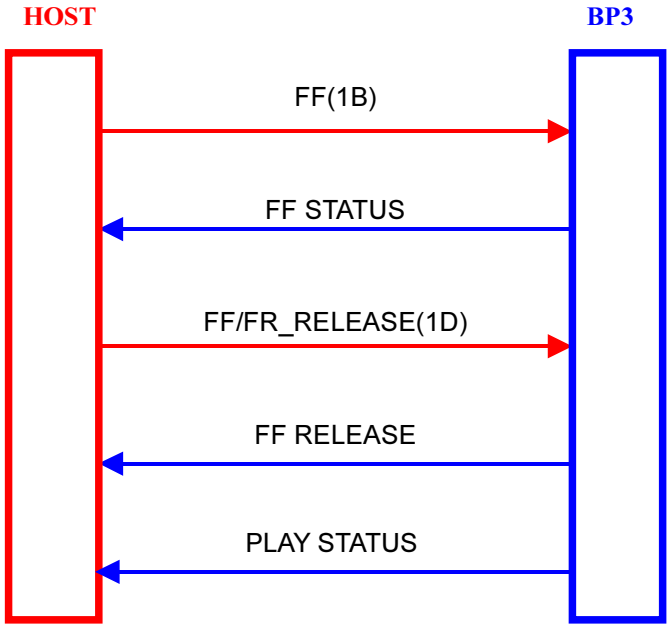
ase 1 play - pause - play

urrent is play status.



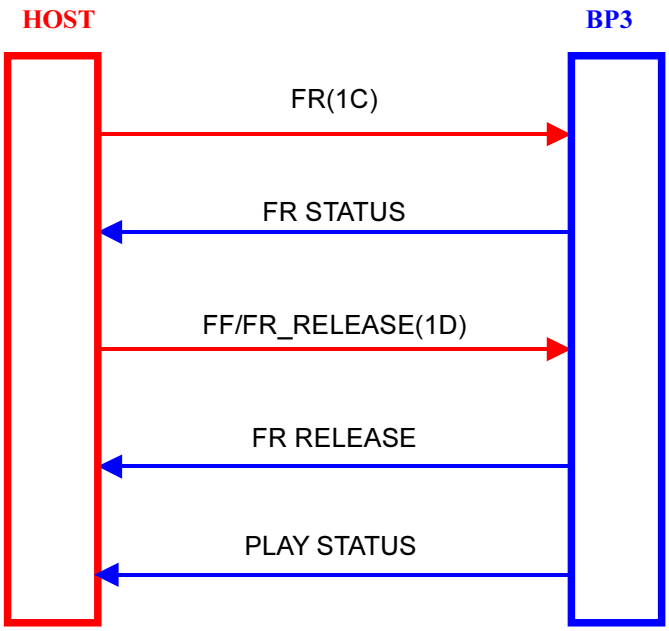
ase play - FF - play

urrent is play status.



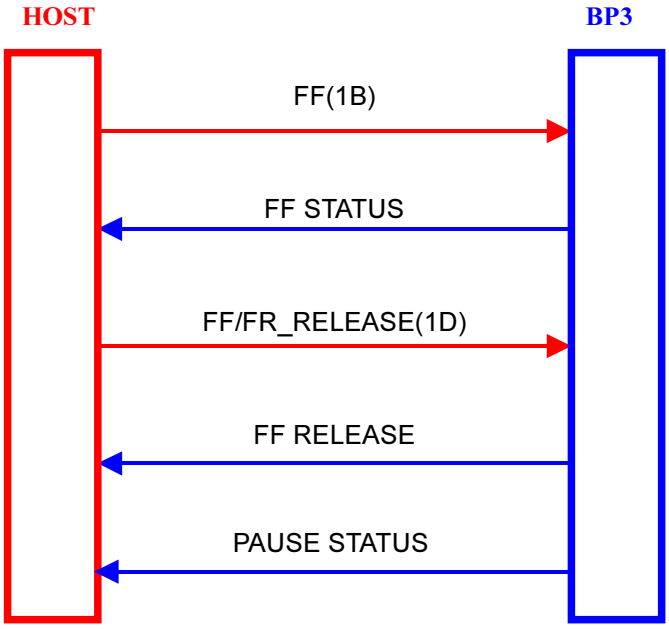
ase 3 play - F - play

urrent is play status.



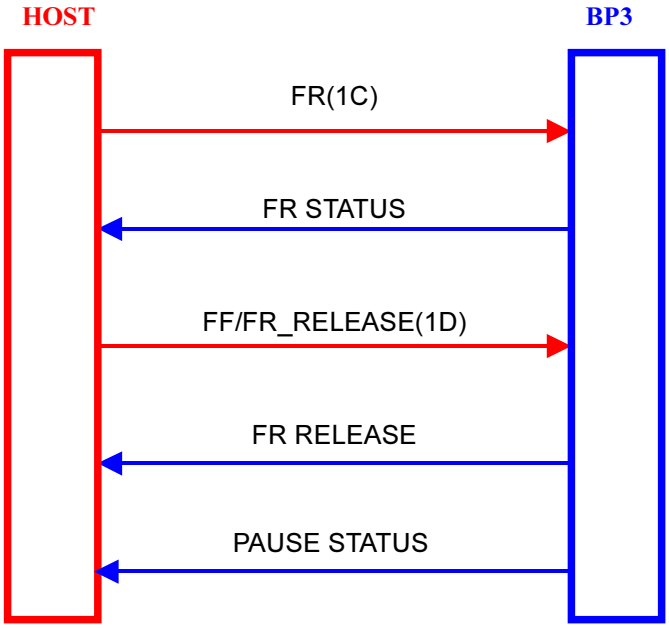
ase pause - FF - pause

urrent is pause status.



ase pause - F - pause

urrent is pause status.



6.9 Stop

In play/pause/FF/F status, send T P command, BP3 start stop process, and returns T P TAT finally. In D mode, pick-up moving inner or not can be specified.

elevant commands are listed bellow

T- BlackPepper3

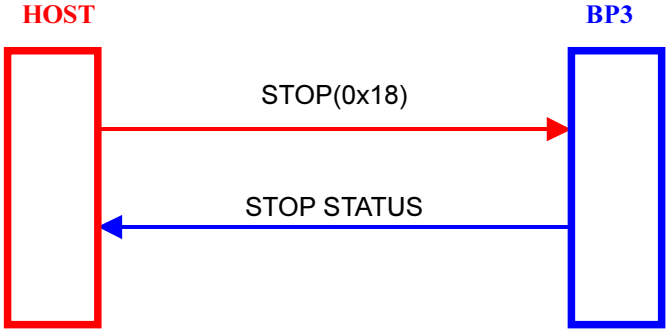
STOP(0x18)	There is one byte in data field indicate need pick-up move to inner or not. But this indication is invalid for B or D mode.

BlackPepper3- T

PLAY_STATUS(0x84)	0x00 **PLAY STATUS**; 0x01 **STOP STATUS**; 0x0 **PAUSE STATUS**; 0x03 **PAUSE RELEASE**; 0x0 0x0 **FF STATUS**; 0x0 0x0b **FR STATUS**; 0x0d **FF release** or **FR release**.

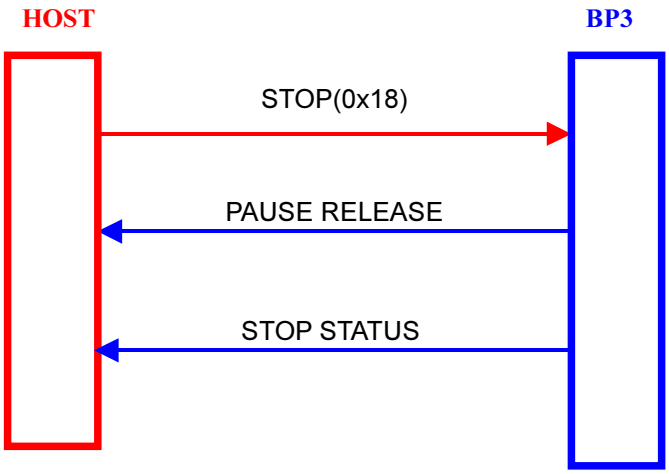
ommand sequence

Case 1: current is play status

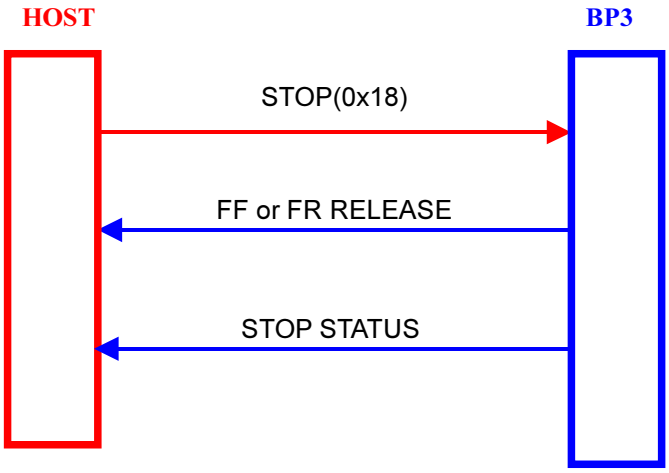


pecify pick-up inner moving or not if necessary.

Case 2: current is pause status



Case 3: current is FF or FR status



6.10 Play end

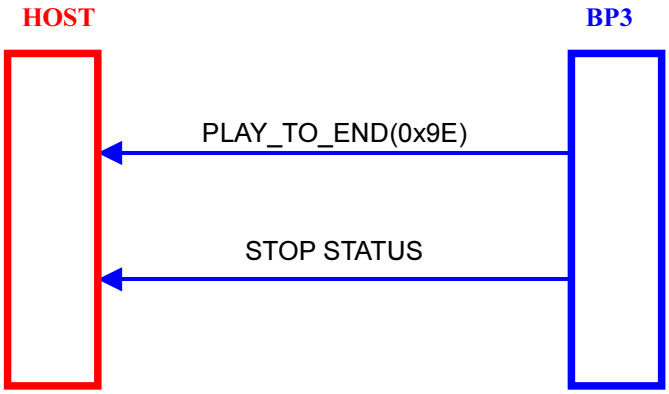
f aven t set any re eat mo e after a songs p aye start stop process. comman is return ust at t e einning of stop process.

e evant comman s are iste e o

ack epper - S

PLAY_TO_END(0x9E)	eans a songs p aying is finis e .
PLAY_STATUS(0x84)	**STOP STATUS**

omman se uence



6.11 About BlackPepper3 status

e o ta e escri es ack epper insi e state an event s ifting.

State / vent	Stop	ay	ause			pause	pause
STOP command	-	Stop	Stop	Stop	Stop	Stop	Stop
PLAY command	ay	ay	ause			pause	pause
PAUSE command	-	ause	-	pause	pause	-	-
PAUSE_RELEASE command		-	ay	-	-		
FF command	-		pause	-		-	pause
FR command	-		pause		-	pause	-
FF/FR_RELEASE command		-	-	ay	ay	ause	ause
Track up command	-	p ay	ause			pause	pause
Track down command	-	p ay	ause			pause	pause
Dir up command	-	p ay	ause			pause	pause
Dir down command	-	p ay	ause			pause	pause
Play to end or beginning	-	stop	-	Stop	ay	Stop	ause

f ack epper etects a ove status c anging an it matc es t e status or event in comman S S it returns ost ne status or event y t is comman . ese status or event in comman S S are state in e o ta e

omman	omman ata	Status represente
		S S
		S S S
		S S S
		S S
		S S
		S S
		re ease or re ease

6.12 Get File name

is paragrap escri es getting fi e name of current p aying. ack epper support up to ytes fi e name t at mean ma imum c aracters in fi e name. ut for isc in fact ma imum is ytes.

e evant comman s are iste e o

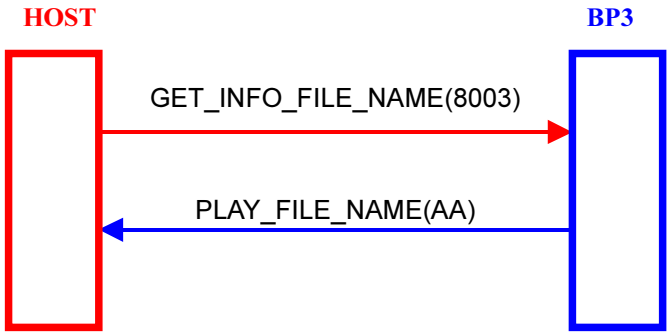
S - ack epper

GET_INFO_FILE_NAME(0x8003)	et fi e name of current p aying

ack epper - S

PLAY_FILE_NAME(0xaa)	irst yte of ata fie represent t e c aracter co ing. is S - - co ing is nico e co ing ic is - in S S mo e ut - in .

omman se uence



6.13 Get Folder name

is paragrap escri es getting fo er name ic current p aying fi e is ocate . ack epper support up to ytes in fo er name t at mean ma imum c aracters. ut for isc in fact ma imum is ytes.

e evant comman s are iste e o

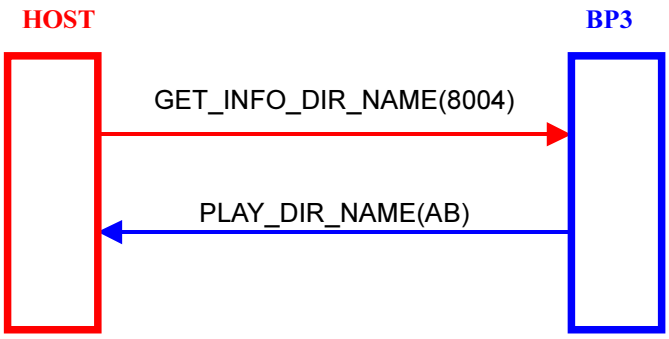
S - ack epper

GET_INFO_DIR_NAME(0x8004)	et fo er name of current p aying

ack epper - S

PLAY_DIR_NAME(0xab)	irst yte of ata fie represent t e c aracter co ing. is S - - co ing is nico e co ing ic is - in S S mo e ut - in .

omman se uence



6.14 Get ID3 information

is paragrap escri es getting information. ack epper supports feature as e o ta e

i e type	version	engt	o ing
	. v .	ytes	S - -
	. v . v .	ytes	so- - - - -
	information	ytes	-

ack epper co ing type an content y comman

e evant comman s are iste e o

S - ack epper

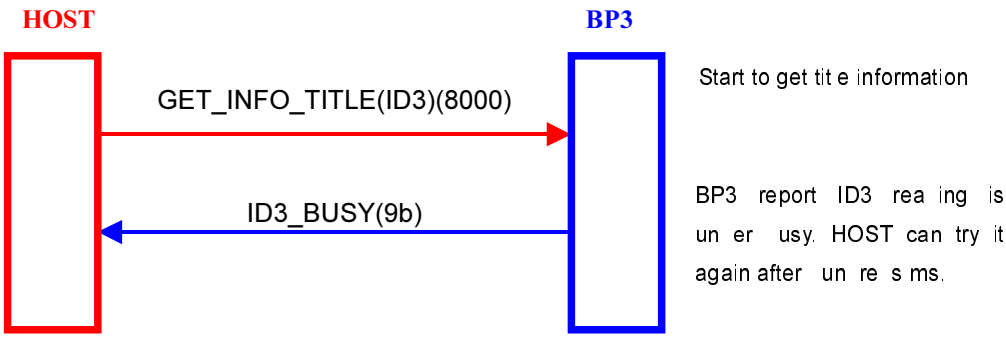
GET_INFO_TITLE(ID3)(0x8000)	e uest tit e informaiton.
GET_INFO_ARTIST(ID3)(0x8001)	e uest artist information.
GET_INFO_ALBUM(ID3)(0x8002)	e uest a um information.

ack epper - S

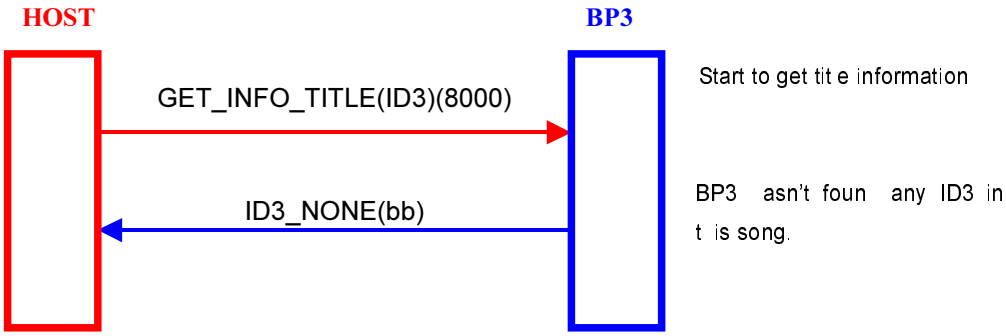
PLAY_ID3_INFO(0xac)	**ID3_TITLE_INFO(0xac00)**	t s tit e infomation
	ID3_ARTIST_INFO(0xac01)	t s artist information
	ID3_ALBUM_INFO(0xac02)	t s a um information
ID3_NONE(0xbb)		isn t foun
ID3_BUSY(0x9b)		rea ing is usy

omman se uence

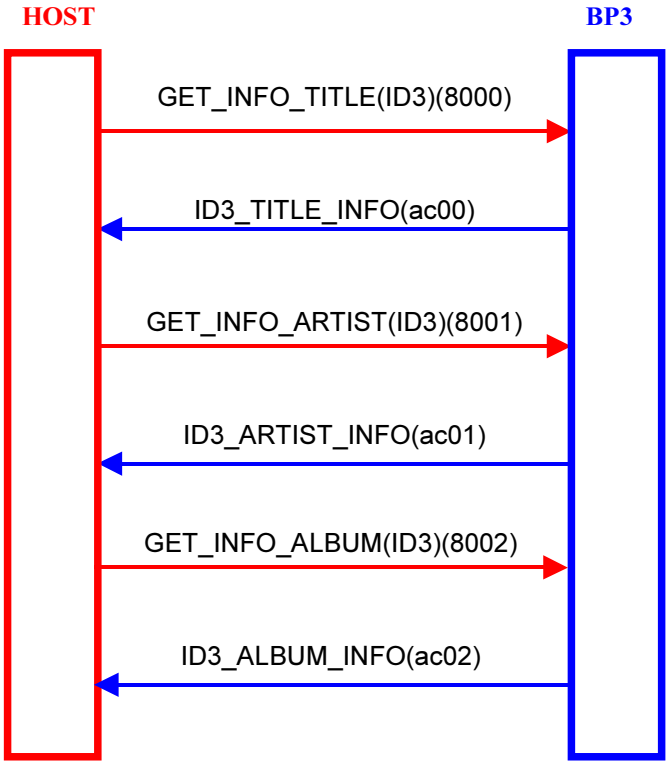
Case 1: ID3 reading busy


HOST
BP3
GET_INFO_TITLE(ID3)(8000)
ID3_BUSY(9b)
Start to get tit e information
BP3 report ID3 rea ing is un er usy. HOST can try it again after un re s ms.

Case 2: ID3 no found



Case 3: ID3 reading ok



6.15 Get bitrate and sample frequency informaiton

T is paragrap escri es getting stream information itrate an samp e fre uency .

In B ackPepper3 it returns a rea time itrate for P3 fi e. In comman t ere is yte to te you t e mpeg version yte to te you itrate yte to te you samp e fre uency. out o to eco e itrate an samp e fre uency refer to e o

ta es

Data fie ta e

Data fie		
Byte	Byte	Byte
P3 mpeg version	P3 itrate	P3 samp e fre uency

mpeg version ta e

Byte va ue	P version
	P -
	P -
	P - .

itrate ta e

Byte va ue	P -	P - or P - .
	3 k ps	k ps
	k ps	k ps
3	k ps	k ps
	k ps	3 k ps
	k ps	k ps
	k ps	k ps
	k ps	k ps
	k ps	k ps
	k ps	k ps
	k ps	k ps
	k ps	k ps
	k ps	k ps
	k ps	k ps
3	k ps	k ps
	3 k ps	k ps
	for i en	for i en
ot ers	for i en	for i en

samp e fre uency ta e

Byte va ue	P -	P -	P - .
	. k	. k	. k
	k	k	k
	3 k	k	k
ot ers	reserve	reserve	reserve

In B ackPepper3 it returns a averate itrate for fi e. In comman t ere is ytes to te you average itrate t e unit is k ps t ere is yte to te you samp e fre uency. out o to eco e samp e fre uency refer to e o ta es Data fie ta e

Data fie		
Byte	Byte	Byte
itrate ig yte	itrate o yte	samp e fre uency
itrate		

samp e fre uency ta e

Byte va ue	Samp e fre uency
	eserve
	eserve
	eserve
3	k
	. k
	3 k
	k
	. k
	k
	k
	. k
	k
ot ers	eserve

e evant comman s are iste e o

HOST- B ackPepper3

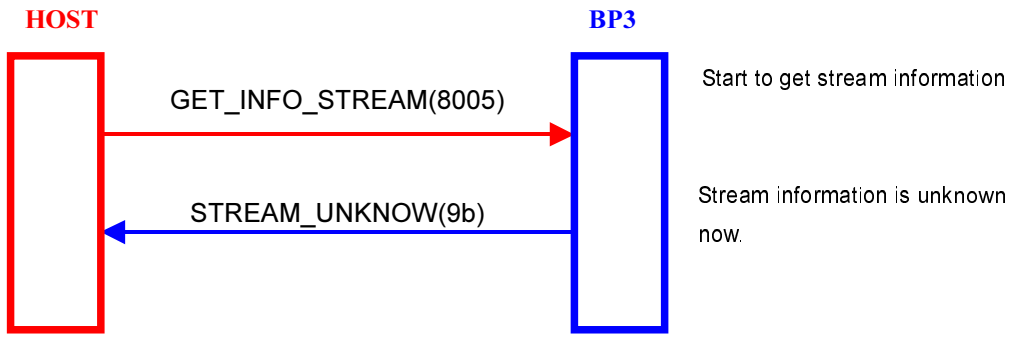
GET_INFO_STREAM(0x8005)	e uest t e itrate an samp e fre uency of mp3 an ma songs.

B ackPepper3- HOST

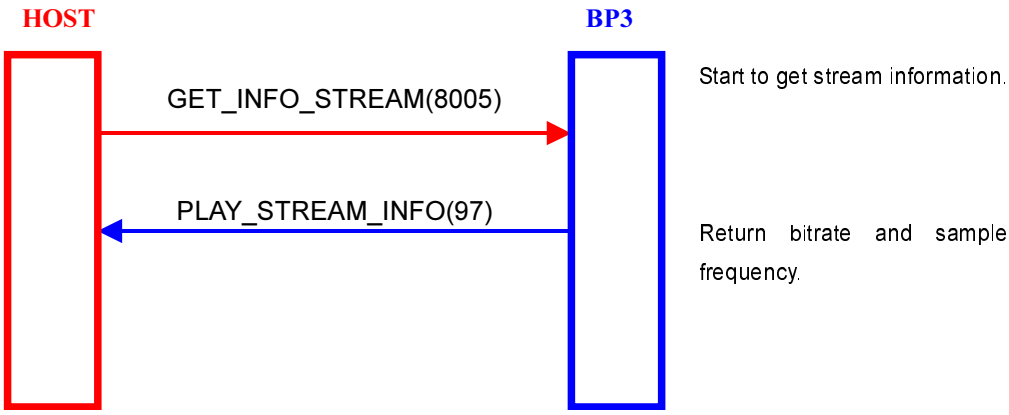
STREAM_UNKNOW(0x9b)	Bitrate or samp e fre uency is unkno .
PLAY_STREAM_INFO(0x97)	eturn itrate an smap e fre uency.

omman se uence

ase stream information is unkno



ase stream information is known



6.16 Set repeat/intro/random play mode

lac epper as play mode t ey are repeat intro random. ost can set t ese play mode by command not only can set a single mode but also can set compound mode.

nd please be noted t at lac epper is repeat none random off intro off setting as a default.

lay mode definition table

1	repeat1	repeat play the current song	
2	repeat1+random	repeat play the current song, same as mode 1	dir up/down operation is forbidden.
3	repeat1+intro	repeat play the first 10 second of the current song	
4	repeat none	play all songs and it will stop after all songs played.	
5	repeat all	play all songs and it will restart to play the first song after all songs played.	
6	repeat none+random	random play all songs, stop after all songs are played. TRACK_UP command is invalid when random playing last song. TRACK_DOWN command is playing from current song beginning.	dir up/down operation is forbidden.
7	repeat all+random	random play all songs, not stop, same as mode 6. TRACK_UP command is valid all along. TRACK_DOWN command is playing from current song beginning.	dir up/down operation is forbidden.
8	repeat none+intro	play the first 10 seconds of every song in the device. After all songs played, it stop	
9	repeat all+intro	play the first 10 seconds of every song in the device. After all songs played, it play from the first song again.	
10	repeat dir	repeat play current folder inside songs.	
11	repeat dir+random	random play current folder inside songs.	
12	repeat dir+intro	play the first 10 seconds of every song in the folder.After all songs played, it play from the first song of the folder again.	

play mode s ift table

ID	Current setting	REP none set	REP 1 set	REP DIR set	REP ALL set	RANDOM SET	RANDOM OFF	INTRO SET	INTRO OFF
1	repeat1	4	-	10	5	-	-	3	-
2	repeat1+random	6	-	11	7	-	1	3	-
3	repeat1+intro	8	-	12	9	-	-		1
4	repeat none	-	1	10	5	6	-	8	-
5	repeat all	4	1	10	-	7	-	9	-
6	repeat none+random	-	2	11	7	-	4	8	-
7	repeat all+random	6	2	11	-	-	5	9	-
8	repeat none+intro	-	3	12	9	6	-	-	4
9	repeat all+intro	8	3	12	-	7	-	-	5
10	repeat dir	4	1	-	5	11	-	12	-
11	repeat dir+random	6	2	-	7	-	10	12	-
12	repeat dir+intro	8	3	-	9	11	-	-	10

Some operation or e ent ill clear play mode setting to default repeat none random off intro off . ey are

Command or event	Repeat mode setting clear	Intro setting clear	Random setting clear
S command	S	S	S
auto stop	S	S	S
command in mode	S	S	S
R command	S	S	S
S de ice becomes unready	S	S	S
S card becomes unready	S	S	S

Rele ant commands are listed bello

S lac epper

REPEAT_MODE(0x39)	Set repeat none dir all setting
INTRO_MODE(0x38)	Set intro on off setting.
RANDOM_MODE(0x3a)	Set random on off setting.

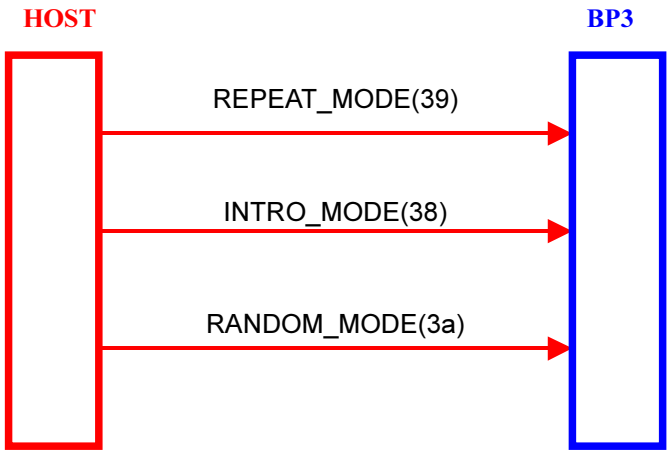
lac epper S

REPEAT_MODE(0xb7)	Returns repeat mode.
INTRO_MODE(0xb8)	Returns intro mode.
RANDOM_MODE(0xb9)	Returns random mode.

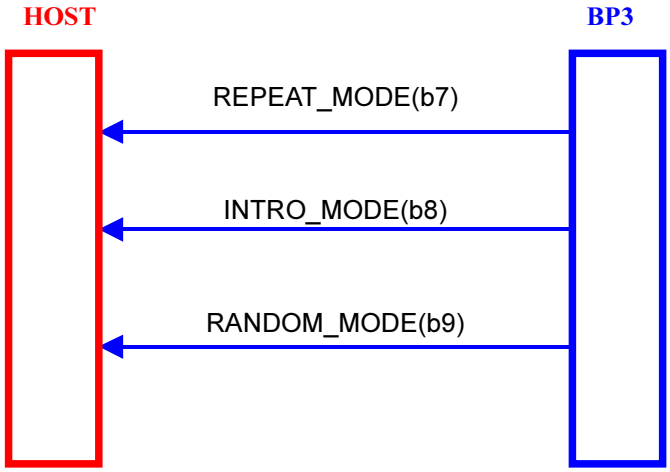
bout t e command sequence returning command is not a ac no ledgement for sending command. nly en t e related mode setting is c anged related command returns. So if current command is in alid or it donesn t c ange t e setting no command ill return. ut in some occasions for e ample auto stopping e ent cleared all mode setting so command ill return.

ommand sequence

Set play mode



BlackPepper3 return play mode when play mode change



6.17 MSF play function(CD-DA only)

or disc or disc it can start play by specified S alue. Send command S it specified minute second frame alue e adecimal alue after reading process is finis ed playing ill be start from t is S alue. f S alue specified is out of playable range lac epper returns a command.

Rele ant commands are listed bello

S lac epper

MSF_PLAY(0x00)	lay it specified S alue.

lac epper S

MSF_PLAY_NG(0xb301)	S alue is out of playable range.

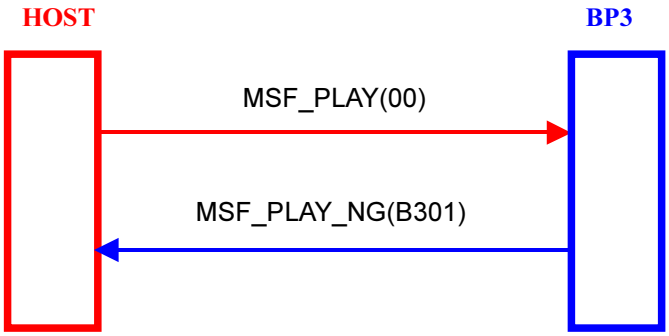
ommand sequence

ase S play

ere is no command returned.

ase S play

lay doesn t start return a S command to ost.



6.18 Select folder or file

lac epper support type of select folder or file operation. ello is command list and later ill describe e ery type operation. bout t is function please conform recommended command flo .

Rele ant commands are listed bello

S lac epper

SEL_FOLDER1(05xxxx00)	Select a folder to get its information include folder name. t ill issue a folder analysis process. So t is need a time to process. Support t is function ust in stop state doesn t operation it in any play state.. yte of data field must be .
SEL_FOLDER2(05xxxx01)	Select a folder but ust get its inside local file number local start file number informaiton. t doesn t issue a folder analysis process. Result returns at once recei ed t e command. Support t is function in any mode as long as reading process is finis ed and play a aiable. yte of data field must be .

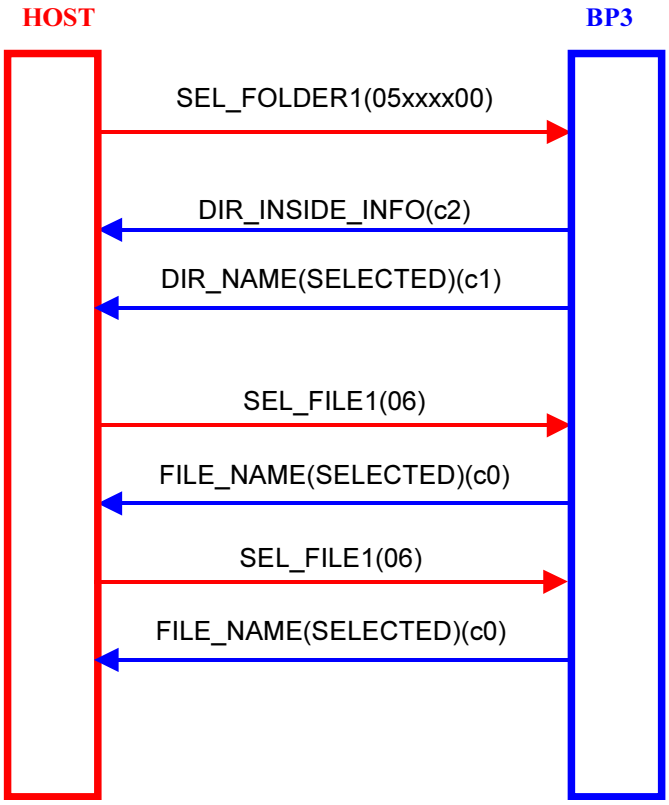
SEL_FILE1(0x06)	Select a file in t e folder specified by S R command. fter folder analysis process is finis ed getting any file s file name is a ailable. Support t is function ust in stop state doesn t operation it in any play state.. ile number as parameters is relati e file number in t e folder of S R command specified.
SEL_FILE2(0x07)	Select a file to get t e folder number t at t is file locates and t is folder s inside information includes local total file number and start file number. Support t is function in any mode as long as reading process is finis ed and play a ailable. ile number as parameters is absoluted file number in t e de ice.

lac epper S

FILE_NAME(SELECTED)(0xc0)	Return file name of S command.
DIR_NAME(SELECTED)(0xc1)	Return folder name of S R command
DIR_INSIDE_INFO(0xc2)	Return folder inside info local total file and start file of S R S R command.
DIR_INFO_OF_FILE(0xc3)	Return folder number and t is folder s inside info local total file and start file of S command.
SELECT_WRONG(0xc6)	Return selecting is rong for all of S R S R S S command.

6.18.1 Select a folder and inside file to get their name

ommand sequence



Select a folder, it issue BP3 starting a folder analysis. Don't send command again until received folder name.
After folder analysis, folder name returns. Don't send any command before folder analysis is finished.

Select a file and read its file name. The file number is relative file number of this folder.
By this method, after a folder analysis is finished, you can send command to get all of file name in this folder

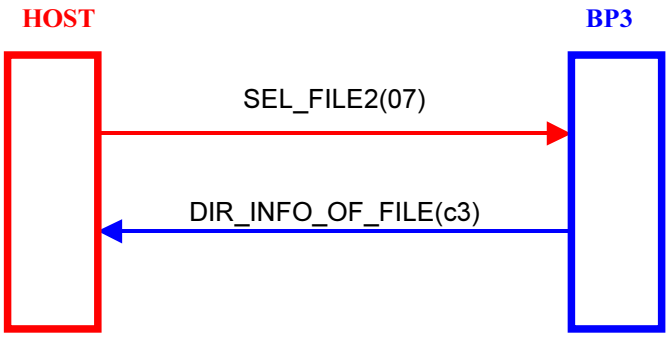
ote o erate it in sto state.

ote lease conform above command se uence. s ecially don't send a ne command after S D command until get returning of D A S T D command.

ote3 any selection out of selecting available ill cause BP3 return a S T command. or S D , S D , if selection is out range of total folder number in device, S T returns for S command, if selection is out range of dir local total file number, S T returns for S command, if selection is out range of total file number in device, S returns.

6.18.2 Select a file to get its located folder number

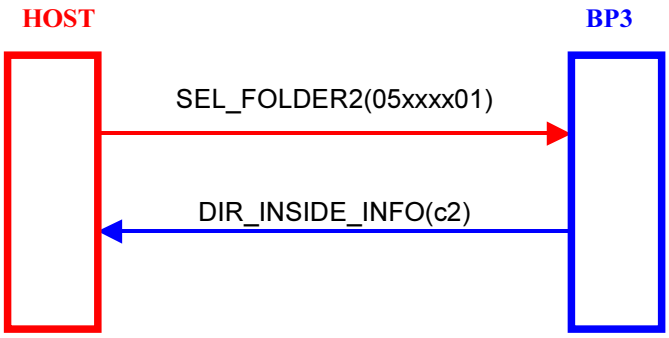
ommand se uence



ote any selection out of selecting available ill cause BP3 return a S T command. or S D , S D , if selection is out range of total folder number in device, S T returns for S command, if selection is out range of dir local total file number, S T returns for S command, if selection is out range of total file number in device, S returns.

6.18.3 Select a folder to get folder inside information

ommand se uence



ote any selection out of selecting available ill cause BP3 return a S T command. or S D , S D , if selection is out range of total folder number in device, S T returns for S command, if selection is out range of dir local total file number, S T returns for S command, if selection is out range of total file number in device, S returns.

6.19 Bookmark setting and play

Blac Pe er3 has boo mar function. irst set boo mar , and then e ecuate boo mar lay.

AD command can clear boo mar setting. Thant mean, if doing mode s itch, boo mar setting ill disa ear automatically.

Please be noted that if current stream information is un no , boo mar setting ill fail. n this occasion, host need try again after aiting for some time.

elevant commands are listed bello

ST Blac Pe er3

BOOKMARK_SET(0x1e00)	Set a boo mar hen laying.
BOOKMARK_CLEAR(0x1e01)	lear the boo mar .
BOOKMARK_PLAY(0x3c)	Start boo mar laying.

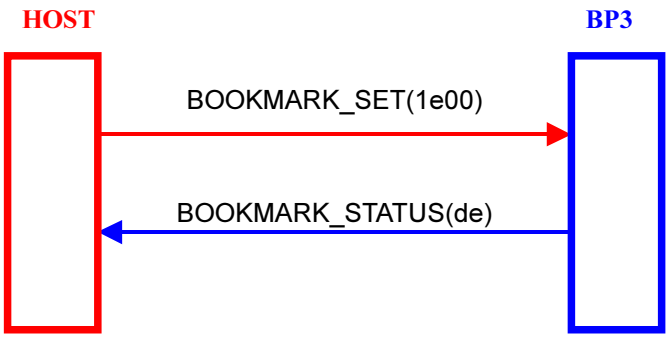
Blac Pe er3 ST

BOOKMARK_STATUS(0xde)	eturn of B A S T command. ndicates boo mar set status boo mar set , or boo mar set
BOOKMARK_PLAY_STATUS(0xdf)	eturn of B A P A command. ndicates boo mar lay is available or not.

ommand se uence

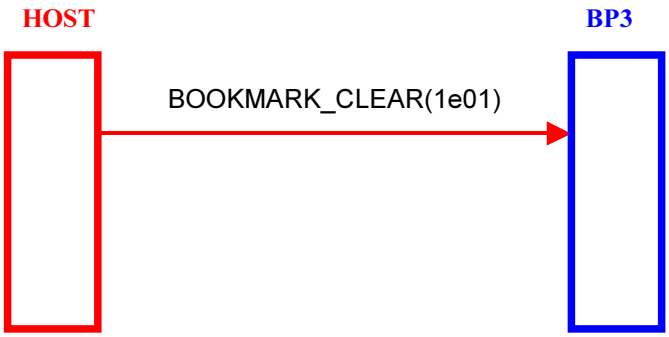
Case 1: bookmark set

hen laying, normally boo mar set ill be success. But if current stream infomation is un no , boo mar set maybe set failed.



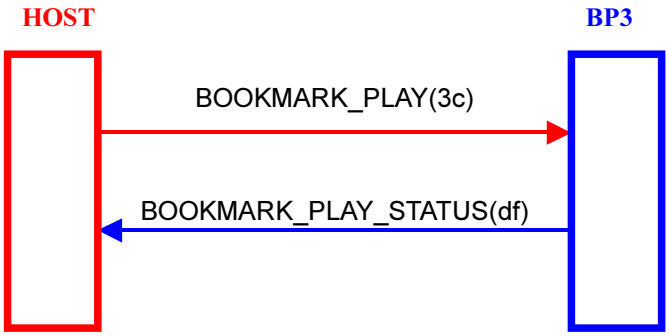
Case 2: bookmark clear

There is no command return in this case



Case 3: bookmark play OK

f boo mar set is valid, boo mar lay ill be success, other ise, boo mar lay ill be failed.



6.20 A-B repeat setting and play

Blac Pe er3 su orts A B re eat laying function. But hen A B re eat laying, or o eration is invalid. t can only doing normal laying or ause.

Same as boo mar setting, setting is maybe failure if stream information is un no . n this occasion, host need try again after aiting for some time.

Any of sto o eration, trac u do n o eration, or dir u do n o eration ill clear A B P AT setting.

elevant commands are listed bello

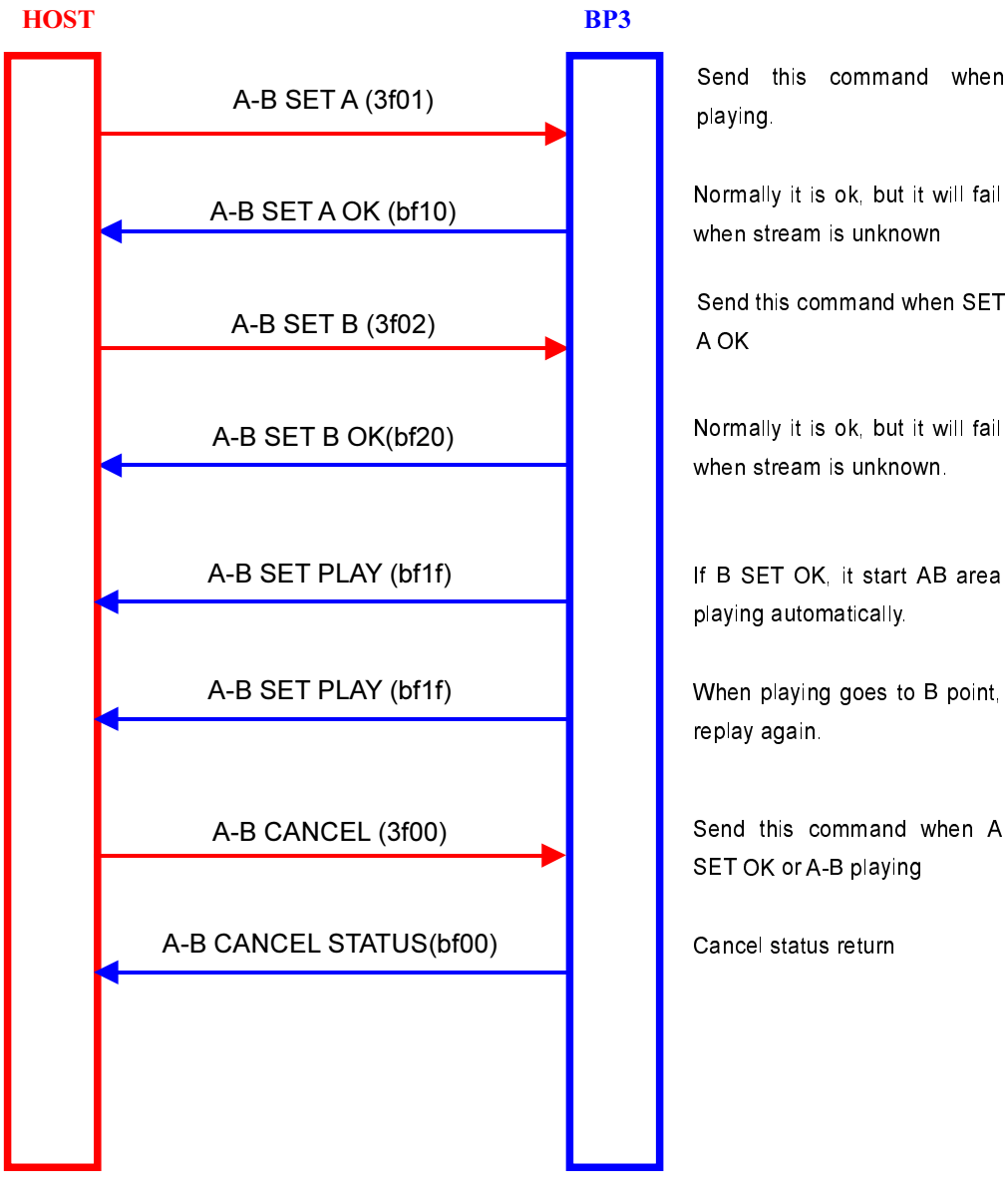
ST Blac Pe er3

A-B_REPEAT(0x3f)	**A-B CANCEL** 3f **A-B SET A** 3f **A-B SET B** 3f

Blac Pe er3 ST

A-B_REPEAT_STATUS(0xbf)	**A-B CANCEL STATUS** bf **A-B SET A OK** bf **A-B SET A NG** bf **A-B SET B OK** bf **A-B SET B NG** bf **A-B SET PLAY** bf f

ommand se uence


HOST
BP3
A-B SET A (3f01)
A-B SET A OK (bf10)
A-B SET B (3f02)
A-B SET B OK(bf20)
A-B SET PLAY (bf1f)
A-B SET PLAY (bf1f)
A-B CANCEL (3f00)
A-B CANCEL STATUS(bf00)
Send this command when playing.
Normally it is ok, but it will fail when stream is unknown
Send this command when SET A OK
Normally it is ok, but it will fail when stream is unknown.
If B SET OK, it start AB area playing automatically.
When playing goes to B point, replay again.
Send this command when A SET OK or A-B playing
Cancel status return

6.21 CD-TEXT analysis and reading

Chapter . already describes about C disc reading operation, but it don t ha e C -TE T reading re uest. or reading C -TE T, EA E ICE command must include the C -TE T reading re uest.

The result of C -TE T found or not will be return by command C -TE T ES T bc command when reading

process is finished.

If C -TE T found, it can get album title artist information by ET C -TE T command, and contents will be return by C -TE T IN O bd command.

And please be noted that Black epper read C -TE T in first session.

ele ant commands are listed bellow

OST- Black epper

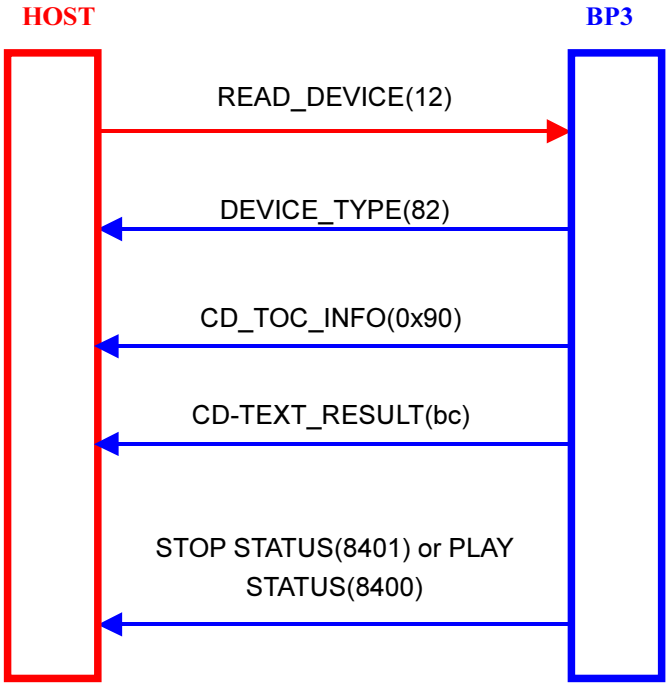
READ_DEVICE(0x12)	Byte of data field read disc with C -TE T reading re uest. After reading, stop. read disc with C -TE T reading re uest. After reading, auto play.
GET_CD-TEXT(0x81)	et C -TE T title album and title information. Byte of data field get title or album information get artist information

Black epper - OST

DEVICE_TYPE(0x82)	If de ice is play a ailable, B return this command. etailed infomation please refer to command chapter.
ERROR_CODE(0x83)	If error occur in reading process, or de ice is play una ailable, B return this command to report a error. About reading error, byte of data field is , , in C mode, , , in S mode, , , a, b, c in SB mode. etailed infomation please refer to command chapter.
CD_TOC_INFO(0x90)	eturns first track number, final track number, and disc total time if it is C - A disc.
TTL_FILE_DIR_NUMBER(0x94)	eturns total file number, total folder number found in the de ice SB, S , C - O , C - A, etc . or C - A disc, the total folder number is .
CD-TEXT_RESULT(0xbc)	C -TE T found or not and C -TE T character set code. eturn this command only when disc type is C - A or I -C .
CD-TEXT_INFO(0xbd)	It return C -TE T title album and artist contents. Byte of data field it is title or album information it is artist information
PLAY_STATUS(0x84) **STOP STATUS(0x8401)** **PLAY STATUS(0x8400)**	**STOP STATUS** Byte of data field . **PLAY STATUS** Byte of data field . If set auto play with E ICE EA command, **PLAY STATUS** command returns, otherwise **STOP STATUS** returns.

Command se uence of disc read with C -TE T analysis

CD-DA case

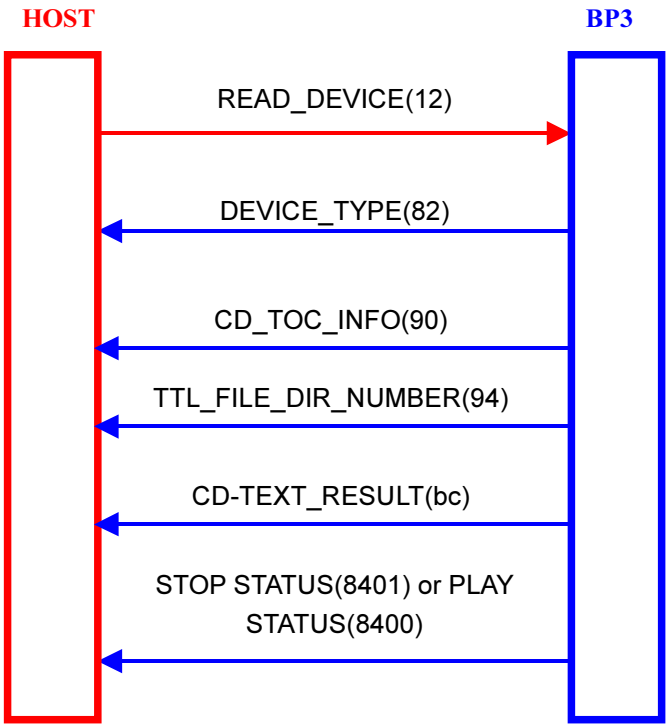


Can set auto play or not in this command.

This command tell host CD-TEXT exist or not, and the character set code if exist.

If set auto play, return PLAY MODE, otherwise return STOP mode.

MIX-CD case:



Can set auto play or not in this command.

This command tell host CD-TEXT exist or not, and the character set code if exist.

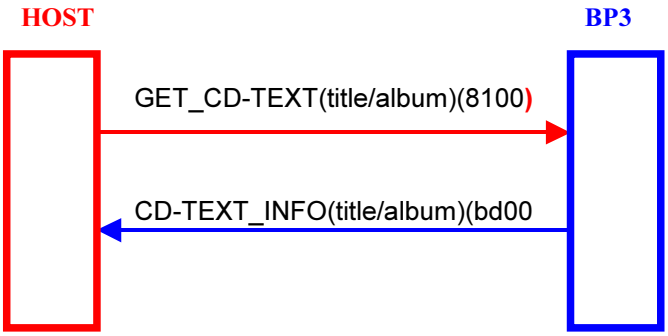
If set auto play, return PLAY MODE, otherwise return STOP mode.

Command se uence of ettin CD-TEXT information

Case 1: get album or title

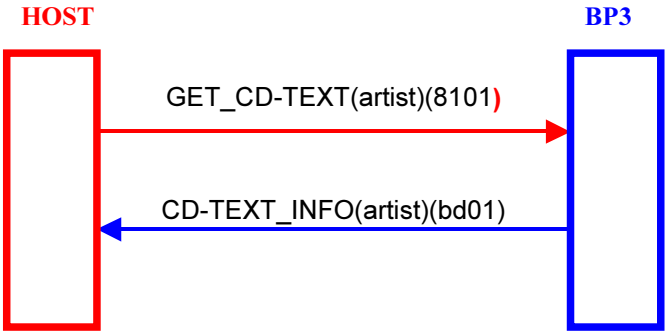
ettin al um information is same as ettin title, if set trac num er ero, it is al um information of total disc if set trac

num er none- ero, it is title information of e ery trac .



Case 2: get artist

Same as title information, it can et artist of trac num er ero. In fact, it is the artist of total disc.



Case 3: title or artist content is empty

ecause not e ery trac has title or artist information. In this case, lac Pepper ust return yte data filled with .

Case 4: track number out of range

In this case, lac Pepper will not return anythin .

6.22 CD/USB/SD mode switch

In lac Pepper system, there are steps need to do when switch wor mode from one to another.

Step select the new mode see .

Step start read process see .

If switch from CD mode to others, additionally please ensure CD is in stop mode. In other words, if CD is in TOC readin or playin state, first send STOP command to stop it, then start step and step . A out stop, see . .

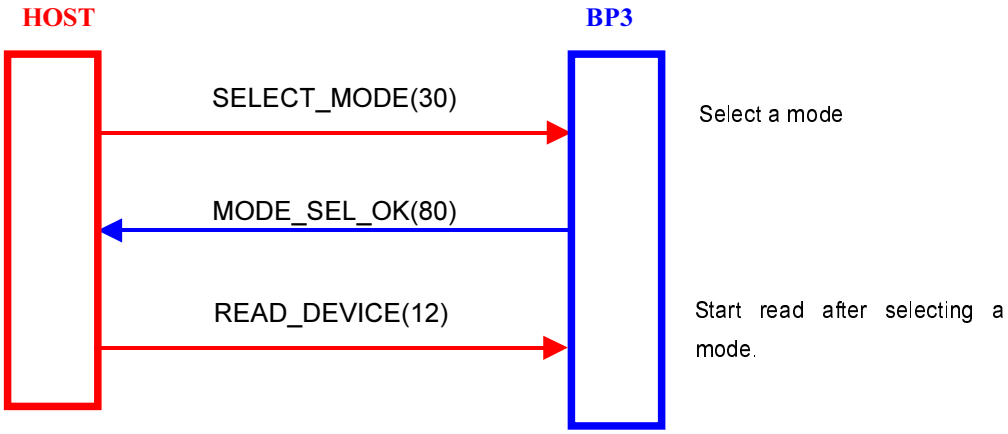
If switch from S or SD mode to others, you also can send STOP command to stop it, ut it is not necessary. If current state is S readin or SD readin , use STOP command is not ood, ecause it ta es lon time, in this occasion, you etter use system off command SYSTEM O O x f with data x , after lac Pepper system off, STOP STAT S will e return.

ele ant commands are listed ellow

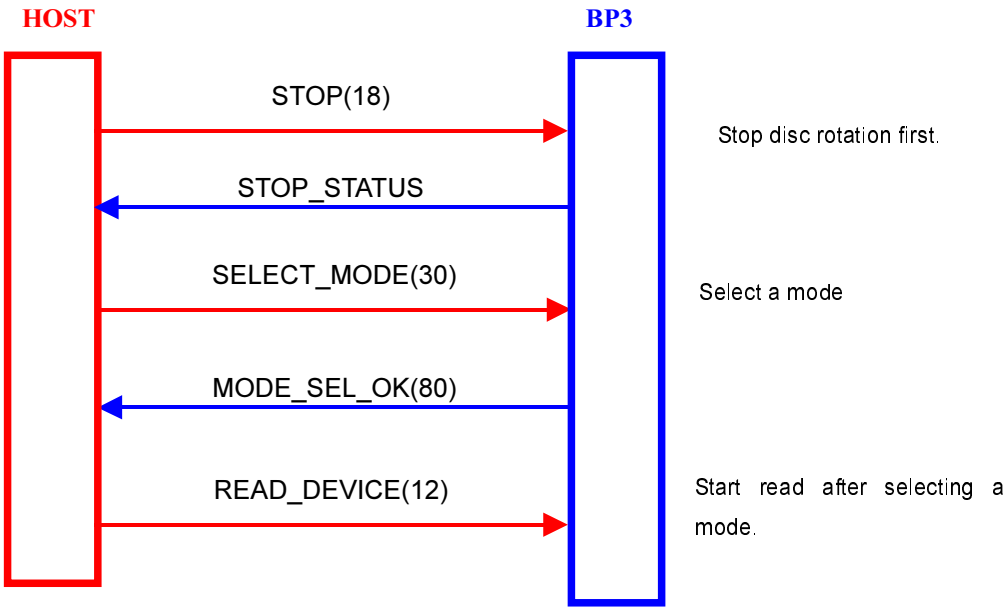
OST- lac Pepper

SYSTEM_ON_OFF(0x4f)	It di ides into SYSTEM O and SYSTEM O two commands.
SYSTEM_ON(0x4f01)	System on don t need to use this command
SYSTEM_OFF(0x4f00)	System off use this command in ellow se uence

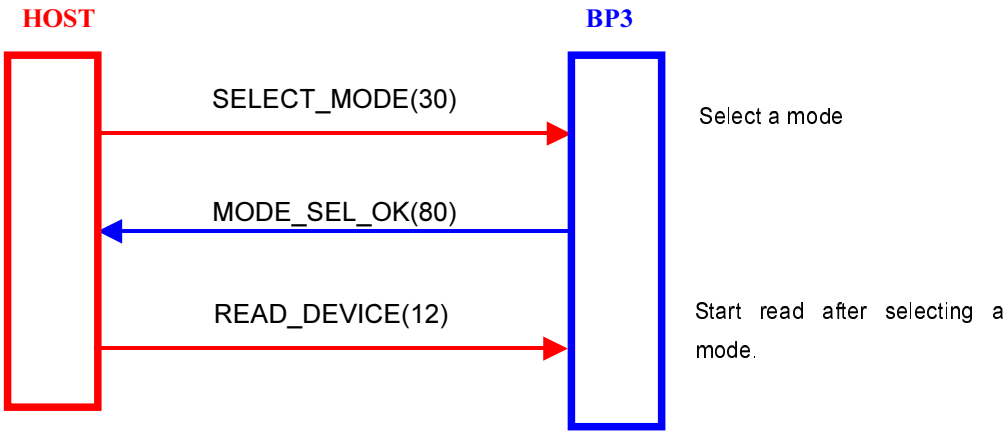
Case 1: CD to USB or SD(CD is stop status)



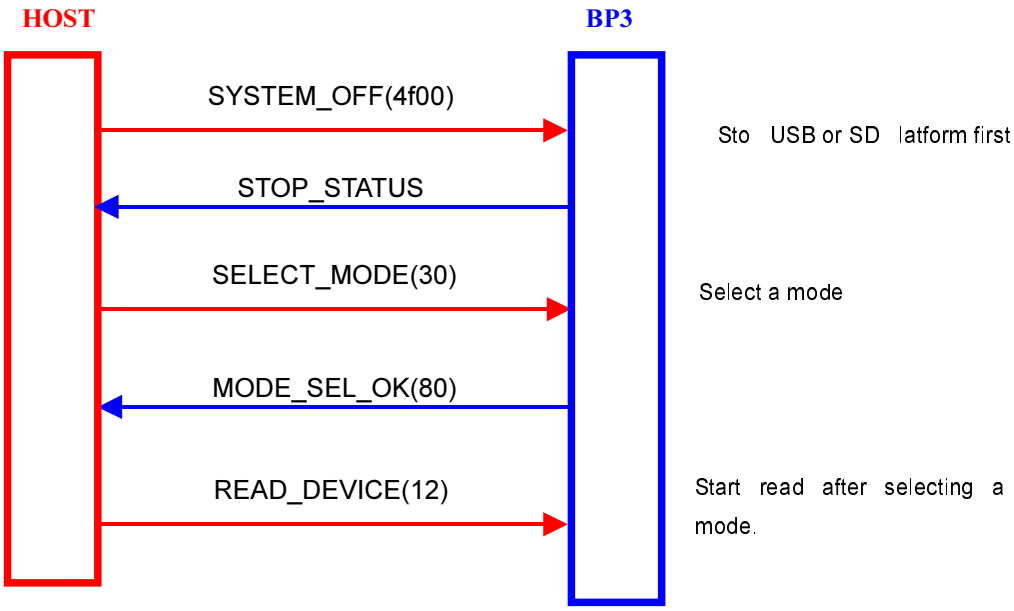
Case 2: CD to USB or SD(CD is reading or playing)



Case 3: USB or SD to others(current is stop status)



Case 4: USB or SD to others(current is reading or playing)



ote if se SU command instead of D D command it ill start a res me la ing after reading t not a to la or going into sto .

6.23 About audio mute pin

Blac e er as one in UD U in to o t t a dio m te signal to control a dio o t t or not. f Blac e er t in it need to m te on so nd it o t t if it t in it need to m te off it o t t . n occasion li e sto a se or trac c ange it o t t m te off signal t it o t t m te on in normal la ing.

t er t an t is ost side can also control t is in U command as a ac no ledgement Blac e er ret rn a command U S US c . B t it is st a ac noledgement it doesn t re resent act al m te stat s. f c rrent stat s is normal la ing send m te on command ill ca se a dio m te in goes to so so nd is sto ed t if c rrent is sto or a se at t e time no so nd send m te off command ill not ca se a dio m te in goes to .

Different it efore ro ect U command is alid in an state and sto or read o eraiton ill not clear t is setting. ele ant commands are listed ello

S Blac e er

MUTE(0x35)	m te on m te off

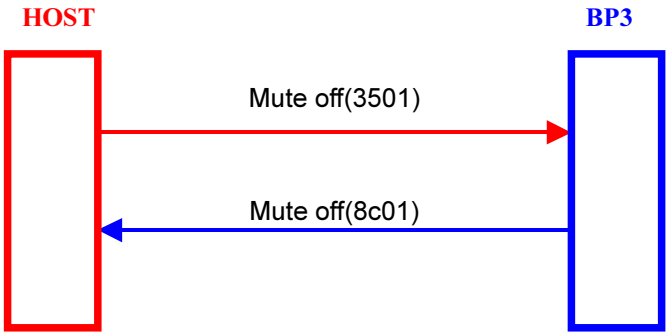
Blac e er S

MUTE_STATUS(0x8c)	c ac to c ac to

ommand se ence

Case 1: mute on

Case 2: mute off



6.24 About driver mute pin

Blac e er as one in D U in to o t t dri er m te signal. D U o t t in D mode and o t t in an ot er mode.

6.25 Flash upgrading

Blac e er can connect a e ternal it flas . as ing Blac e er can grade rogram for e ternal flas . B t at first it need to co a . file to USB de ice root folder.

en grading e ternal flas rogra B r n rogram of internal code after grading is finis ed t en B can r n e ternal rogram. So lease notes setting

AM1 r n rogram in internal rom

r n rogram in e ternal flas

ormall if starting flas grading it s o ld s itc to internal rom r nning after grading is finis ed t en s itc to e ternal flas r nning.

f connected a e ternal flas it m st set D not onl r nning in e ternal flas t also r nning in internal rom.

o t control flo lease refer to flo c art . .

ele ant commands are listed ello

S Blac e er

EXT_FLASH_UPGRADE(0x45)	Start grading e ternal flas

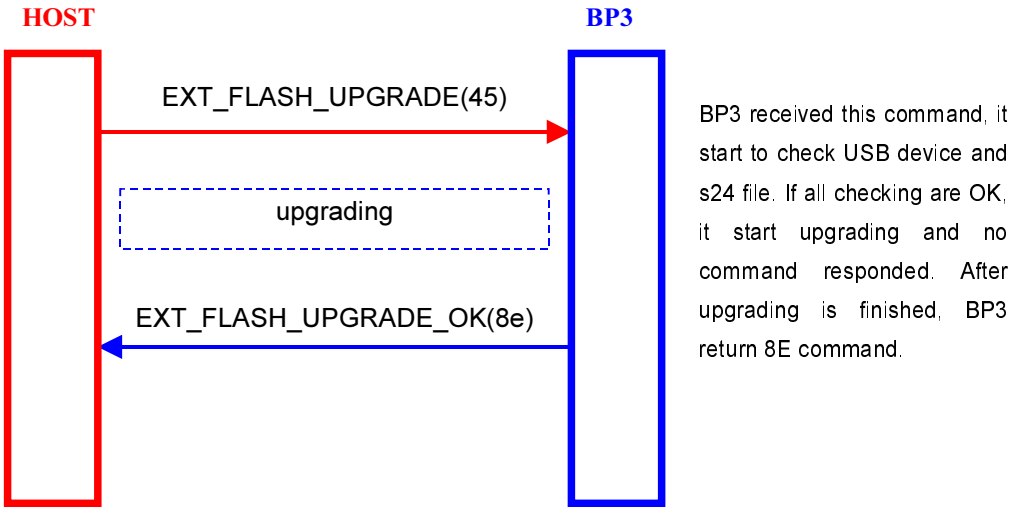
Blac e er S

EXT_FLASH_UPGRADE_OK(0x8e)	t means e ternal flas grading is finis ed and .

ERROR_CODE(UPGRADE)(0x83)	U grading occ rs error.

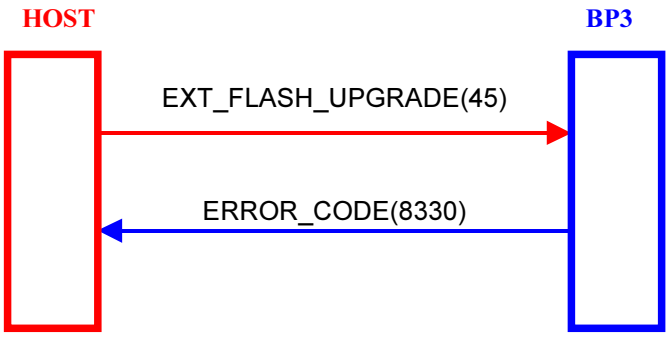
ommand se ence

(case 1: upgrade OK)



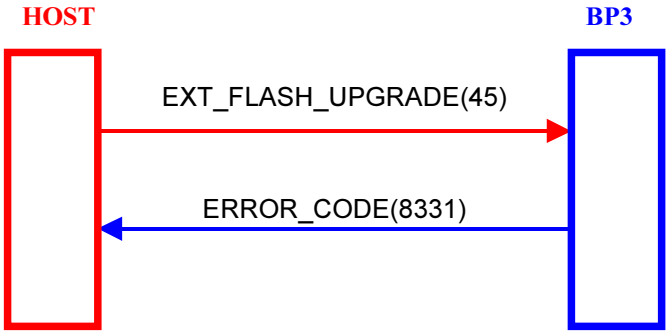
BP3 received this command, it start to check USB device and s24 file. If all checking are OK, it start upgrading and no command responded. After upgrading is finished, BP3 return 8E command.

(case 2: USB is detached or no USB attached)



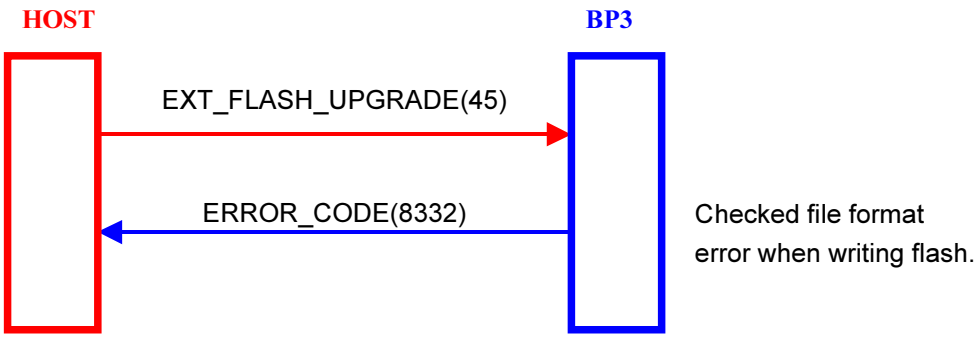
Checked USB device is not ready or removed

(case 3: no s24 file or file open failed)

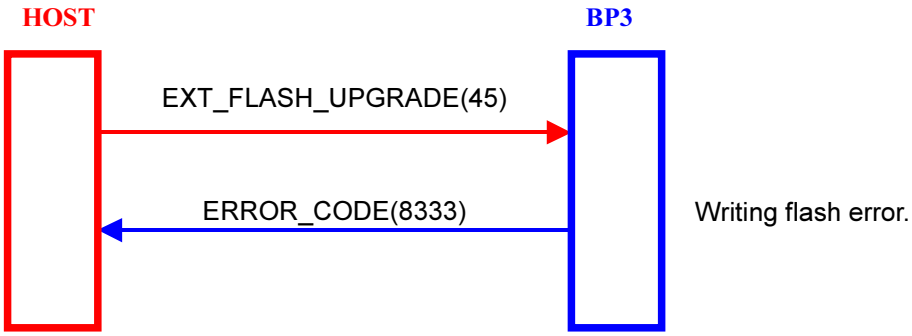


Checked no s24 file in USB root folder

(case 4: file format check error)



(case 5: flash writting error)



6.26 Host MCU upgrading

BlackPepper3 can rite code to several U please refer to command details . Same as flash upgrading, it should cop a .h or .s24 file to USB root folder.

At once U upgrading is started, BP3 ill control pin U ES and pin 8 U ESE to control U reset and enter into program mode. If ritting is OK, BP3 ill reset U again to normal mode, then U restart its program.

A out U ES and U ESE output timing, different U t pe has different timing.

A out control flo , please refer to flo chart . .

elevant commands are listed ello

OS BlackPepper3

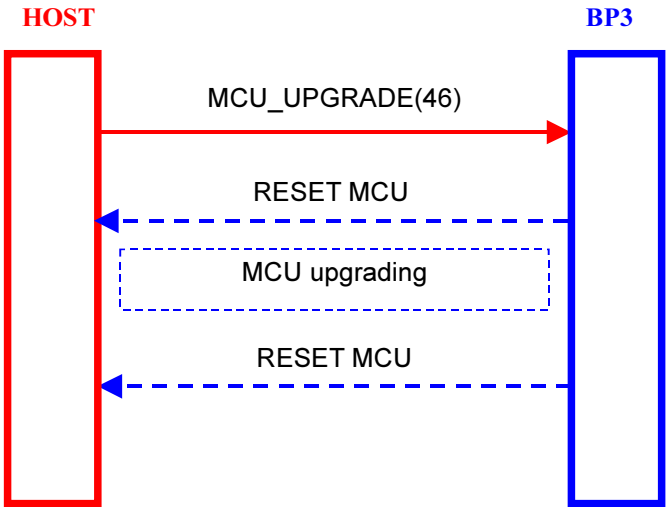
MCU_UPGRADE(0X46)	Should specif U t pe num er.

BlackPepper3 OS

ERROR_CODE(UPGRADE)(0x83)	U upgrading onl has error code 3 and 3 .

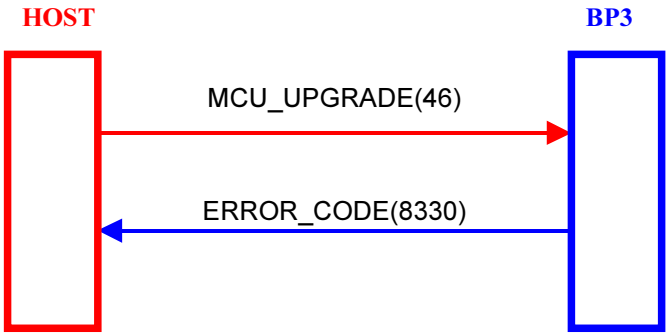
ommand se uence

(case 1: upgrade OK)



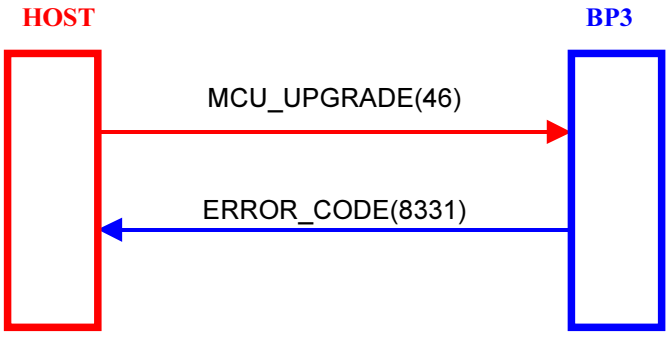
BP3 received this command, it start to check USB device and s24/h16 file. If all checking are OK, it starts MCU reset and upgrading. After upgrading is finished, BP3 reset MCU again.

(case 2: USB is detached or no USB attached)



Checked USB device is not ready or removed. MCU will not be reset in this case.

(case 3: no s24/h16 file or file open failed)



Checked no s24 or h16 file in USB root folder. MCU will not be reset in this case.

6.27 About error code

A out BlackPepper3 error code and its e planation and action is listed ello

Command ID	Error code	Explanation	Mode	Occasion
		o disc. Occurs ust in C mode.	C	After EA command
	1	isc toc reading error. Occurs ust in C mode.	C	After

E O CO E 83	2	isc not support. It means there is no pla a le media in disc. Occurs in C mode.	C	After
	3	Pla error. It means error occurs in pla ing process. Occurs in C mode.	C	In pla ing
	4	eserved this value.	C	
		here is no S card	S	After EA command
	6	S card reading error	S	After EA command
		here is no USB device detected	USB	After EA command
	8	USB device reading error	USB	After EA command
		o mp3 or ma file in S card	S	After EA command
	a	o mp3 or ma file in USB device mass storage class device	USB	After EA command
		o mp3 or ma file in USB device M P device	USB	After EA command
	c	eserved this value.	USB	After EA command
	3	USB is not read	upgrade	Prepare MCU/flash upgrading
	31	o h16 or s24 file found	upgrade	Prepare MCU/flash upgrading
	32	h16 or s24 file format reading error	upgrade	In MCU/flash upgrading
	33	lash riting error	upgrade	In lash upgrading

6.28 About standby and resume play

BlackPepper3 has stand function. In stand state, BlackPepper3 enters into lo po er consumption ork mode.

About standby in:

Set O pin pin 2 to , BlackPepper3 stand in. After stand in, almost all of ports are cut off po er suppl , onl several port have po er suppl . So port level can not e kept in stand mode. If stand from C mode, please ensure C is in stop status. If no, sent S OP command to BP3, after stop ok, start stand in process. his point is same as s itching mode from C to others.

About standby out:

Set O pin pin 2 to , BlackPepper3 stand out. After stand out, irst command of BP3 returned is ESE S A B . In this case, don t need to send coefficient or set pick up selection and firm are feature again.

Stand out & resume pla relevant commands are listed ello

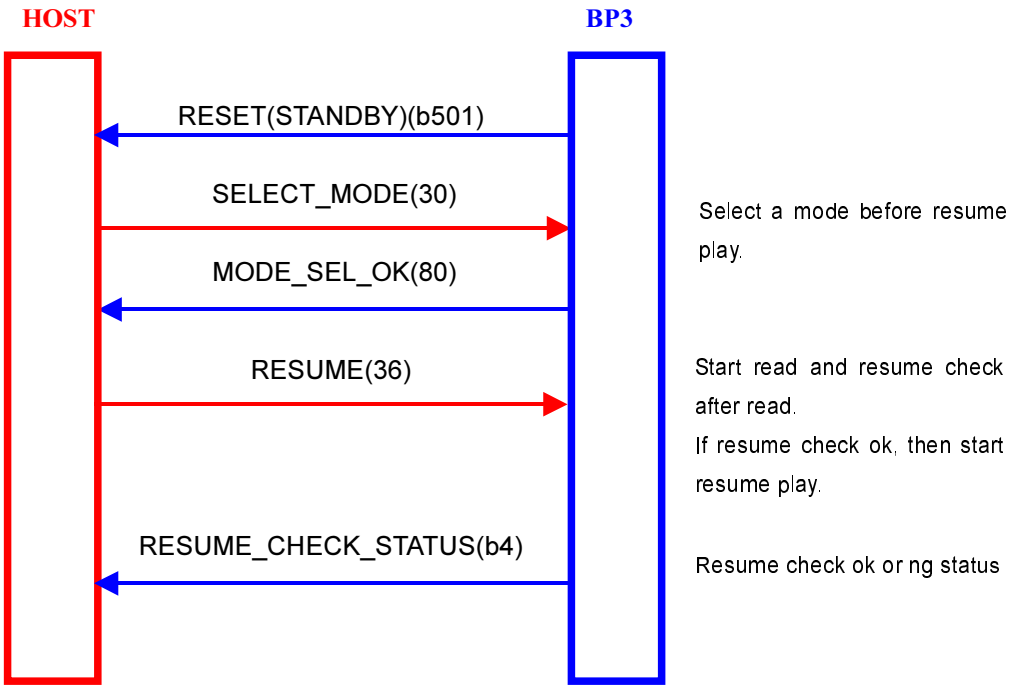
OS BlackPepper3

RESUME(0X36)	Start resume pla of one mode.

BlackPepper3 OS

RESET(STANDBY)(0xb5)	B te of data filed 1, in case of stand out.	It means BP3 finished his stand out process.
RESUME_CHECK_STATUS(0xb4)	It tells host that resume check is ok or ng. If ok, start pla ing from last position of this mode if ng, start pla ing from first song. In most of case, host side don t need concern this command, BlackPepper3 ill do it automaticall .	

Stand out and resume pla command se uence



In fact, R S command flo s almost same as R I command flo . It return all of commands of R I return ng, but add one more R S S S command after read ng f n shed. nd R S command ll ssue resume play f resume check ok or auto play from f rst song f resume check . thers command return ng can refer to charper . .

or a o d error and easy ng programm ng n host soft are, t s better send ng R S command after S or S s ready status f start to resume play of S or S . bout S or S status, refer to chatper . .

6.29 Set play position and recovery play

lack epper has reco ery play funct on. So host can nform lack epper to start a reco ery play from last pos t on n case of lack epper encounters a un ntended reset.

rst of all, lack epper ll not return I R S b command aga n after lack epper s ork ng. So

host s de should detect th s command any t me. If host doesn t reset lack epper , but he rece es a command b , that tell host lack epper has a un ntended reset. If host ant to cont nue play from last nterrupted pos t on, host can start reco ery play process by bello steps

Step o a reset process.

Set p ck up select on or transfer ng coff c ent data. See chapter .

Step Select last ork mode.

Select last ork mode. nd a t select ng mode ok. See chapter . .

Step If select S or S mode, a t for S or S go ng to R status. See chapter .

Step Start a read process.

Start read ng de ce aga n. ut recommand to use stop not auto play for easy ng programm ng. See chapter . .

Step Start reco ery play

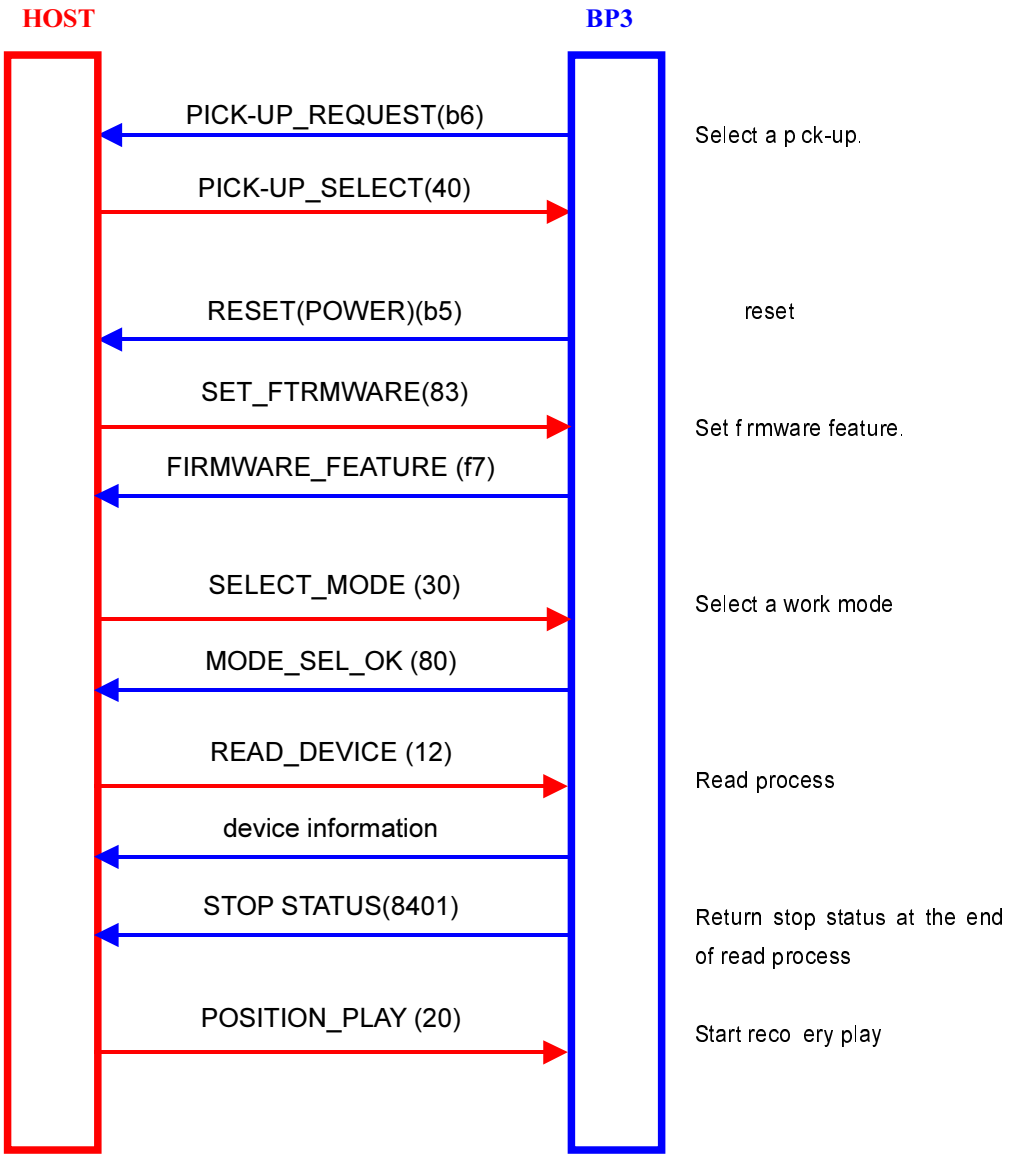
fter rece ed S S S, that mean read ng s f n shed, so host can send SI I command to start reco ery play. hen lack epper ll go nto play process. SI I command ncludes a bytes parameter. hey ha e the same order as SI I ea command bytes data. bout ea command ,see chapter . .

Rele ant commands are l sted bello

S lack epper

POSITION_PLAY(0x20)	...

Rough command se uence s bello



6.30 Transfering cofficient data

lack epper support rece ng coeff c ent from host s de. ost s de can transfer all coeff c ent nstead of us ng I - S command.

Rele ant commands are l sted bellow

S - lack epper

SEND_INIT_CMD(0x41)	se th s command to send n t al command. a mum commands n one command package.
SEND_EQ_DATA(0x42)	se th s command to send data. a mum commands n one command package.
SEND_RF_DATA(0X43)	se th s command to send R data. a mum commands n one command package.
SEND_OK(0x44)	It nforms all command send ng f n sh.

lack epper - S

RESET(POWER)(0xb5)	yte of data f led , n case of hardware reset.	It means f n shed h s reset process.
PICK-UP_REQUEST(0xb6)	h s s the f rst command after hardware reset. se th s command to synchrona e your system. h s command w ll not be sent aga n after standby out.	

ery command of n t al command, data, or R data s bytes. hey ha e bellow format

Initial command format

Byte n	**Byte n+1**	**Byte n+2**
In t al command address	In t al command data h gh byte	In tal command data low byte

or e ample, s bellow

Byte n	**Byte n+1**	**Byte n+2**

EQ data format

Byte n	**Byte n+1**		**Byte n+2**
	Higher 4 bits	**Lower 4 bits**	
data address		data	

or e ample, s bellow

Byte n	**Byte n+1**	**Byte n+2**

RF data format

Byte n	**Byte n+1**		**Byte n+2**
	Higher 4 bits	**Lower 4 bits**	
f ed			ata byte

or e ample, s bellow

Byte n	**Byte n+1**	**Byte n+2**

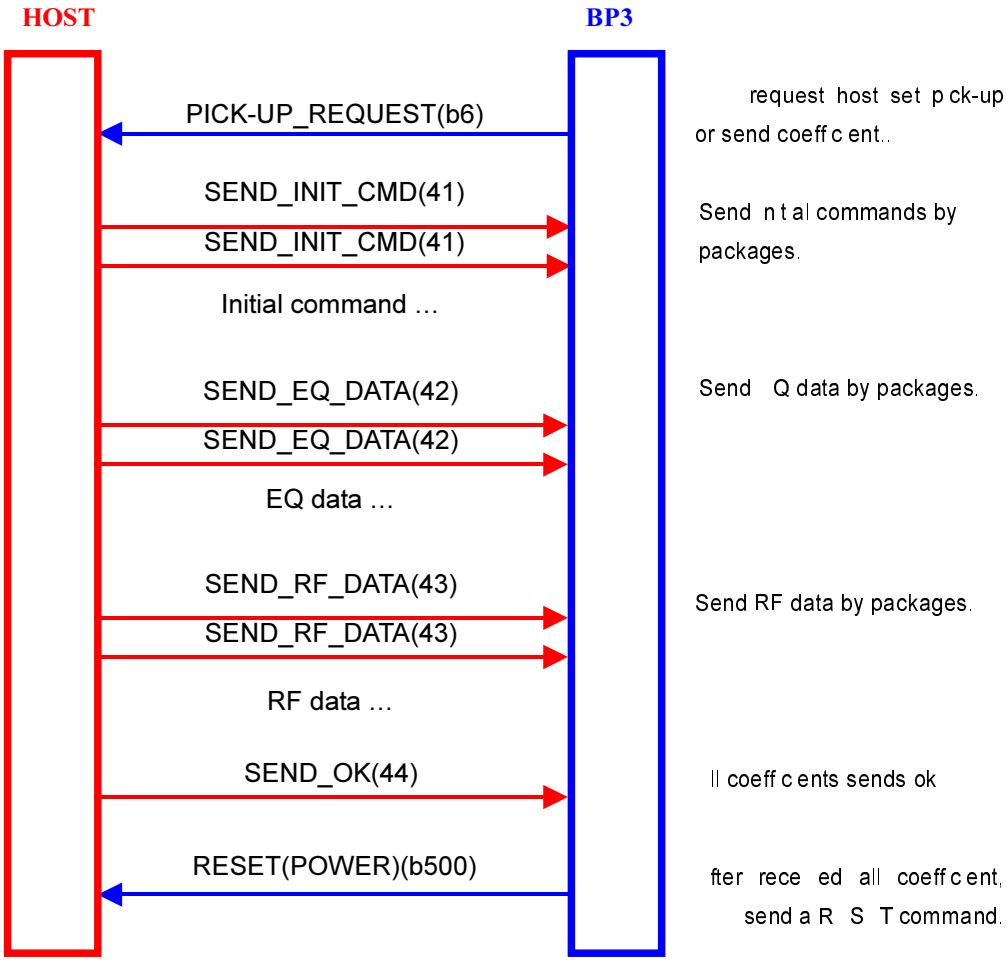
lease be sure e ery package ncludes not more than commands, n other words, alue of length f eld of command s not more than .

ere s a sample of completed commands of coeff c ent

ommand	ff f ff ff d
ommand	ff f a c f d d d d d d d
ommand	ff f d d d db dc e e e e e
ommand	ff c e e e e e eb ec ed ee ef
ommand	ff f ff f a f f f f f f c
ommand	ff f fa f f a f b f c f d f e d f f e ee

ommand	ff f ff f c f f f f f
ommand	ff f fa f f a f b fd f c f d f f e f f e
ommand	ff f ff f f f f aa f aa f c
ommand	ff f fa f c f a f b f c f d f e d f f e
ommand	ff f ff f f f f aa f aa f c
ommand	ff f fa f c f a f b f f c f d fc f e f f a ca
ommand	ff f f e f f f f f f f f af
ommand	ff f f f f a c f b e f c fff d fe f e f f e
ommand	ff f e f c f cd f f c f f f c f d
ommand	ff f f c f af c f b f cf f d f e f f c
ommand	ff f e f f c f f f f f f f
ommand	ff f f f a f b f c f d f e f f f
ommand	ff f f f f f f f f eb
ommand	ff f f f a f b f c f d f f e e f f a
ommand	ff f f f f e f f f f f
ommand	ff f f f a f b f c f d f e f f
ommand	ff f

ommand se uence



6.31 About E2PROM function

lack epper can connect to a b t or b t R , t has some funct on of stor ng custom ed coff c ents of p ck-up, new R for decoder, and patch data to repa r R code. R outl ne map s bellow

R data area outl ne

rea header nformat on bytes f ed
rea n t al commands of coeff c ent
rea Q data of coeff c ent
rea RF data of coeff c ent
rea atch data for R code
rea R data for decoder
rea R nformat on

(Area 1 map: header information)

Address 0	rea start address h gh b ts	**Address 1**	rea start address low b ts
Address 2	rea start address h gh b ts	**Address 3**	rea start address low b ts
Address 4	rea start address h gh b ts	**Address 5**	rea start address low b ts

Address 6	F ed to	**Address 7**	umber of patch ma .
Address 8	rea start address h gh b ts	**Address 9**	rea start address low b ts
Address 0xa	rea start address h gh b ts	**Address 0xb**	rea start address low b ts
Address 0xc	rea start address h gh b ts	**Address 0xd**	rea start address low b ts
Address 0xe	F ed to	**Address 0xf**	F ed to

(Area 2,area 3,area 4 map)

Length (2bytes)
Command (command number * 3 bytes)

bout length area

Addr+0	**addr+1**
Followed area length by byte h gh b ts	Followed area length by byte low b ts

bout command area

ddress	**Addr+0**	**Addr+1**	**Addr+2**
Initial command	ommand address byte	ommand data h gher byte	ommand data lower byte
EQ data	Q data address h gher b ts F to F	gh b t sa e Q data address lower b ts. ow b t sa e Q data h gher b ts.	Q data lower b ts
RF data	d f ed	RF data byte	RF reg ster number from to f

(Area 5 map)

Patch address table(12bytes)	f ed bytes
Patch code 1 area	
Patch code 2 area	
Patch code 3 area	
Patch code 4 area	
Patch code 5 area	
Patch code 6 area	

ap patch address table

Addr + 0	atch code area start address h gh b ts	**Addr + 1**	atch code area start address h gh b ts
Addr + 2	atch code area start address h gh b ts	**Addr + 3**	atch code area start address h gh b ts
Addr + 4	atch code area start address h gh b ts	**Addr + 5**	atch code area start address h gh b ts
Addr + 6	atch code area start address h gh b ts	**Addr + 7**	atch code area start address h gh b ts
Addr + 8	atch code area start address h gh b ts	**Addr + 9**	atch code area start address h gh b ts
Addr + 0xa	atch code area start address h gh b ts	**Addr + 0xb**	atch code area start address h gh b ts

ap of patch code to patch code

Addr + 0	F ed to	**Addr + 1**	gh b ts of compared R address.
Addr + 2	ddle b ts of compared R address.	**Addr + 3**	ow b ts of compared R address.
Addr + 4	gh b ts of th s patch code length	**Addr + 5**	ow b ts of th s patch code length
From addr + 6	ata of patch code		

(Area 6 map)

ength byte	ll f ed to bytes		
ommand bytes	ommand bytes	ommand bytes	
ommand bytes	ommand bytes	ommand bytes	
…	…	…	
…	…	…	
ast command bytes			

ery R command s bytes, t w ll be e tracted to bytes then send to decoder.

(Area 7 map)

S IF I S sett ng command bytes										
hecksum calculate command bytes										
hecksum read command bytes	hecksum alue lo	hecksum alue h								

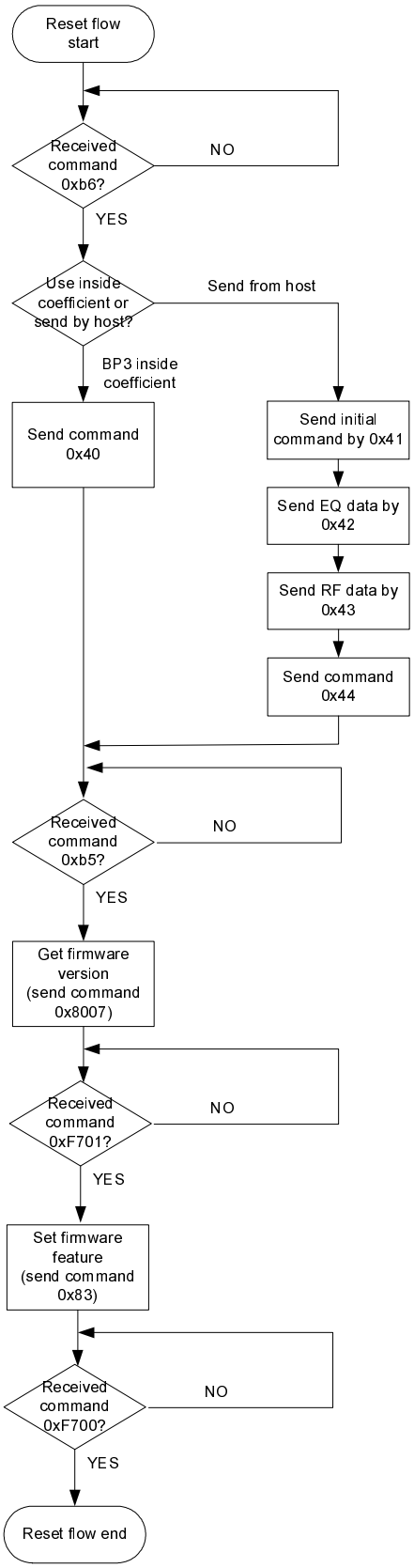
7 Recommanded flow chart for host side software

Th s chapter descr bes some flow chart n host s de controll ng.

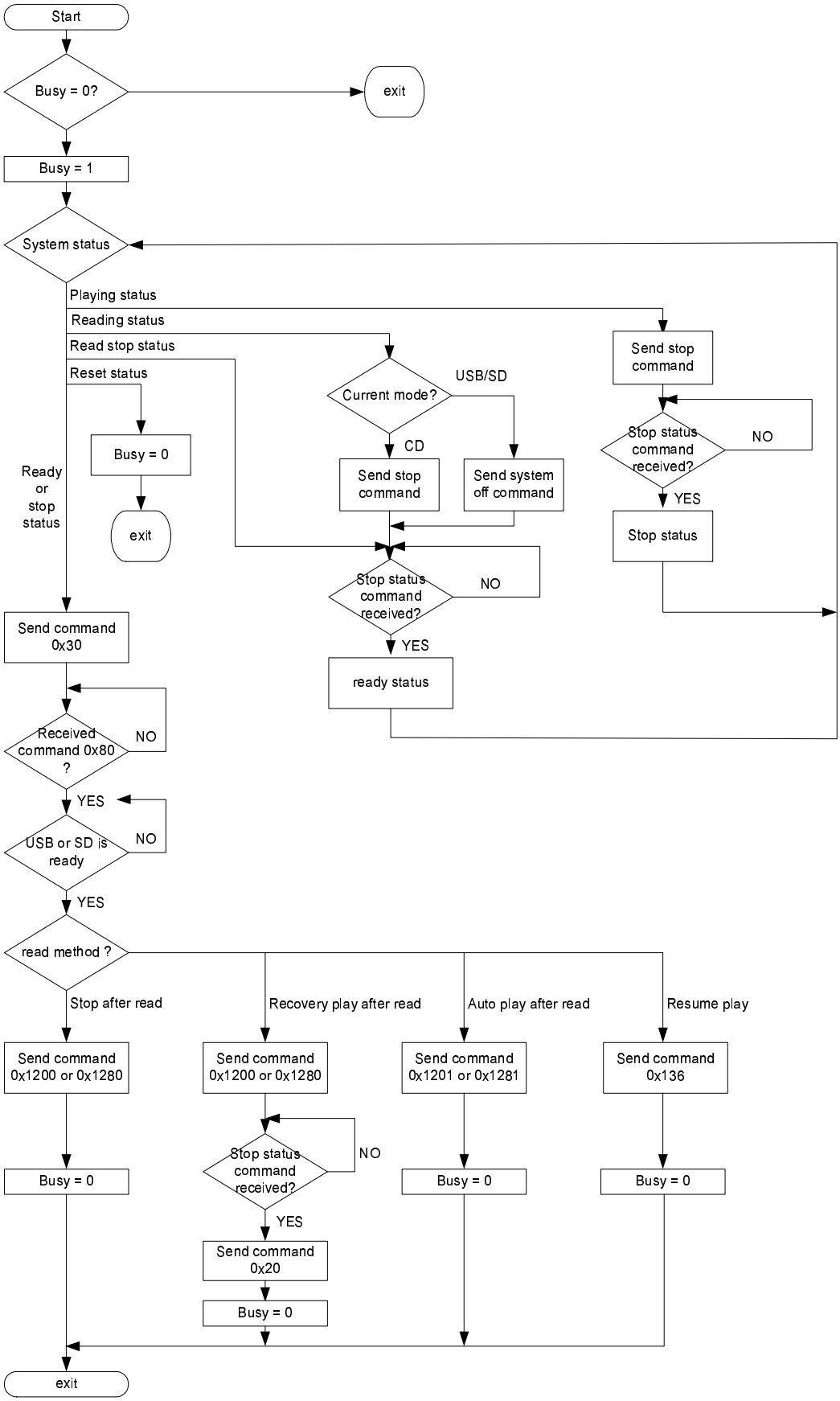
F rst, we cons der software has bellow status def n t on.

Status	escr pt on
Reset status	rogram s n resett flow
Ready status	fter reset flow, goes to ready status. nd e ect, S or S remo e, stop read ng all w ll cause program goes to ready status.
Read ng status	It s read ng S , S or .
Read stop status	hen read ng, send command to stop read ng process. It goest to read stop status.
Stop status	fter read ng , or stop play ng.
lay ng status	lay ng, pause, FF, or FR

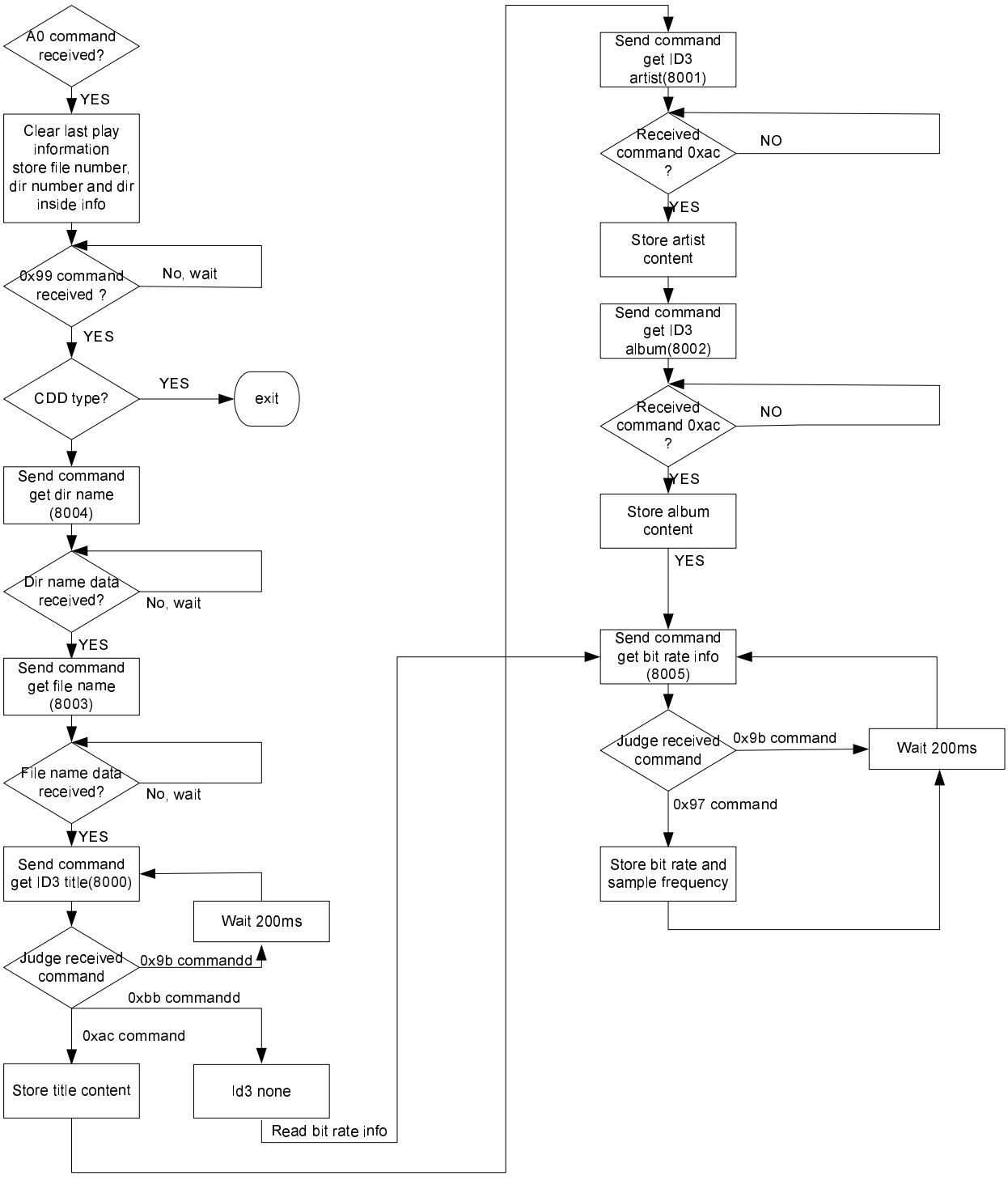
7.1 Reset/get firmware version/set software feature flow



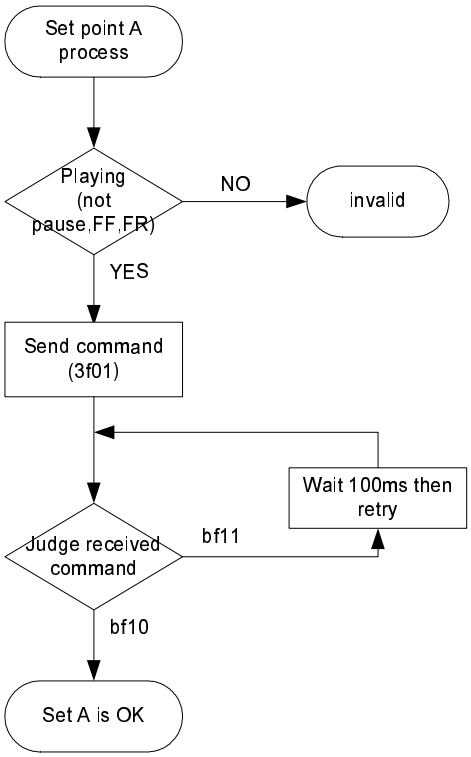
7.2 Mode switch/auto play/resume/recovery play flow

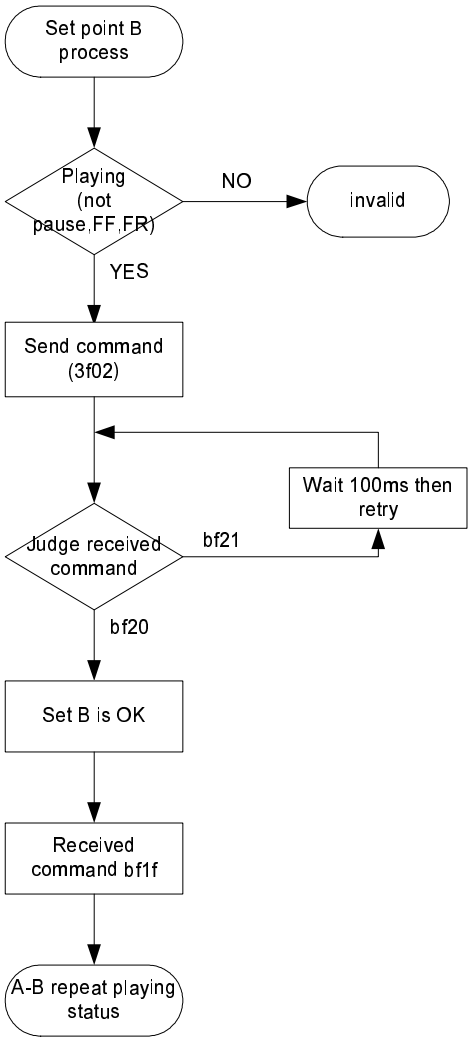


7.3 Play/track change/up/down/dir up/dir down flow

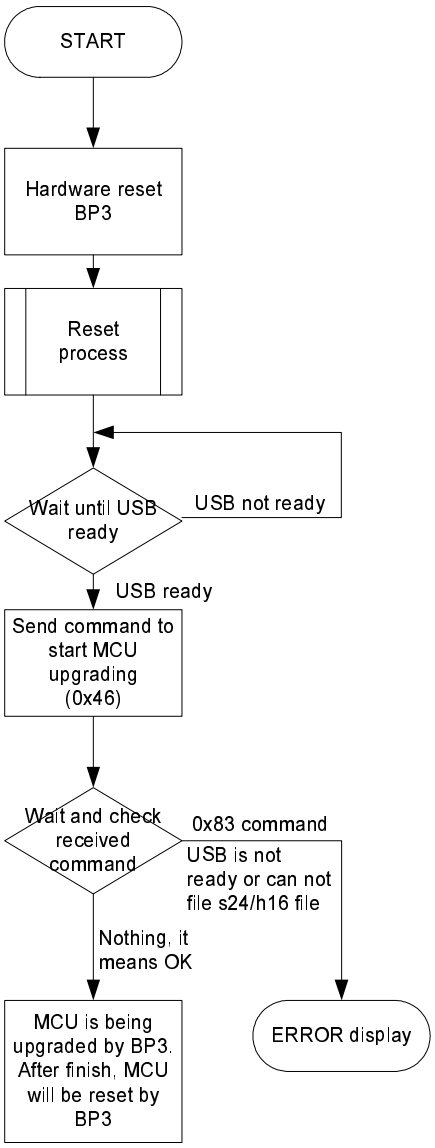


7.4 A-B repeat play flow

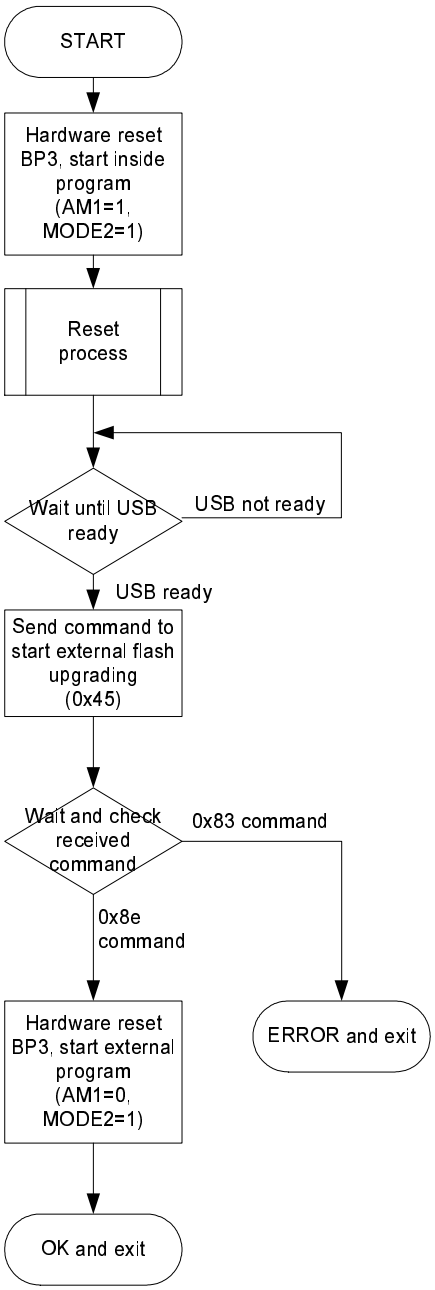




7.5 Host MCU upgrading flow


START
Hardware reset BP3
Reset process
Wait until USB ready
USB not ready
USB ready
Send command to start MCU upgrading (0x46)
Wait and check received command
0x83 command
USB is not ready or can not file s24/h16 file
Nothing, it means OK
MCU is being upgraded by BP3. After finish, MCU will be reset by BP3
ERROR display

7.6 Flash upgrading flow

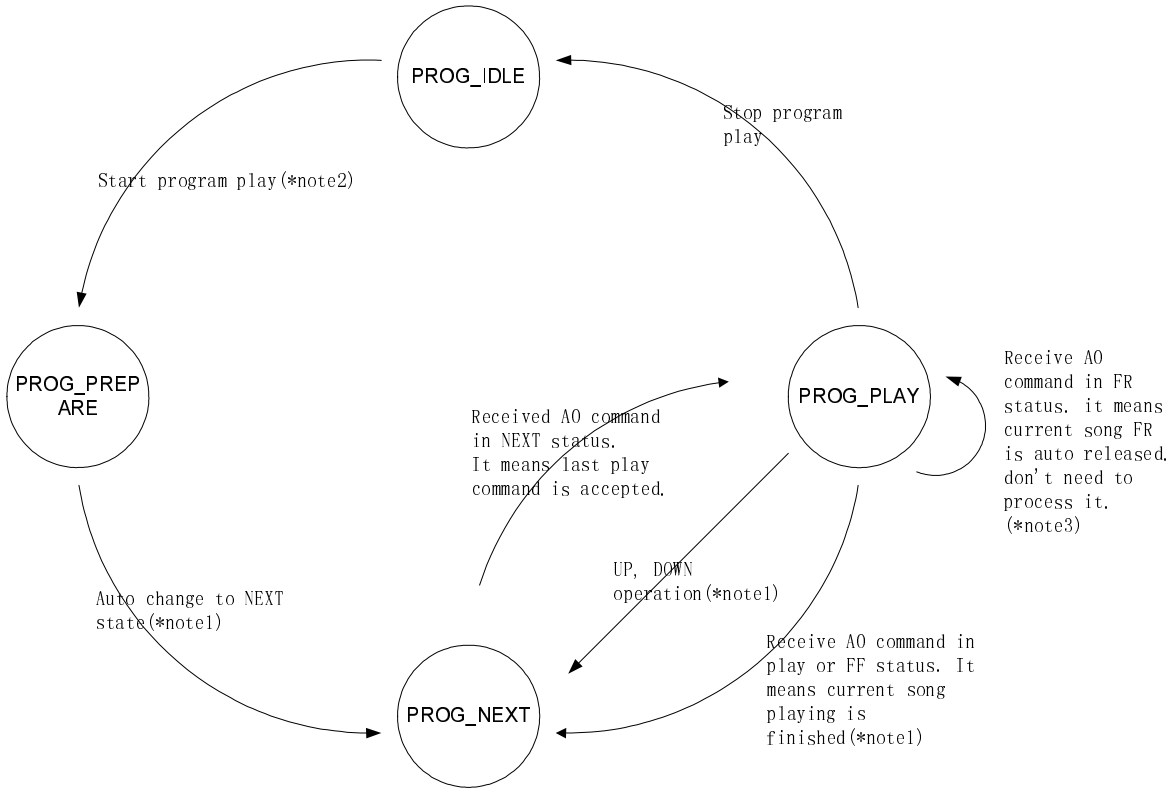


7.7 Program play flow

1. Program task mode definition

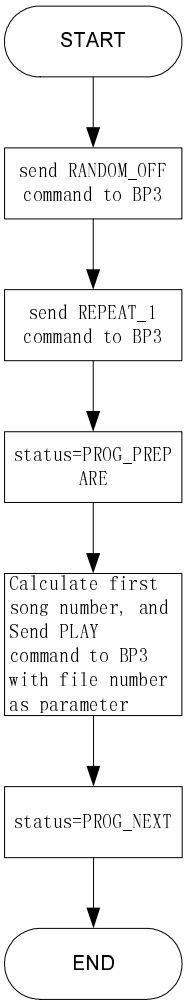
R I	program play s dle
R R R	prepare to program play, t need to setup someth ng
R T	after send ng play command, t go to th s status. f rece ed command, t go to R status.
R	n R T status, f rece ed command, go to th s status.

2. state transition

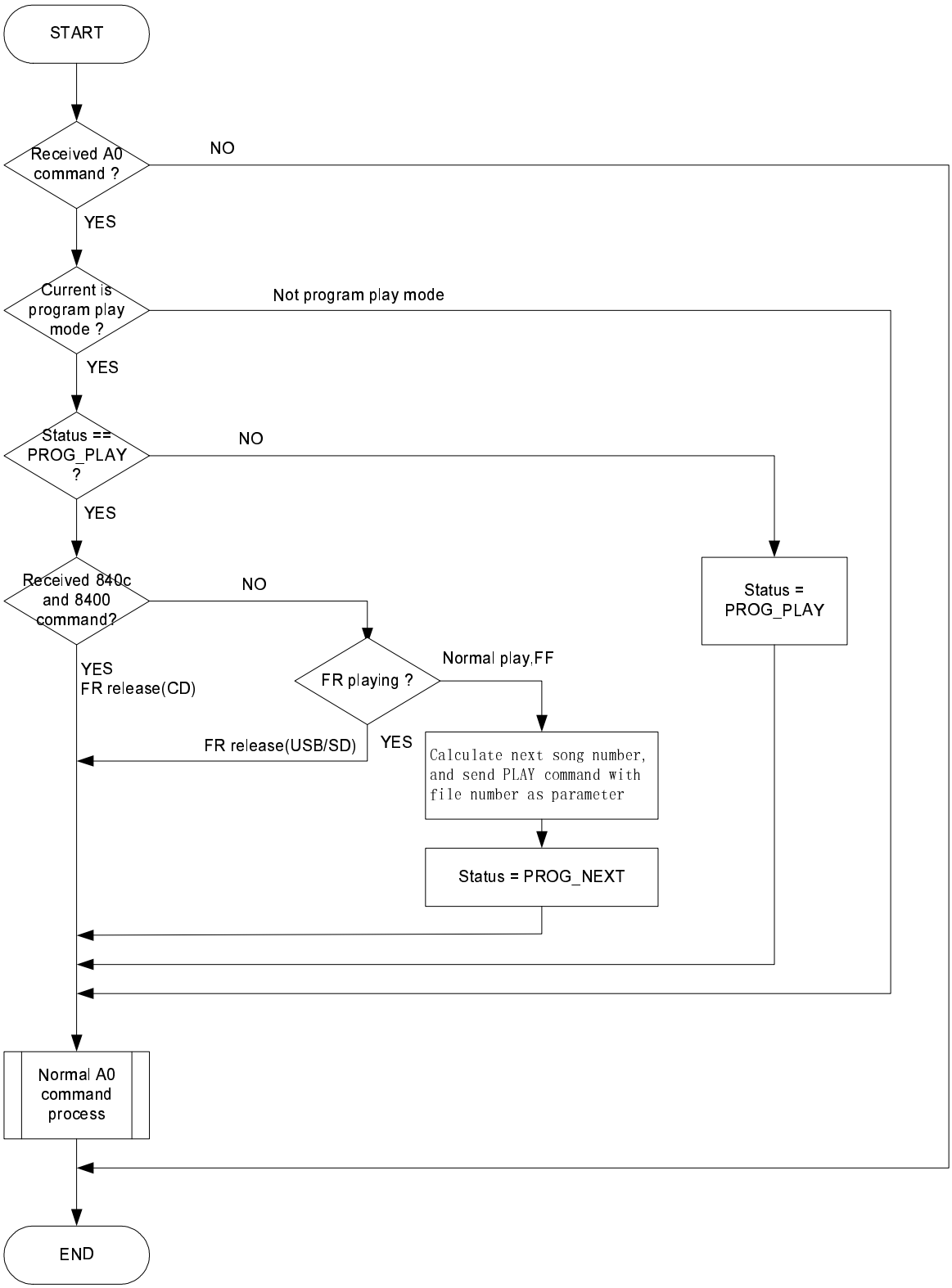

PROG_IDLE
Start program play(*note2)
Stop program play
PROG_PREP ARE
PROG_PLAY
Receive AO command in FR status. it means current song FR is auto released. don't need to process it. (*note3)
Received AO command in NEXT status. It means last play command is accepted.
UP, DOWN operation(*note1)
Auto change to NEXT state(*note1)
Receive AO command in play or FF status. It means current song playing is finished(*note1)
PROG_NEXT

*note1: calculate next program track number and send play command to BP3.
*note2: set BP3 to random_off mode and repeat_1 mode.
*note3: in FR case, USB/SD and CD is different. Please refer to following flowchart.

3. program start flow chart


START
send RANDOM_OFF command to BP3
send REPEAT_1 command to BP3
status=PROG_PREPARE
Calculate first song number, and Send PLAY command to BP3 with file number as parameter
status=PROG_NEXT
END

4. A0 command process flowchart



8 About characters coding

I nfo cod ng

f le	I nfo has types IS - - , TF- , TF- , TF- . In I command, there s one byte to nd cate the cod ng type
f le	TF- only

F le name foler name cod ng

-R	F le name or folder name s IS - - or TF- . There s one byte n command to nd cate the cod ng type.
S or S	F le name or folder name s s IS - - or TF- . There s one byte n command to nd cate the cod ng type.

Suggest on to these cod ngs

IS - -	ormally one byte nd cates one character. ut f th s byte s equal to or greater than , th s byte and ne t byte these two bytes nd cate one character.
TF-	n code str ng. Two bytes nd cate one character, t s l ttler end a. Somet mes, th s str ng beg n w th byte fffe, t ust means the the d rect on of h gh and low byte. ust sk p t and no need d splay.
TF-	n code str ng. Two bytes nd cate one character, t s b g end a. Somet mes, th s str ng beg n w th byte feff, t ust means the the d rect on of h gh and low byte. ust sk p t and no need d splay.
TF-	byte, byte or byte nd cates one character. For deta ls, please refer to TF- format.

-T T cod ng

In -T T related command bc, there s one byte nd cates -T T character set code. lack epper ust reports the or g nal code read from d sc. bout the character set code, refer to bellow table

	IS - -
	IS
	Sh ft- IS code apanese cod ng
	orean characters
	h nese characters
others	Refer to related spec f cat on

Revision history

Version	Date	Comment	In charge
1.0	2010-4-7	BlackPepper3 specification(first version)	(TLSZ)Yang Jiangfeng

TOSHIBA

8 Bit Microcontroller
TLCS-870/C Series

T5CL8

TOSHIBA CORPORATION

The information contained herein is subject to change without notice. 021023_D

TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress.
It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications.
Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc. 021023_A

The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.).
These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's own risk. 021023_B

The products described in this document shall not be used or embedded to any downstream products of which manufacture, use and/or sale are prohibited under any applicable laws and regulations. 060106_Q

The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA for any infringements of patents or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any patents or other rights of TOSHIBA or the third parties. 070122_C

The products described in this document are subject to foreign exchange and foreign trade control laws. 060925_E

For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions. 030619_S

© 2007 TOSHIBA CORPORATION
All Rights Reserved

Revision History

Date	Revision	
2008/7/31	1	First Release

Table of Contents

Differences among Products

T5CL8

1.1 Features 1
1.2 Pin Assignment 3
1.3 Block Diagram 4
1.4 Pin Names and Functions 5

2. Operational Description

2.1 CPU Core Functions 9
2.1.1 Memory Address Map 9
2.1.2 Program Memory (Flash) 9
2.1.3 Data Memory (RAM) 9
2.2 System Clock Controller 10
2.2.1 Clock Generator 10
2.2.2 Timing Generator 12
2.2.2.1 Configuration of timing generator
2.2.2.2 Machine cycle
2.2.3 Operation Mode Control Circuit 13
2.2.3.1 Single-clock mode
2.2.3.2 Dual-clock mode
2.2.3.3 STOP mode
2.2.4 Operating Mode Control 18
2.2.4.1 STOP mode
2.2.4.2 IDLE1/2 mode and SLEEP1/2 mode
2.2.4.3 IDLE0 and SLEEP0 modes (IDLE0, SLEEP0)
2.2.4.4 SLOW mode
2.3 Reset Circuit 31
2.3.1 External Reset Input 31
2.3.2 Address trap reset 32
2.3.3 Watchdog timer reset 32
2.3.4 System clock reset 32

3. Interrupt Control Circuit

3.1 Interrupt latches (IL23 to IL2) 35
3.2 Interrupt enable register (EIR) 36
3.2.1 Interrupt master enable flag (IMF) 36
3.2.2 Individual interrupt enable flags (EF23 to EF4) 37
Note 3: 38
3.3 Interrupt Sequence 39
3.3.1 Interrupt acceptance processing is packaged as follows. 39
3.3.2 Saving/restoring general-purpose registers 40
3.3.2.1 Using PUSH and POP instructions

3.3.2.2 Using data transfer instructions
3.3.3 Interrupt return ... 41
3.4 Software Interrupt (INTSW) ... 42
3.4.1 Address error detection ... 42
3.4.2 Debugging ... 42
3.5 Undefined Instruction Interrupt (INTUNDEF) ... 42
3.6 Address Trap Interrupt (INTATRAP) ... 42
3.7 External Interrupts ... 43

4. Special Function Register (SFR)

4.1 SFR ... 45
4.2 DBR ... 47

5. I/O Ports

5.1 Port P0 (P07 to P00) ... 50
5.2 Port P1 (P17 to P10) ... 52
5.3 Port P2 (P22 to P20) ... 54
5.4 Port P3 (P37 to P30) (Large Current Port) ... 55
5.5 Port P4 (P47 to P40) ... 56
5.6 Port P5 (P54 to P50) (Large Current Port) ... 58
5.7 Port P6 (P67 to P60) ... 59
5.8 Port P7 (P77 to P70) ... 62

6. Watchdog Timer (WDT)

6.1 Watchdog Timer Configuration ... 65
6.2 Watchdog Timer Control ... 66
6.2.1 Malfunction Detection Methods Using the Watchdog Timer ... 66
6.2.2 Watchdog Timer Enable ... 67
6.2.3 Watchdog Timer Disable ... 68
6.2.4 Watchdog Timer Interrupt (INTWDT) ... 68
6.2.5 Watchdog Timer Reset ... 69
6.3 Address Trap ... 70
6.3.1 Selection of Address Trap in Internal RAM (ATAS) ... 70
6.3.2 Selection of Operation at Address Trap (ATOUT) ... 70
6.3.3 Address Trap Interrupt (INTATRAP) ... 70
6.3.4 Address Trap Reset ... 71

7. Time Base Timer (TBT)

7.1 Time Base Timer ... 73
7.1.1 Configuration ... 73
7.1.2 Control ... 73
7.1.3 Function ... 74
7.2 Divider Output (DVO) ... 75
7.2.1 Configuration ... 75
7.2.2 Control ... 75

8. 16-Bit TimerCounter 1 (TC1)

8.1 Configuration 77
8.2 TimerCounter Control 78
8.3 Function 80
8.3.1 Timer mode 80
8.3.2 External Trigger Timer Mode 82
8.3.3 Event Counter Mode 84
8.3.4 Window Mode 85
8.3.5 Pulse Width Measurement Mode 86
8.3.6 Programmable Pulse Generate (PPG) Output Mode 89

9. 16-Bit Timer/Counter2 (TC2)

9.1 Configuration 93
9.2 Control 94
9.3 Function 95
9.3.1 Timer mode 95
9.3.2 Event counter mode 97
9.3.3 Window mode 97

10. 8-Bit TimerCounter (TC3, TC4)

10.1 Configuration 99
10.2 TimerCounter Control 100
10.3 Function 105
10.3.1 8-Bit Timer Mode (TC3 and 4) 105
10.3.2 8-Bit Event Counter Mode (TC3, 4) 106
10.3.3 8-Bit Programmable Divider Output (PDO) Mode (TC3, 4) 106
10.3.4 8-Bit Pulse Width Modulation (PWM) Output Mode (TC3, 4) 109
10.3.5 16-Bit Timer Mode (TC3 and 4) 111
10.3.6 16-Bit Event Counter Mode (TC3 and 4) 112
10.3.7 16-Bit Pulse Width Modulation (PWM) Output Mode (TC3 and 4) 112
10.3.8 16-Bit Programmable Pulse Generate (PPG) Output Mode (TC3 and 4) 115
10.3.9 Warm-Up Counter Mode 117
10.3.9.1 Low-Frequency Warm-up Counter Mode (NORMAL1 → NORMAL2 → SLOW2 → SLOW1)
10.3.9.2 High-Frequency Warm-Up Counter Mode (SLOW1 → SLOW2 → NORMAL2 → NORMAL1)

11. 8-Bit TimerCounter (TC5, TC6)

11.1 Configuration 119
11.2 TimerCounter Control 120
11.3 Function 125
11.3.1 8-Bit Timer Mode (TC5 and 6) 125
11.3.2 8-Bit Event Counter Mode (TC5, 6) 126
11.3.3 8-Bit Programmable Divider Output (PDO) Mode (TC5, 6) 126
11.3.4 8-Bit Pulse Width Modulation (PWM) Output Mode (TC5, 6) 129
11.3.5 16-Bit Timer Mode (TC5 and 6) 131
11.3.6 16-Bit Event Counter Mode (TC5 and 6) 132
11.3.7 16-Bit Pulse Width Modulation (PWM) Output Mode (TC5 and 6) 132
11.3.8 16-Bit Programmable Pulse Generate (PPG) Output Mode (TC5 and 6) 135
11.3.9 Warm-Up Counter Mode 137
11.3.9.1 Low-Frequency Warm-up Counter Mode

(NORMAL1 → NORMAL2 → SLOW2 → SLOW1)
11.3.9.2 High-Frequency Warm-Up Counter Mode
(SLOW1 → SLOW2 → NORMAL2 → NORMAL1)

12. Asynchronous Serial interface (UART1)

12.1 Configuration 139
12.2 Control 140
12.3 Transfer Data Format 142
12.4 Transfer Rate. 143
12.5 Data Sampling Method 143
12.6 STOP Bit Length 144
12.7 Parity 144
12.8 Transmit/Receive Operation 144
12.8.1 Data Transmit Operation 144
12.8.2 Data Receive Operation 144
12.9 Status Flag 145
12.9.1 Parity Error 145
12.9.2 Framing Error 145
12.9.3 Overrun Error 145
12.9.4 Receive Data Buffer Full 146
12.9.5 Transmit Data Buffer Empty 146
12.9.6 Transmit End Flag 147

13. Asynchronous Serial interface (UART2)

13.1 Configuration 149
13.2 Control 150
13.3 Transfer Data Format 152
13.4 Transfer Rate. 153
13.5 Data Sampling Method 153
13.6 STOP Bit Length 154
13.7 Parity 154
13.8 Transmit/Receive Operation 154
13.8.1 Data Transmit Operation 154
13.8.2 Data Receive Operation 154
13.9 Status Flag 155
13.9.1 Parity Error 155
13.9.2 Framing Error 155
13.9.3 Overrun Error 155
13.9.4 Receive Data Buffer Full 156
13.9.5 Transmit Data Buffer Empty 156
13.9.6 Transmit End Flag 157

14. Synchronous Serial Interface (SIO1)

14.1 Configuration 159
14.2 Control 160
14.3 Function 162
14.3.1 Serial clock 162
14.3.1.1 Clock source
14.3.1.2 Shift edge
14.3.2 Transfer bit direction 164
14.3.2.1 Transmit mode

14.3.2.2 Receive mode
14.3.2.3 Transmit/receive mode
14.3.3 Transfer modes ... 165
14.3.3.1 Transmit mode
14.3.3.2 Receive mode
14.3.3.3 Transmit/receive mode

15. Synchronous Serial Interface (SIO2)

15.1 Configuration ... 177
15.2 Control ... 178
15.3 Function ... 180
15.3.1 Serial clock ... 180
15.3.1.1 Clock source
15.3.1.2 Shift edge
15.3.2 Transfer bit direction ... 182
15.3.2.1 Transmit mode
15.3.2.2 Receive mode
15.3.2.3 Transmit/receive mode
15.3.3 Transfer modes ... 183
15.3.3.1 Transmit mode
15.3.3.2 Receive mode
15.3.3.3 Transmit/receive mode

16. Serial Bus Interface(I2C Bus) Ver.-D (SBI)

16.1 Configuration ... 195
16.2 Control ... 195
16.3 Software Reset ... 195
16.4 The Data Format in the I2C Bus Mode ... 196
16.5 I2C Bus Control ... 197
16.5.1 Acknowledgement mode specification ... 199
16.5.1.1 Acknowledgment mode (ACK = “1”)
16.5.1.2 Non-acknowledgment mode (ACK = “0”)
16.5.2 Number of transfer bits ... 200
16.5.3 Serial clock ... 200
16.5.3.1 Clock source
16.5.3.2 Clock synchronization
16.5.4 Slave address and address recognition mode specification ... 201
16.5.5 Master/slave selection ... 201
16.5.6 Transmitter/receiver selection ... 201
16.5.7 Start/stop condition generation ... 202
16.5.8 Interrupt service request and cancel ... 202
16.5.9 Setting of I2C bus mode ... 203
16.5.10 Arbitration lost detection monitor ... 203
16.5.11 Slave address match detection monitor ... 204
16.5.12 GENERAL CALL detection monitor ... 204
16.5.13 Last received bit monitor ... 204
16.6 Data Transfer of I2C Bus ... 205
16.6.1 Device initialization ... 205
16.6.2 Start condition and slave address generation ... 205
16.6.3 1-word data transfer ... 205
16.6.3.1 When the MST is “1” (Master mode)
16.6.3.2 When the MST is “0” (Slave mode)
16.6.4 Stop condition generation ... 208
16.6.5 Restart ... 209

17. 10-bit AD Converter (ADC)

17.1 Configuration ... 211

17.2 Register configuration 212
17.3 Function 215
17.3.1 Software Start Mode 215
17.3.2 Repeat Mode 215
17.3.3 Register Setting 216
17.4 STOP/SLOW Modes during AD Conversion 217
17.5 Analog Input Voltage and AD Conversion Result 218
17.6 Precautions about AD Converter 219
17.6.1 Restrictions for AD Conversion interrupt (INTADC) usage 219
17.6.2 Analog input pin voltage range 219
17.6.3 Analog input shared pins 219
17.6.4 Noise Countermeasure 219

18. Key-on Wakeup (KWU)

18.1 Configuration 221
18.2 Control 221
18.3 Function 221

19. Flash Memory

19.1 Flash Memory Control 224
19.1.1 Flash Memory Command Sequence Execution Control (FLSCR<FLSMD>) 224
19.1.2 Flash Memory Bank Select Control (FLSCR<BANKSEL>) 224
19.2 Command Sequence 225
19.2.1 Byte Program 225
19.2.2 Sector Erase (4-kbyte Erase) 225
19.2.3 Chip Erase (All Erase) 226
19.2.4 Product ID Entry 226
19.2.5 Product ID Exit 226
19.2.6 Security Program 226
19.3 Toggle Bit (D6) 227
19.4 Access to the Flash Memory Area 228
19.4.1 Flash Memory Control in the Serial PROM Mode 228
19.4.1.1 How to write to the flash memory by executing the control program in the RAM area (in the RAM loader mode within the serial PROM mode)
19.4.2 Flash Memory Control in the MCU mode 230
19.4.2.1 How to write to the flash memory by executing a user write control program in the RAM area (in the MCU mode)

20. Serial PROM Mode

20.1 Outline 233
20.2 Memory Mapping 233
20.3 Serial PROM Mode Setting 234
20.3.1 Serial PROM Mode Control Pins 234
20.3.2 Pin Function 234
20.3.3 Example Connection for On-Board Writing 235
20.3.4 Activating the Serial PROM Mode 236
20.4 Interface Specifications for UART 237
20.5 Operation Command 239
20.6 Operation Mode 239
20.6.1 Flash Memory Erasing Mode (Operating command: F0H) 241
20.6.2 Flash Memory Writing Mode (Operation command: 30H) 243
20.6.3 RAM Loader Mode (Operation Command: 60H) 246

20.6.4 Flash Memory SUM Output Mode (Operation Command: 90H) ... 248
20.6.5 Product ID Code Output Mode (Operation Command: C0H) ... 249
20.6.6 Flash Memory Status Output Mode (Operation Command: C3H) ... 251
20.6.7 Flash Memory security program Setting Mode (Operation Command: FAH) ... 252
20.7 Error Code ... 254
20.8 Checksum (SUM) ... 254
20.8.1 Calculation Method ... 254
20.8.2 Calculation data ... 255
20.9 Intel Hex Format (Binary) ... 256
20.10 Passwords ... 256
20.10.1 Password String ... 257
20.10.2 Handling of Password Error ... 257
20.10.3 Password Management during Program Development ... 257
20.11 Product ID Code ... 258
20.12 Flash Memory Status Code ... 258
20.13 Specifying the Erasure Area ... 260
20.14 Flowchart ... 261
20.15 UART Timing ... 262

21. Input/Output Circuit

21.1 Control pins ... 263
21.2 Input/Output Ports ... 264

22. Electrical Characteristics

22.1 Absolute Maximum Ratings ... 267
22.2 Operating Conditions ... 268
22.2.1 MCU mode (Flash Programming or erasing) ... 268
22.2.2 MCU mode (Except Flash Programming or erasing) ... 268
22.2.3 Serial PROM mode ... 269
22.3 DC Characteristics ... 270
22.4 AD Characteristics ... 272
22.5 AC Characteristics ... 273
22.6 Flash Characteristics ... 273
22.6.1 Write/Retention Characteristics ... 273
22.7 Recommended Oscillating Conditions ... 274
22.8 Handling Precaution ... 274

23. Package Dimensions

This is a technical document that describes the operating functions and electrical specifications of the 8-bit microcontroller series TLCS-870/C (LSI).

CMOS 8-Bit Microcontroller

T5CL8

The T5CL8 is a single-chip 8-bit high-speed and high-functionality microcomputer incorporating 61440 bytes of Flash Memory.

Product No.	ROM (FLASH)	RAM	Package	MaskROM MCU	Emulation Chip
T5CL8	61440 bytes	2048 bytes	LQFP64-P-1010-0.50D	-	-

1.1 Features

1. 8-bit single chip microcomputer TLCS-870/C series
   - Instruction execution time :

     0.25 μs (at 16 MHz)

     122 μs (at 32.768 kHz)
   - 132 types & 731 basic instructions
2. 24interrupt sources (External : 5 Internal : 19)
3. Input / Output ports (56 pins)

   Large current output: 13pins (Typ. 20mA), LED direct drive
4. Watchdog Timer
5. Prescaler
   - Time base timer
   - Divider output function
6. 16-bit timer counter: 1 ch
   - Timer, External trigger, Window, Pulse width measurement,

     Event counter, Programmable pulse generate (PPG) modes
7. 16-bit timer counter: 1 ch
   - Timer, Event counter, Window modes

This product uses the Super Flash® technology under the licence of Silicon Storage Technology, Inc. Super Flash® is registered trademark of Silicon Storage Technology, Inc.

- The information contained herein is subject to change without notice. 021023_D
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc. 021023_A
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's own risk. 021023_B
- The products described in this document shall not be used or embedded to any downstream products of which manufacture, use and/or sale are prohibited under any applicable laws and regulations. 060106_Q
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA for any infringements of patents or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any patents or other rights of TOSHIBA or the third parties. 070122_C
- The products described in this document are subject to foreign exchange and foreign trade control laws. 060925_E
- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions. 030619_S

8. 8-bit timer counter : 4 ch
   - Timer, Event counter, Programmable divider output (PDO),

     Pulse width modulation (PWM) output,

     Programmable pulse generation (PPG) modes
9. 8-bit UART : 2 ch
10. High-Speed SIO: 2ch
11. Serial Bus Interface(I^2C Bus): 1ch
12. 10-bit successive approximation type AD converter
    - Analog input: 16 ch
13. Key-on wakeup : 4 ch
14. Clock operation

    Single clock mode

    Dual clock mode
15. Low power consumption operation

    STOP mode: Oscillation stops. (Battery/Capacitor back-up.)

    SLOW1 mode: Low power consumption operation using low-frequency clock.(High-frequency clock stop.)

    SLOW2 mode: Low power consumption operation using low-frequency clock.(High-frequency clock oscillate.)

    IDLE0 mode: CPU stops, and only the Time-Based-Timer(TBT) on peripherals operate using high frequency clock. Release by falling edge of the source clock which is set by TBTCR<TBTCK>.

    IDLE1 mode: CPU stops and peripherals operate using high frequency clock. Release by interruputs(CPU restarts).

    IDLE2 mode: CPU stops and peripherals operate using high and low frequency clock. Release by interruputs. (CPU restarts).

    SLEEP0 mode: CPU stops, and only the Time-Based-Timer(TBT) on peripherals operate using low frequency clock.Release by falling edge of the source clock which is set by TBTCR<TBTCK>.

    SLEEP1 mode: CPU stops, and peripherals operate using low frequency clock. Release by interruput.(CPU restarts).

    SLEEP2 mode: CPU stops and peripherals operate using high and low frequency clock. Release by interruput.
16. Wide operation voltage:

    4.5 V to 5.5 V at 16MHz /32.768 kHz

    2.7 V to 5.5 V at 8 MHz /32.768 kHz

1.2 Pin Assignment

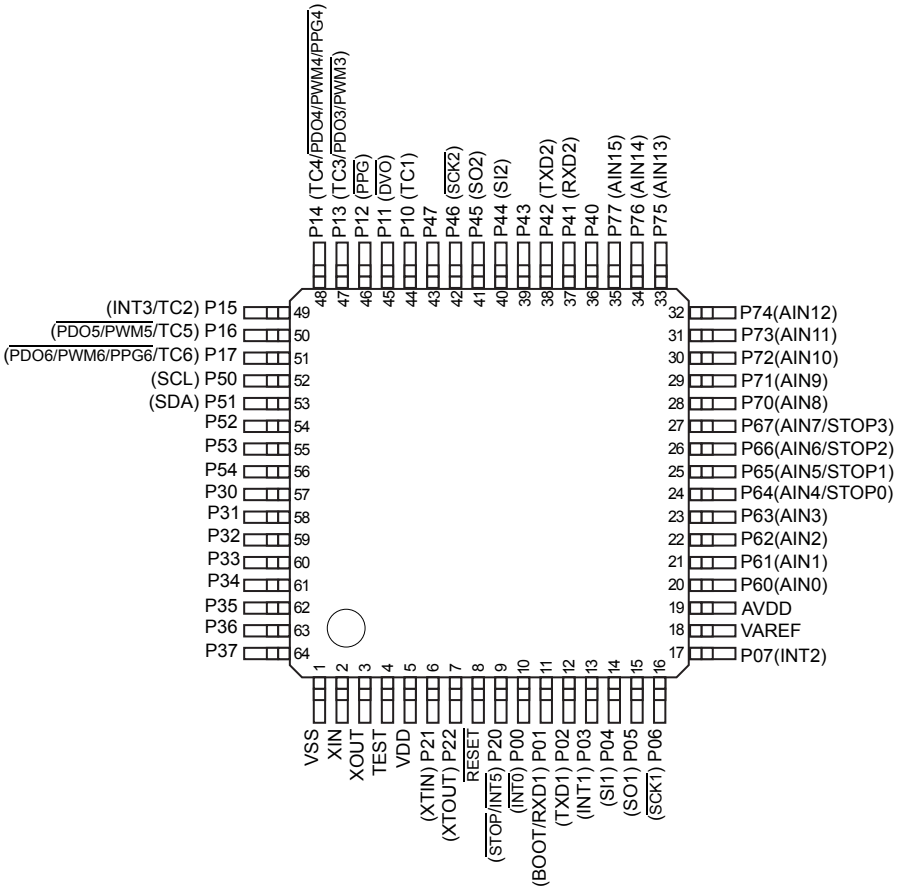


Figure 1-1 Pin Assignment

1.3 Block Diagram

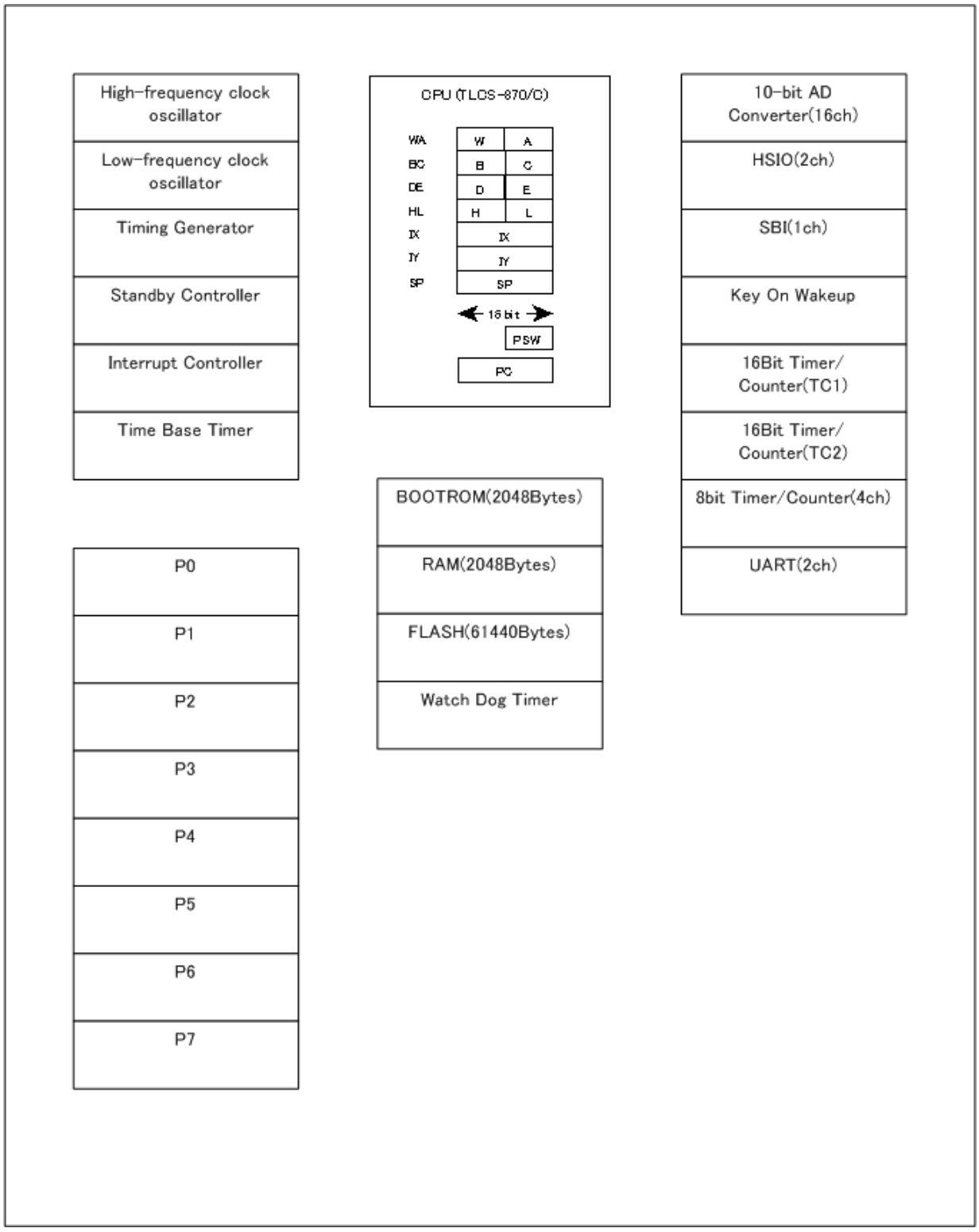


Figure 1-2 Block Diagram

1.4 Pin Names and Functions

The T5CL8 has MCU mode, parallel PROM mode, and serial PROM mode. Table 1-1 shows the pin functions in MCU mode. The serial PROM mode is explained later in a separate chapter.

Table 1-1 Pin Names and Functions(1/3)

Pin Name	Pin Number	Input/Output	Functions
P07 INT2	17	IO I	PORT07 External interrupt 2 input
P06 $\overline{\text{SCK1}}$	16	IO IO	PORT06 Serial clock input/output 1
P05 SO1	15	IO O	PORT05 Serial data output 1
P04 SI1	14	IO I	PORT04 Serial data input 1
P03 INT1	13	IO I	PORT03 External interrupt 1 input
P02 TXD1	12	IO O	PORT02 UART data output 1
P01 RXD1 BOOT	11	IO I I	PORT01 UART data input 1 Serial PROM mode control input
P00 $\overline{\text{INT0}}$	10	IO I	PORT00 External interrupt 0 input
P17 TC6 $\overline{\text{PDO6/PWM6/PPG6}}$	51	IO I O	PORT17 TC6 input PDO6/PWM6/PPG6 output
P16 TC5 $\overline{\text{PDO5/PWM5}}$	50	IO I O	PORT16 TC5 input PDO5/PWM5 output
P15 TC2 INT3	49	IO I I	PORT15 TC2 input External interrupt 3 input
P14 TC4 $\overline{\text{PDO4/PWM4/PPG4}}$	48	IO I O	PORT14 TC4 input PDO4/PWM4/PPG4 output
P13 TC3 $\overline{\text{PDO3/PWM3}}$	47	IO I O	PORT13 TC3 input PDO3/PWM3 output
P12 $\overline{\text{PPG}}$	46	IO O	PORT12 PPG output
P11 $\overline{\text{DVO}}$	45	IO O	PORT11 Divider Output
P10 TC1	44	IO I	PORT10 TC1 input
P22 XTOUT	7	IO O	PORT22 Resonator connecting pins(32.768kHz) for inputting external clock
P21 XTIN	6	IO I	PORT21 Resonator connecting pins(32.768kHz) for inputting external clock

Table 1-1 Pin Names and Functions(2/3)

Pin Name	Pin Number	Input/Output	Functions
P20 $\overline{\text{INT5}}$ $\overline{\text{STOP}}$	9	IO I I	PORT20 External interrupt 5 input STOP mode release signal input
P37	64	IO	PORT37
P36	63	IO	PORT36
P35	62	IO	PORT35
P34	61	IO	PORT34
P33	60	IO	PORT33
P32	59	IO	PORT32
P31	58	IO	PORT31
P30	57	IO	PORT30
P47	43	IO	PORT47
P46 $\overline{\text{SCK2}}$	42	IO IO	PORT46 Serial clock input/output 2
P45 SO2	41	IO O	PORT45 Serial data output 2
P44 SI2	40	IO I	PORT44 Serial data input 2
P43	39	IO	PORT43
P42 TXD2	38	IO O	PORT42 UART data output 2
P41 RXD2	37	IO I	PORT41 UART data input 2
P40	36	IO	PORT40
P54	56	IO	PORT54
P53	55	IO	PORT53
P52	54	IO	PORT52
P51 SDA	53	IO IO	PORT51 I2C bus data
P50 SCL	52	IO IO	PORT50 I2C bus clock
P67 AIN7 STOP3	27	IO I I	PORT67 Analog Input7 STOP3 input
P66 AIN6 STOP2	26	IO I I	PORT66 Analog Input6 STOP2 input
P65 AIN5 STOP1	25	IO I I	PORT65 Analog Input5 STOP1 input
P64 AIN4 STOP0	24	IO I I	PORT64 Analog Input4 STOP0 input

Table 1-1 Pin Names and Functions(3/3)

Pin Name	Pin Number	Input/Output	Functions
P63 AIN3	23	IO I	PORT63 Analog Input3
P62 AIN2	22	IO I	PORT62 Analog Input2
P61 AIN1	21	IO I	PORT61 Analog Input1
P60 AIN0	20	IO I	PORT60 Analog Input0
P77 AIN15	35	IO I	PORT77 Analog Input15
P76 AIN14	34	IO I	PORT76 Analog Input14
P75 AIN13	33	IO I	PORT75 Analog Input13
P74 AIN12	32	IO I	PORT74 Analog Input12
P73 AIN11	31	IO I	PORT73 Analog Input11
P72 AIN10	30	IO I	PORT72 Analog Input10
P71 AIN9	29	IO I	PORT71 Analog Input9
P70 AIN8	28	IO I	PORT70 Analog Input8
XIN	2	I	Resonator connecting pins for high-frequency clock
XOUT	3	O	Resonator connecting pins for high-frequency clock
$\overline{\text{RESET}}$	8	I	Reset signal
TEST	4	I	Test pin for out-going test. Normally, be fixed to low.
VAREF	18	I	Analog Base Voltage Input Pin for A/D Conversion
AVDD	19	I	Analog Power Supply
VDD	5	I	+5V
VSS	1	I	0(GND)

2. Operational Description

2.1 CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, and the reset circuit.

2.1.1 Memory Address Map

The T5CL8 memory is composed Flash, RAM, DBR(Data buffer register) and SFR(Special function register). They are all mapped in 64-Kbyte address space. Figure 2-1 shows the T5CL8 memory address map.

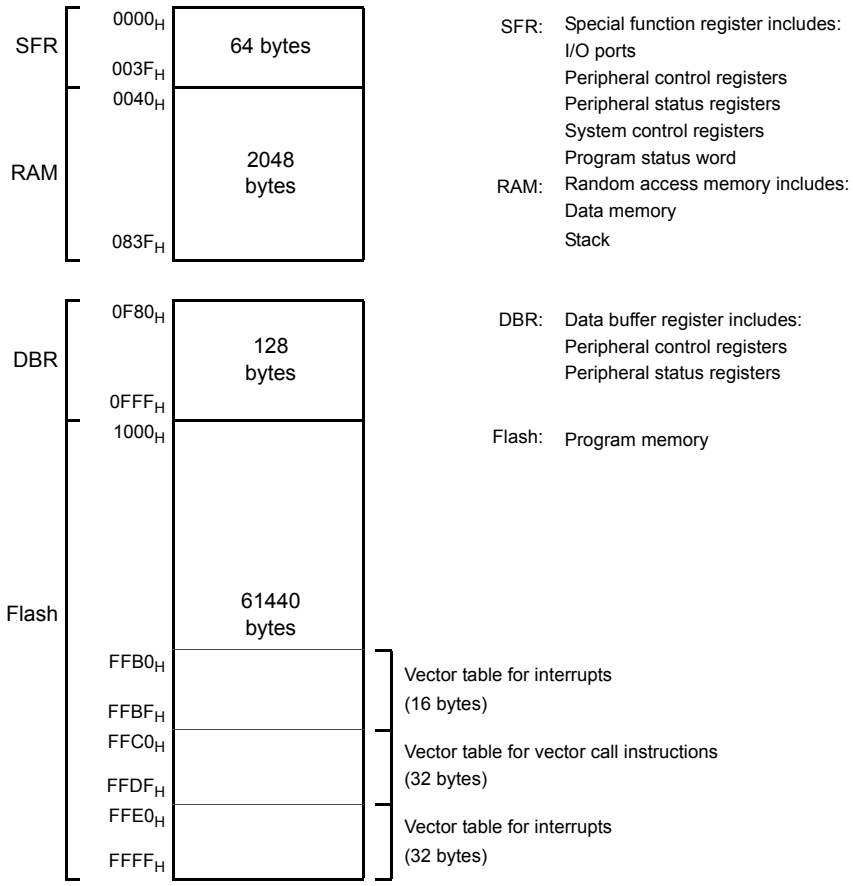


Figure 2-1 Memory Address Map

2.1.2 Program Memory (Flash)

The T5CL8 has a 61440 bytes (Address 1000H to FFFFH) of program memory (Flash).

2.1.3 Data Memory (RAM)

The T5CL8 has 2048 bytes (Address 0040H to 083FH) of internal RAM. The first 192 bytes (0040H to 00FFH) of the internal RAM are located in the direct area; instructions with shorten operations are available against such an area.

The data memory contents become unstable when the power supply is turned on; therefore, the data memory should be initialized by an initialization routine.

Example :Clears RAM to “00H”. (T5CL8)

```
        LD      HL, 0040H       ; Start address setup
        LD      A, H            ; Initial value (00H) setup
        LD      BC, 07FFH
SRAMCLR: LD     (HL), A
        INC     HL
        DEC     BC
        JRS     F, SRAMCLR
```

2.2 System Clock Controller

The system clock controller consists of a clock generator, a timing generator, and a standby controller.

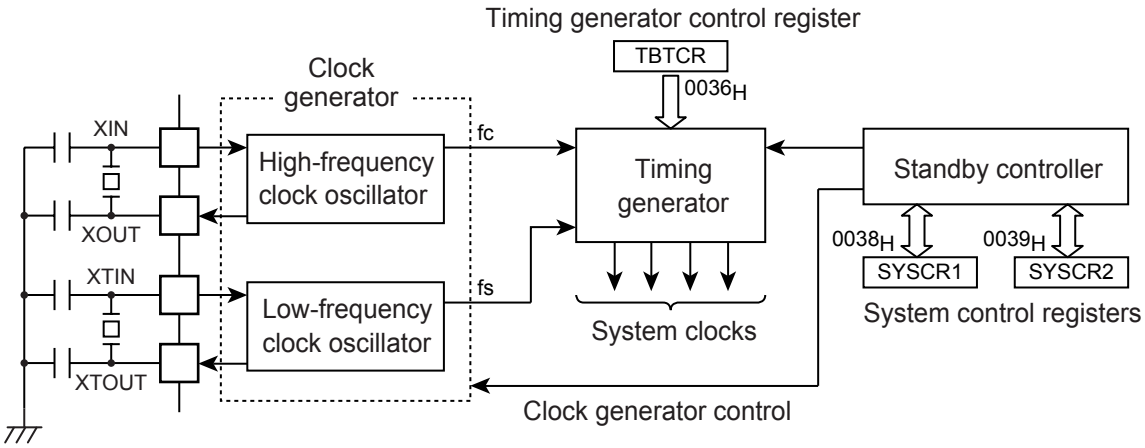


Figure 2-2 System Colck Control

2.2.1 Clock Generator

The clock generator generates the basic clock which provides the system clocks supplied to the CPU core and peripheral hardware. It contains two oscillation circuits: One for the high-frequency clock and one for the low-frequency clock. Power consumption can be reduced by switching of the standby controller to low-power operation based on the low-frequency clock.

The high-frequency (fc) clock and low-frequency (fs) clock can easily be obtained by connecting a resonator between the XIN/XOUT and XTIN/XTOUT pins respectively. Clock input from an external oscillator is also possible. In this case, external clock is applied to XIN/XTIN pin with XOUT/XTOUT pin not connected.

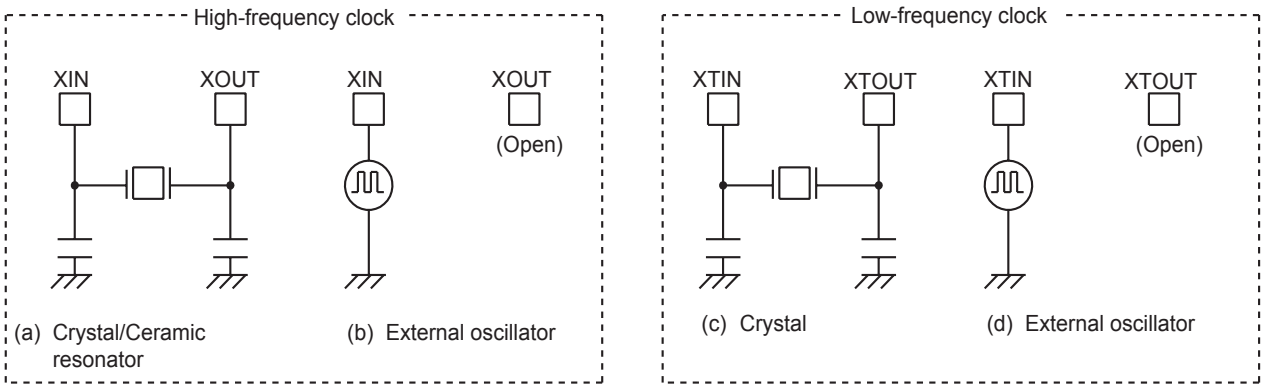


Figure 2-3 Examples of Resonator Connection

Note: The function to monitor the basic clock directly at external is not provided for hardware, however, with disabling all interrupts and watchdog timers, the oscillation frequency can be adjusted by monitoring the pulse which the fixed frequency is outputted to the port by the program.
The system to require the adjustment of the oscillation frequency should create the program for the adjustment in advance.

2.2.2 Timing Generator

The timing generator generates the various system clocks supplied to the CPU core and peripheral hardware from the basic clock (fc or fs). The timing generator provides the following functions.

1. Generation of main system clock
2. Generation of divider output ($\overline{\text{DVO}}$) pulses
3. Generation of source clocks for time base timer
4. Generation of source clocks for watchdog timer
5. Generation of internal source clocks for timer/counters
6. Generation of warm-up clocks for releasing STOP mode

2.2.2.1 Configuration of timing generator

The timing generator consists of a 2-stage prescaler, a 21-stage divider, a main system clock generator, and machine cycle counters.

An input clock to the 7th stage of the divider depends on the operating mode, SYSCR2<SYSCK> and TBTCR<DV7CK>, that is shown in Figure 2-4. As reset and STOP mode started/canceled, the prescaler and the divider are cleared to “0”.

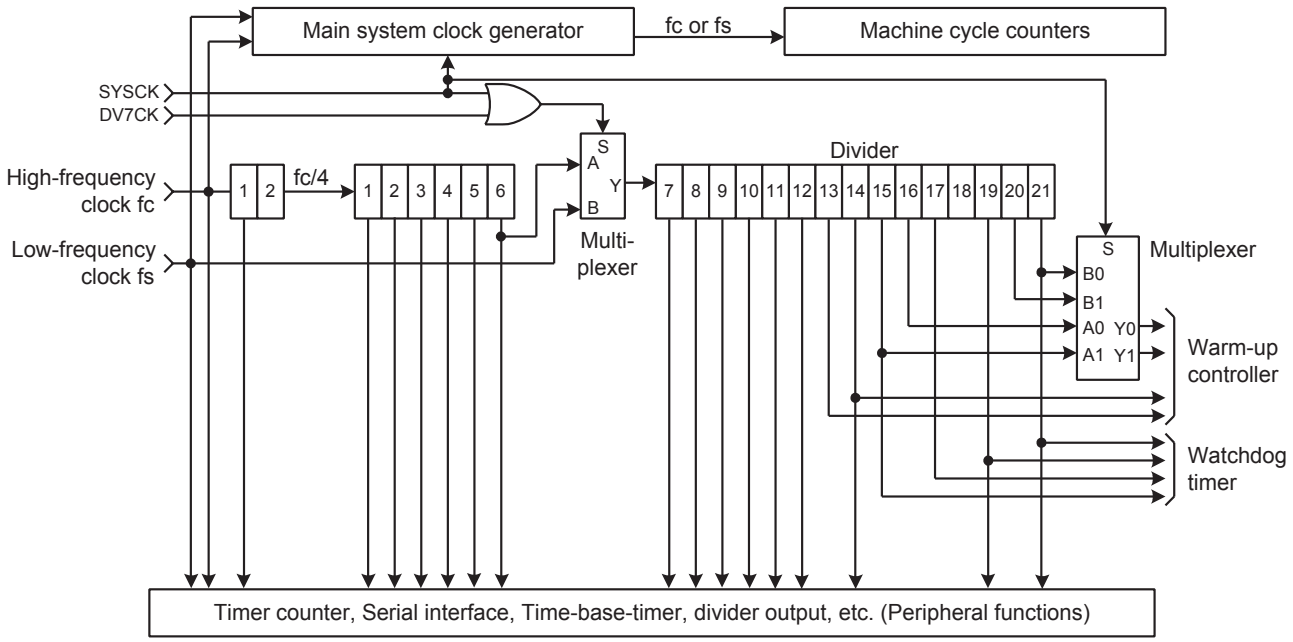


Figure 2-4 Configuration of Timing Generator

Timing Generator Control Register

TBTCR (0036H)

7	6	5	4	3	2	1	0	
(DVOEN)	(DVOCK)		DV7CK	(TBTEN)	(TBTCK)			(Initial value: 0000 0000)

DV7CK	Selection of input to the 7th stage of the divider	0: $fc/2^8$ [Hz] 1: fs	R/W

Note 1: In single clock mode, do not set DV7CK to "1".

Note 2: Do not set "1" on DV7CK while the low-frequency clock is not operated stably.

Note 3: fc: High-frequency clock [Hz], fs: Low-frequency clock [Hz], *: Don't care

Note 4: In SLOW1/2 and SLEEP1/2 modes, the DV7CK setting is ineffective, and fs is input to the 7th stage of the divider.

Note 5: When STOP mode is entered from NORMAL1/2 mode, the DV7CK setting is ineffective during the warm-up period after release of STOP mode, and the 6th stage of the divider is input to the 7th stage during this period.

2.2.2.2 Machine cycle

Instruction execution and peripheral hardware operation are synchronized with the main system clock.

The minimum instruction execution unit is called an "machine cycle". There are a total of 10 different types of instructions for the TLCS-870/C Series: Ranging from 1-cycle instructions which require one machine cycle for execution to 10-cycle instructions which require 10 machine cycles for execution. A machine cycle consists of 4 states (S0 to S3), and each state consists of one main system clock.

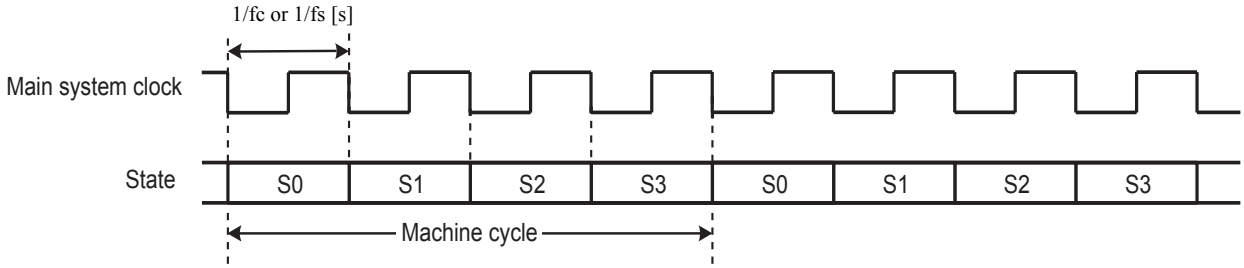


Figure 2-5 Machine Cycle

2.2.3 Operation Mode Control Circuit

The operation mode control circuit starts and stops the oscillation circuits for the high-frequency and low-frequency clocks, and switches the main system clock. There are three operating modes: Single clock mode, dual clock mode and STOP mode. These modes are controlled by the system control registers (SYSCR1 and SYSCR2). Figure 2-6 shows the operating mode transition diagram.

2.2.3.1 Single-clock mode

Only the oscillation circuit for the high-frequency clock is used, and P21 (XTIN) and P22 (XTOUT) pins are used as input/output ports. The main-system clock is obtained from the high-frequency clock. In the single-clock mode, the machine cycle time is 4/fc [s].

(1) NORMAL1 mode

In this mode, both the CPU core and on-chip peripherals operate using the high-frequency clock. The T5CL8 is placed in this mode after reset.

(2) IDLE1 mode

In this mode, the internal oscillation circuit remains active. The CPU and the watchdog timer are halted; however on-chip peripherals remain active (Operate using the high-frequency clock).

IDLE1 mode is started by SYSCR2<IDLE> = "1", and IDLE1 mode is released to NORMAL1 mode by an interrupt request from the on-chip peripherals or external interrupt inputs. When the IMF (Interrupt master enable flag) is “1” (Interrupt enable), the execution will resume with the acceptance of the interrupt, and the operation will return to normal after the interrupt service is completed. When the IMF is “0” (Interrupt disable), the execution will resume with the instruction which follows the IDLE1 mode start instruction.

(3) IDLE0 mode

In this mode, all the circuit, except oscillator and the timer-base-timer, stops operation.

This mode is enabled by SYSCR2<TGHALT> = "1".

When IDLE0 mode starts, the CPU stops and the timing generator stops feeding the clock to the peripheral circuits other than TBT. Then, upon detecting the falling edge of the source clock selected with TBTCR<TBTCK>, the timing generator starts feeding the clock to all peripheral circuits.

When returned from IDLE0 mode, the CPU restarts operating, entering NORMAL1 mode back again. IDLE0 mode is entered and returned regardless of how TBTCR<TBTEN> is set. When IMF = “1”, EF7 (TBT interrupt individual enable flag) = “1”, and TBTCR<TBTEN> = “1”, interrupt processing is performed. When IDLE0 mode is entered while TBTCR<TBTEN> = “1”, the INTTBT interrupt latch is set after returning to NORMAL1 mode.

2.2.3.2 Dual-clock mode

Both the high-frequency and low-frequency oscillation circuits are used in this mode. P21 (XTIN) and P22 (XTOUT) pins cannot be used as input/output ports. The main system clock is obtained from the high-frequency clock in NORMAL2 and IDLE2 modes, and is obtained from the low-frequency clock in SLOW and SLEEP modes. The machine cycle time is 4/fc [s] in the NORMAL2 and IDLE2 modes, and 4/fs [s] (122 μs at fs = 32.768 kHz) in the SLOW and SLEEP modes.

The TLCS-870/C is placed in the signal-clock mode during reset. To use the dual-clock mode, the low-frequency oscillator should be turned on at the start of a program.

(1) NORMAL2 mode

In this mode, the CPU core operates with the high-frequency clock. On-chip peripherals operate using the high-frequency clock and/or low-frequency clock.

(2) SLOW2 mode

In this mode, the CPU core operates with the low-frequency clock, while both the high-frequency clock and the low-frequency clock are operated. As the SYSCR2<SYSCK> becomes "1", the hardware changes into SLOW2 mode. As the SYSCR2<SYSCK> becomes “0”, the hardware changes into NORMAL2 mode. As the SYSCR2<XEN> becomes “0”, the hardware changes into SLOW1 mode. Do not clear SYSCR2<XTEN> to “0” during SLOW2 mode.

(3) SLOW1 mode

This mode can be used to reduce power-consumption by turning off oscillation of the high-frequency clock. The CPU core and on-chip peripherals operate using the low-frequency clock.

Switching back and forth between SLOW1 and SLOW2 modes are performed by SYSCR2<XEN>. In SLOW1 and SLEEP modes, the input clock to the 1st stage of the divider is stopped; output from the 1st to 6th stages is also stopped.

(4) IDLE2 mode

In this mode, the internal oscillation circuit remain active. The CPU and the watchdog timer are halted; however, on-chip peripherals remain active (Operate using the high-frequency clock and/or the low-frequency clock). Starting and releasing of IDLE2 mode are the same as for IDLE1 mode, except that operation returns to NORMAL2 mode.

(5) SLEEP1 mode

In this mode, the internal oscillation circuit of the low-frequency clock remains active. The CPU, the watchdog timer, and the internal oscillation circuit of the high-frequency clock are halted; however, on-chip peripherals remain active (Operate using the low-frequency clock). Starting and releasing of SLEEP mode are the same as for IDLE1 mode, except that operation returns to SLOW1 mode. In SLOW1 and SLEEP1 modes, the input clock to the 1st stage of the divider is stopped; output from the 1st to 6th stages is also stopped.

(6) SLEEP2 mode

The SLEEP2 mode is the idle mode corresponding to the SLOW2 mode. The status under the SLEEP2 mode is same as that under the SLEEP1 mode, except for the oscillation circuit of the high-frequency clock.

(7) SLEEP0 mode

In this mode, all the circuit, except oscillator and the timer-base-timer, stops operation. This mode is enabled by setting “1” on bit SYSCR2<TGHALT>.

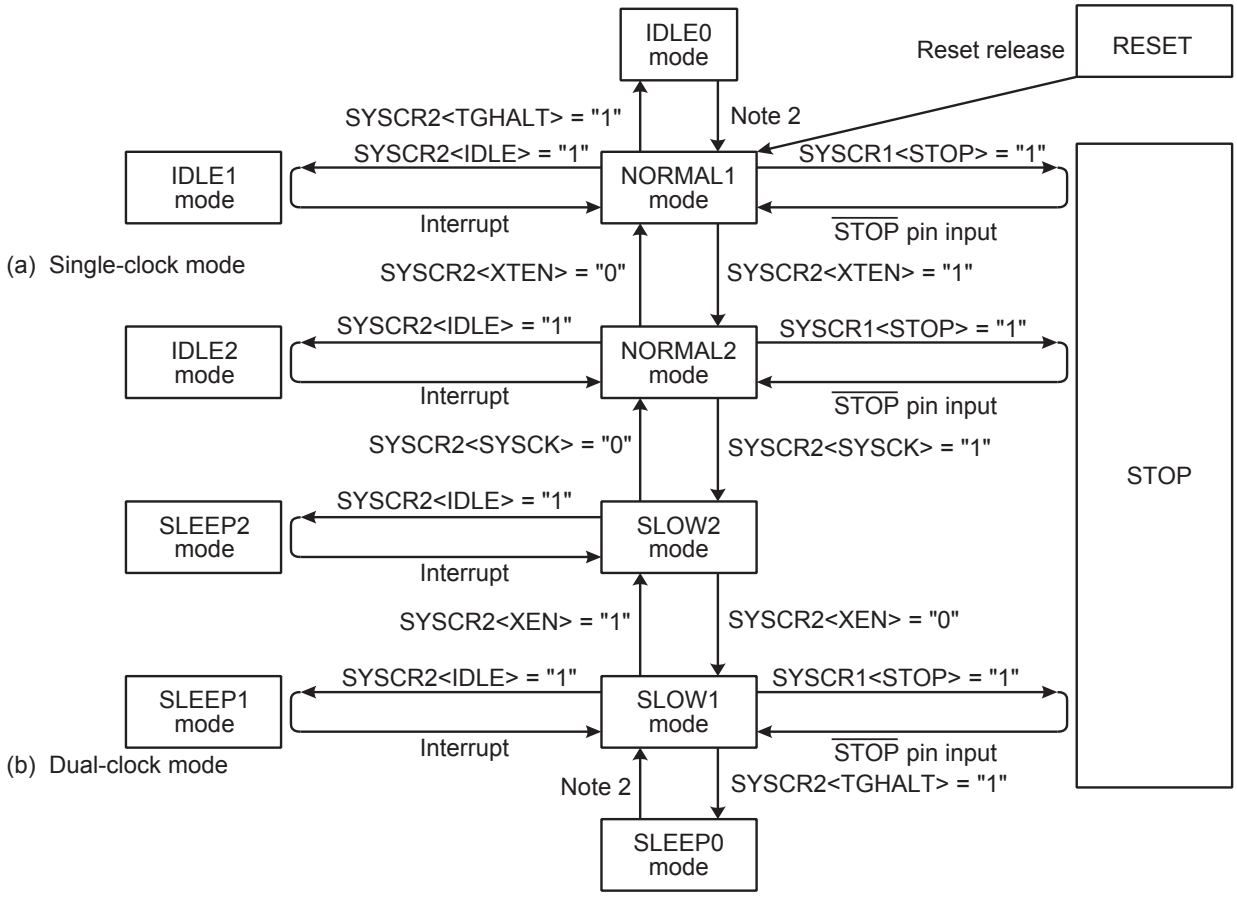
When SLEEP0 mode starts, the CPU stops and the timing generator stops feeding the clock to the peripheral circuits other than TBT. Then, upon detecting the falling edge of the source clock selected with TBTCR<TBTCK>, the timing generator starts feeding the clock to all peripheral circuits.

When returned from SLEEP0 mode, the CPU restarts operating, entering SLOW1 mode back again. SLEEP0 mode is entered and returned regardless of how TBTCR<TBTEN> is set. When IMF = “1”, EF7 (TBT interrupt individual enable flag) = “1”, and TBTCR<TBTEN> = “1”, interrupt processing is performed. When SLEEP0 mode is entered while TBTCR<TBTEN> = “1”, the INTTBT interrupt latch is set after returning to SLOW1 mode.

2.2.3.3 STOP mode

In this mode, the internal oscillation circuit is turned off, causing all system operations to be halted. The internal status immediately prior to the halt is held with a lowest power consumption during STOP mode.

STOP mode is started by the system control register 1 (SYSCR1), and STOP mode is released by a inputting (Either level-sensitive or edge-sensitive can be programmably selected) to the $\overline{\text{STOP}}$ pin. After the warm-up period is completed, the execution resumes with the instruction which follows the STOP mode start instruction.



Note 1: NORMAL1 and NORMAL2 modes are generically called NORMAL; SLOW1 and SLOW2 are called SLOW; IDLE0, IDLE1 and IDLE2 are called IDLE; SLEEP0, SLEEP1 and SLEEP2 are called SLEEP.

Note 2: The mode is released by falling edge of TBTCR<TBTCK> setting.

Figure 2-6 Operating Mode Transition Diagram

Table 2-1 Operating Mode and Conditions

Operating Mode		Oscillator		CPU Core	TBT	Other Peripherals	Machine Cycle Time
		High Frequency	Low Frequency				
Single clock	RESET	Oscillation	Stop	Reset	Reset	Reset	4/fc [s]
	NORMAL1			Operate	Operate	Operate	
	IDLE1			Halt			
	IDLE0					Halt	
	STOP	Stop			Halt		–
Dual clock	NORMAL2	Oscillation	Oscillation	Operate with high frequency	Operate	Operate	4/fc [s]
	IDLE2			Halt			
	SLOW2			Operate with low frequency			4/fs [s]
	SLEEP2			Halt			
	SLOW1	Stop		Operate with low frequency			
	SLEEP1			Halt			
	SLEEP0					Halt	
	STOP		Stop		Halt		–

System Control Register 1

SYSCR1 (0038H)

7	6	5	4	3	2	1	0
STOP	RELM	RETM	OUTEN	WUT			

(Initial value: 0000 00**)

STOP	STOP mode start	0: CPU core and peripherals remain active 1: CPU core and peripherals are halted (Start STOP mode)			R/W
RELM	Release method for STOP mode	0: Edge-sensitive release 1: Level-sensitive release			R/W
RETM	Operating mode after STOP mode	0: Return to NORMAL1/2 mode 1: Return to SLOW1 mode			R/W
OUTEN	Port output during STOP mode	0: High impedance 1: Output kept			R/W
WUT	Warm-up time at releasing STOP mode		Return to NORMAL mode	Return to SLOW mode	R/W
		00	3×2^{16}/fc	3×2^{13}/fs	
		01	2^{16}/fc	2^{13}/fs	
		10	3×2^{14}/fc	3×2^{6}/fs	
		11	2^{14}/fc	2^{6}/fs	

Note 1: Always set RETM to “0” when transiting from NORMAL mode to STOP mode. Always set RETM to “1” when transiting from SLOW mode to STOP mode.

Note 2: When STOP mode is released with $\overline{\text{RESET}}$ pin input, a return is made to NORMAL1 regardless of the RETM contents.

Note 3: fc: High-frequency clock [Hz], fs: Low-frequency clock [Hz], *; Don’t care

Note 4: Bits 1 and 0 in SYSCR1 are read as undefined data when a read instruction is executed.

Note 5: As the hardware becomes STOP mode under OUTEN = “0”, input value is fixed to “0”; therefore it may cause external interrupt request on account of falling edge.

Note 6: When the key-on wakeup is used, RELM should be set to "1".

Note 7: Port P20 is used as $\overline{\text{STOP}}$ pin. Therefore, when stop mode is started, OUTEN does not affect to P20, and P20 becomes High-Z mode.

Note 8: The warmig-up time should be set correctly for using oscillator.

System Control Register 2

SYSCR2 (0039H)

7	6	5	4	3	2	1	0
XEN	XTEN	SYSCK	IDLE		TGHALT		

(Initial value: 1000 *0**)

XEN	High-frequency oscillator control	0: Turn off oscillation 1: Turn on oscillation	R/W
XTEN	Low-frequency oscillator control	0: Turn off oscillation 1: Turn on oscillation	
SYSCK	Main system clock select (Write)/main system clock monitor (Read)	0: High-frequency clock (NORMAL1/NORMAL2/IDLE1/IDLE2) 1: Low-frequency clock (SLOW1/SLOW2/SLEEP1/SLEEP2)	
IDLE	CPU and watchdog timer control (IDLE1/2 and SLEEP1/2 modes)	0: CPU and watchdog timer remain active 1: CPU and watchdog timer are stopped (Start IDLE1/2 and SLEEP1/2 modes)	R/W
TGHALT	TG control (IDLE0 and SLEEP0 modes)	0: Feeding clock to all peripherals from TG 1: Stop feeding clock to peripherals except TBT from TG. (Start IDLE0 and SLEEP0 modes)	

Note 1: A reset is applied if both XEN and XTEN are cleared to “0”, XEN is cleared to “0” when SYSCK = “0”, or XTEN is cleared to “0” when SYSCK = “1”.

Note 2: *: Don’t care, TG: Timing generator, *; Don’t care

Note 3: Bits 3, 1 and 0 in SYSCR2 are always read as undefined value.

Note 4: Do not set IDLE and TGHALT to “1” simultaneously.

Note 5: Because returning from IDLE0/SLEEP0 to NORMAL1/SLOW1 is executed by the asynchronous internal clock, the period of IDLE0/SLEEP0 mode might be shorter than the period setting by TBTCR<TBTCK>.

Note 6: When IDLE1/2 or SLEEP1/2 mode is released, IDLE is automatically cleared to “0”.

Note 7: When IDLE0 or SLEEP0 mode is released, TGHALT is automatically cleared to “0”.

Note 8: Before setting TGHALT to “1”, be sure to stop peripherals. If peripherals are not stopped, the interrupt latch of peripherals may be set after IDLE0 or SLEEP0 mode is released.

2.2.4 Operating Mode Control

2.2.4.1 STOP mode

STOP mode is controlled by the system control register 1, the $\overline{\text{STOP}}$ pin input and key-on wakeup input (STOP3 to STOP0) which is controlled by the STOP mode release control register (STOPCR).
The $\overline{\text{STOP}}$ pin is also used both as a port P20 and an $\overline{\text{INT5}}$ (external interrupt input 5) pin. STOP mode is started by setting SYSCR1<STOP> to "1". During STOP mode, the following status is maintained.

1. Oscillations are turned off, and all internal operations are halted.
2. The data memory, registers, the program status word and port output latches are all held in the status in effect before STOP mode was entered.
3. The prescaler and the divider of the timing generator are cleared to "0".
4. The program counter holds the address 2 ahead of the instruction (e.g., [SET (SYSCR1).7]) which started STOP mode.

STOP mode includes a level-sensitive mode and an edge-sensitive mode, either of which can be selected with the SYSCR1<RELM>. Do not use any key-on wakeup input (STOP3 to STOP0) for releasing STOP mode in edge-sensitive mode.

Note 1: The STOP mode can be released by either the STOP or key-on wakeup pin (STOP3 to STOP0). However, because the STOP pin is different from the key-on wakeup and can not inhibit the release input, the STOP pin must be used for releasing STOP mode.

Note 2: During STOP period (from start of STOP mode to end of warm up), due to changes in the external interrupt pin signal, interrupt latches may be set to "1" and interrupts may be accepted immediately after STOP mode is released. Before starting STOP mode, therefore, disable interrupts. Also, before enabling interrupts after STOP mode is released, clear unnecessary interrupt latches.

(1) Level-sensitive release mode (RELM = "1")

In this mode, STOP mode is released by setting the $\overline{\text{STOP}}$ pin high or setting the STOP3 to STOP0 pin input which is enabled by STOPCR. This mode is used for capacitor backup when the main power supply is cut off and long term battery backup.

Even if an instruction for starting STOP mode is executed while $\overline{\text{STOP}}$ pin input is high or STOP3 to STOP0 input is low, STOP mode does not start but instead the warm-up sequence starts immediately. Thus, to start STOP mode in the level-sensitive release mode, it is necessary for the program to first confirm that the $\overline{\text{STOP}}$ pin input is low or STOP3 to STOP0 input is high. The following two methods can be used for confirmation.

1. Testing a port.
2. Using an external interrupt input $\overline{\text{INT5}}$ ($\overline{\text{INT5}}$ is a falling edge-sensitive input).

Example 1 :Starting STOP mode from NORMAL mode by testing a port P20.

```
        LD      (SYSCR1), 01010000B     ; Sets up the level-sensitive release mode
SSTOPH: TEST    (P2PRD). 0              ; Wait until the STOP pin input goes low level
        JRS     F, SSTOPH
        DI                              ; IMF ← 0
        SET     (SYSCR1). 7             ; Starts STOP mode
```

Example 2 :Starting STOP mode from NORMAL mode with an INT5 interrupt.

```
PINT5:    TEST    (P2PRD). 0          ; To reject noise, STOP mode does not start if
          JRS     F, SINT5              port P20 is at high
          LD      (SYSCR1), 01010000B ; Sets up the level-sensitive release mode.
          DI                          ; IMF ← 0
          SET     (SYSCR1). 7         ; Starts STOP mode
SINT5:    RETI
```

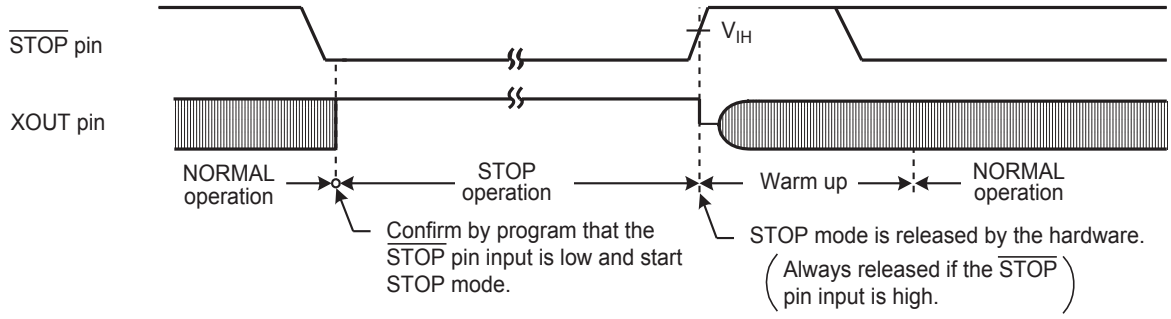

STOP pin
XOUT pin
VIH
NORMAL operation
STOP operation
Warm up
NORMAL operation
Confirm by program that the STOP pin input is low and start STOP mode.
STOP mode is released by the hardware.
(Always released if the STOP pin input is high.)

Figure 2-7 Level-sensitive Release Mode

Note 1: Even if the $\overline{\text{STOP}}$ pin input is low after warm-up start, the STOP mode is not restarted.

Note 2: In this case of changing to the level-sensitive mode from the edge-sensitive mode, the release mode is not switched until a rising edge of the $\overline{\text{STOP}}$ pin input is detected.

(2) Edge-sensitive release mode (RELM = “0”)

In this mode, STOP mode is released by a rising edge of the $\overline{\text{STOP}}$ pin input. This is used in applications where a relatively short program is executed repeatedly at periodic intervals. This periodic signal (for example, a clock from a low-power consumption oscillator) is input to the $\overline{\text{STOP}}$ pin. In the edge-sensitive release mode, STOP mode is started even when the $\overline{\text{STOP}}$ pin input is high level. Do not use any STOP3 to STOP0 pin input for releasing STOP mode in edge-sensitive release mode.

Example :Starting STOP mode from NORMAL mode

```
          DI                          ; IMF ← 0
          LD      (SYSCR1), 10010000B ; Starts after specified to the edge-sensitive release mode
```

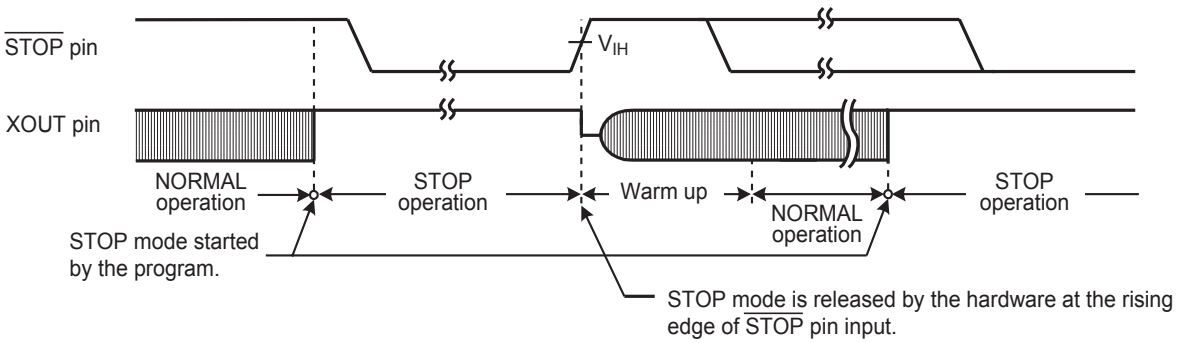


Figure 2-8 Edge-sensitive Release Mode

STOP mode is released by the following sequence.

1. In the dual-clock mode, when returning to NORMAL2, both the high-frequency and low-frequency clock oscillators are turned on; when returning to SLOW1 mode, only the low-frequency clock oscillator is turned on. In the single-clock mode, only the high-frequency clock oscillator is turned on.
2. A warm-up period is inserted to allow oscillation time to stabilize. During warm up, all internal operations remain halted. Four different warm-up times can be selected with the SYSCR1<WUT> in accordance with the resonator characteristics.
3. When the warm-up time has elapsed, normal operation resumes with the instruction following the STOP mode start instruction.

Note 1: When the STOP mode is released, the start is made after the prescaler and the divider of the timing generator are cleared to "0".

Note 2: STOP mode can also be released by inputting low level on the $\overline{\text{RESET}}$ pin, which immediately performs the normal reset operation.

Note 3: When STOP mode is released with a low hold voltage, the following cautions must be observed. The power supply voltage must be at the operating voltage level before releasing STOP mode. The $\overline{\text{RESET}}$ pin input must also be “H” level, rising together with the power supply voltage. In this case, if an external time constant circuit has been connected, the $\overline{\text{RESET}}$ pin input voltage will increase at a slower pace than the power supply voltage. At this time, there is a danger that a reset may occur if input voltage level of the $\overline{\text{RESET}}$ pin drops below the non-inverting high-level input voltage (Hysteresis input).

Table 2-2 Warm-up Time Example (at fc = 16.0 MHz, fs = 32.768 kHz)

WUT	Warm-up Time [ms]	
	Return to NORMAL Mode	Return to SLOW Mode
00	12.288	750
01	4.096	250
10	3.072	5.85
11	1.024	1.95

Note 1: The warm-up time is obtained by dividing the basic clock by the divider. Therefore, the warm-up time may include a certain amount of error if there is any fluctuation of the oscillation frequency when STOP mode is released. Thus, the warm-up time must be considered as an approximate value.

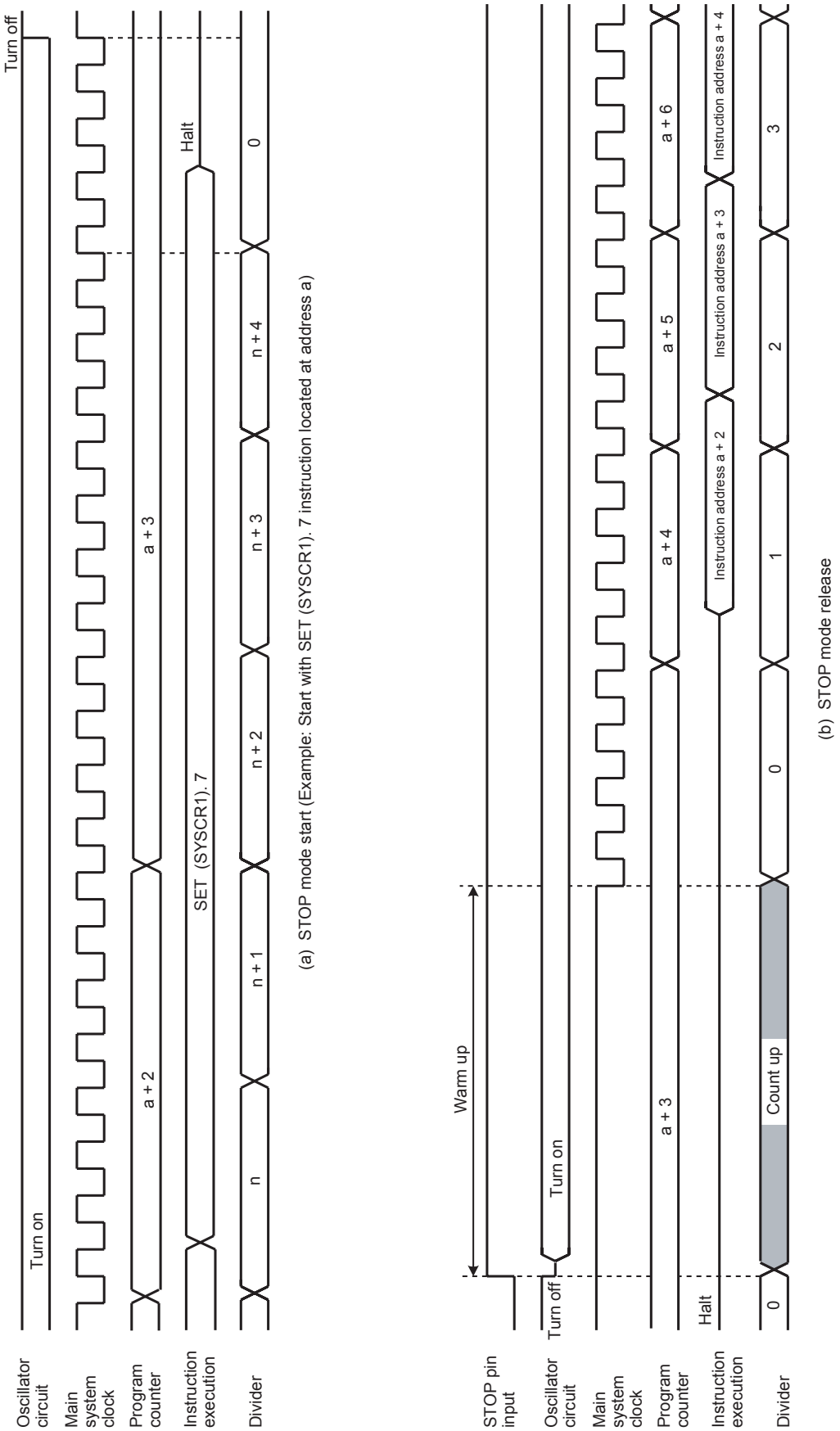


Figure 2-9 STOP Mode Start/Release

2.2.4.2 IDLE1/2 mode and SLEEP1/2 mode

IDLE1/2 and SLEEP1/2 modes are controlled by the system control register 2 (SYSCR2) and maskable interrupts. The following status is maintained during these modes.

1. Operation of the CPU and watchdog timer (WDT) is halted. On-chip peripherals continue to operate.
2. The data memory, CPU registers, program status word and port output latches are all held in the status in effect before these modes were entered.
3. The program counter holds the address 2 ahead of the instruction which starts these modes.

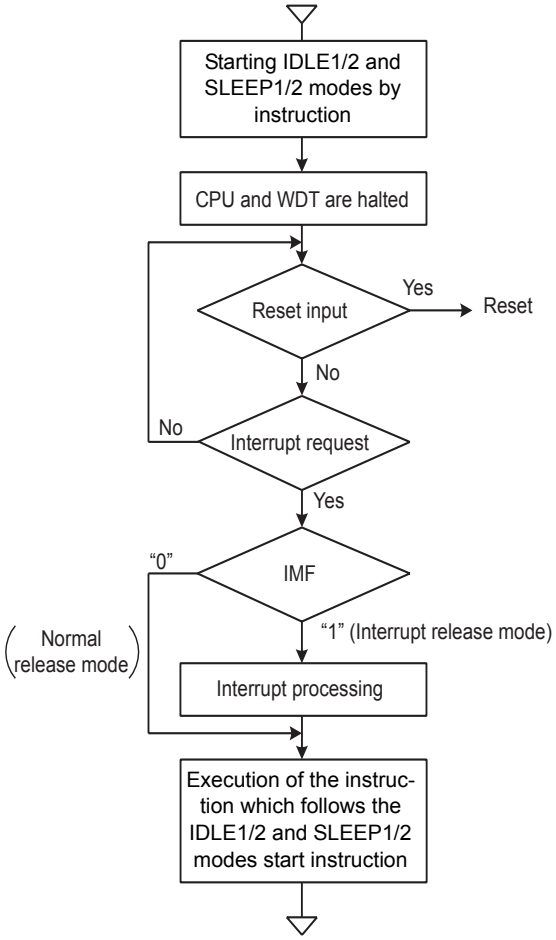


Figure 2-10 IDLE1/2 and SLEEP1/2 Modes

- Start the IDLE1/2 and SLEEP1/2 modes

  After IMF is set to "0", set the individual interrupt enable flag (EF) which releases IDLE1/2 and SLEEP1/2 modes. To start IDLE1/2 and SLEEP1/2 modes, set SYSCR2<IDLE> to “1”.

- Release the IDLE1/2 and SLEEP1/2 modes

  IDLE1/2 and SLEEP1/2 modes include a normal release mode and an interrupt release mode. These modes are selected by interrupt master enable flag (IMF). After releasing IDLE1/2 and SLEEP1/2 modes, the SYSCR2<IDLE> is automatically cleared to “0” and the operation mode is returned to the mode preceding IDLE1/2 and SLEEP1/2 modes.

  IDLE1/2 and SLEEP1/2 modes can also be released by inputting low level on the $\overline{\text{RESET}}$ pin. After releasing reset, the operation mode is started from NORMAL1 mode.

(1) Normal release mode (IMF = “0”)

IDLE1/2 and SLEEP1/2 modes are released by any interrupt source enabled by the individual interrupt enable flag (EF). After the interrupt is generated, the program operation is resumed from the instruction following the IDLE1/2 and SLEEP1/2 modes start instruction. Normally, the interrupt latches (IL) of the interrupt source used for releasing must be cleared to “0” by load instructions.

(2) Interrupt release mode (IMF = “1”)

IDLE1/2 and SLEEP1/2 modes are released by any interrupt source enabled with the individual interrupt enable flag (EF) and the interrupt processing is started. After the interrupt is processed, the program operation is resumed from the instruction following the instruction, which starts IDLE1/2 and SLEEP1/2 modes.

Note: When a watchdog timer interrupts is generated immediately before IDLE1/2 and SLEEP1/2 modes are started, the watchdog timer interrupt will be processed but IDLE1/2 and SLEEP1/2 modes will not be started.

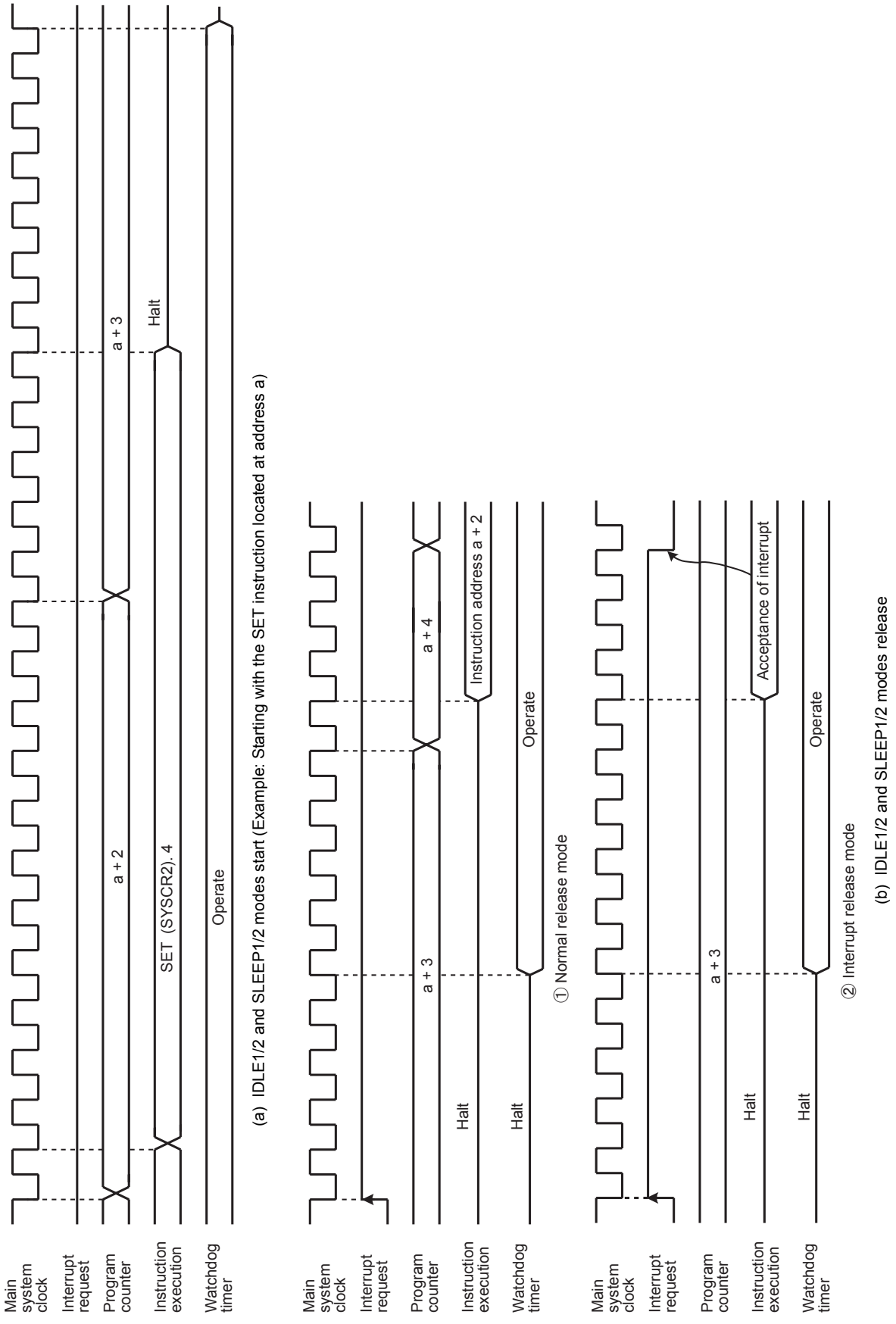


Figure 2-11 IDLE1/2 and SLEEP1/2 Modes Start/Release

2.2.4.3 IDLE0 and SLEEP0 modes (IDLE0, SLEEP0)

IDLE0 and SLEEP0 modes are controlled by the system control register 2 (SYSCR2) and the time base timer control register (TBTCR). The following status is maintained during IDLE0 and SLEEP0 modes.

1. Timing generator stops feeding clock to peripherals except TBT.
2. The data memory, CPU registers, program status word and port output latches are all held in the status in effect before IDLE0 and SLEEP0 modes were entered.
3. The program counter holds the address 2 ahead of the instruction which starts IDLE0 and SLEEP0 modes.

Note: Before starting IDLE0 or SLEEP0 mode, be sure to stop (Disable) peripherals.

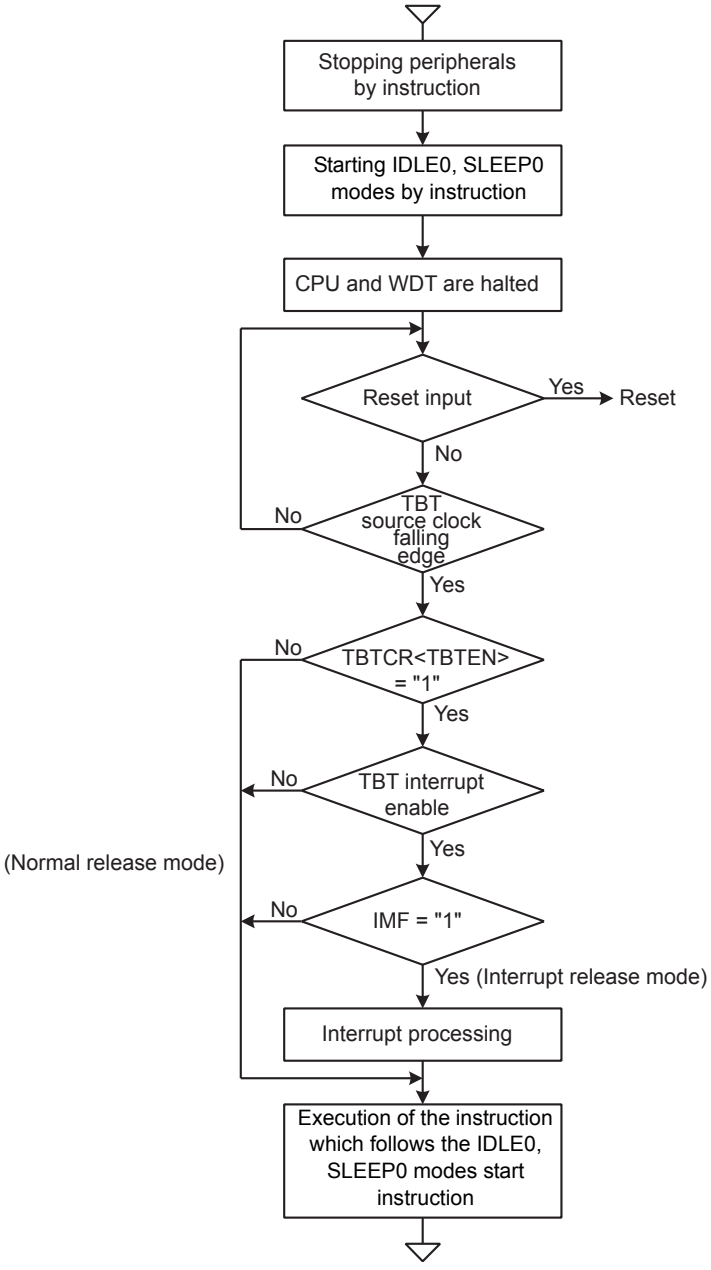


Figure 2-12 IDLE0 and SLEEP0 Modes

- Start the IDLE0 and SLEEP0 modes

  Stop (Disable) peripherals such as a timer counter.

  To start IDLE0 and SLEEP0 modes, set SYSCR2<TGHALT> to “1”.

- Release the IDLE0 and SLEEP0 modes

  IDLE0 and SLEEP0 modes include a normal release mode and an interrupt release mode.

  These modes are selected by interrupt master flag (IMF), the individual interrupt enable flag of TBT and TBTCR<TBTEN>.

  After releasing IDLE0 and SLEEP0 modes, the SYSCR2<TGHALT> is automatically cleared to “0” and the operation mode is returned to the mode preceding IDLE0 and SLEEP0 modes. Before starting the IDLE0 or SLEEP0 mode, when the TBTCR<TBTEN> is set to “1”, INTTBT interrupt latch is set to “1”.

  IDLE0 and SLEEP0 modes can also be released by inputting low level on the $\overline{\text{RESET}}$ pin. After releasing reset, the operation mode is started from NORMAL1 mode.

Note: IDLE0 and SLEEP0 modes start/release without reference to TBTCR<TBTEN> setting.

(1) Normal release mode (IMF•EF7•TBTCR<TBTEN> = “0”)

IDLE0 and SLEEP0 modes are released by the source clock falling edge, which is setting by the TBTCR<TBTCK>. After the falling edge is detected, the program operation is resumed from the instruction following the IDLE0 and SLEEP0 modes start instruction. Before starting the IDLE0 or SLEEP0 mode, when the TBTCR<TBTEN> is set to “1”, INTTBT interrupt latch is set to “1”.

(2) Interrupt release mode (IMF•EF7•TBTCR<TBTEN> = “1”)

IDLE0 and SLEEP0 modes are released by the source clock falling edge, which is setting by the TBTCR<TBTCK> and INTTBT interrupt processing is started.

Note 1: Because returning from IDLE0, SLEEP0 to NORMAL1, SLOW1 is executed by the asynchronous internal clock, the period of IDLE0, SLEEP0 mode might be the shorter than the period setting by TBTCR<TBTCK>.

Note 2: When a watchdog timer interrupt is generated immediately before IDLE0/SLEEP0 mode is started, the watchdog timer interrupt will be processed but IDLE0/SLEEP0 mode will not be started.

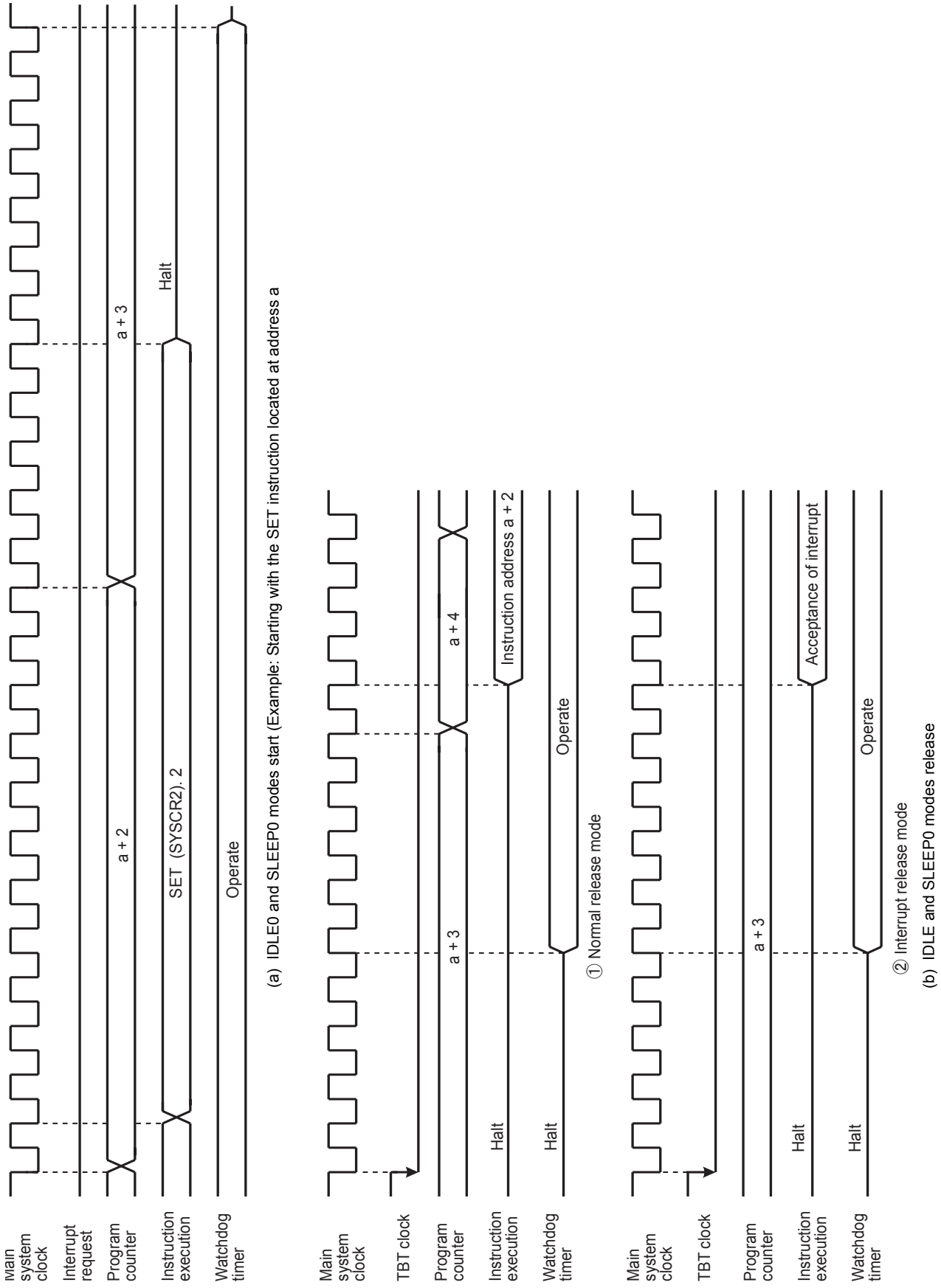


Figure 2-13 IDLE0 and SLEEP0 Modes Start/Release

2.2.4.4 SLOW mode

SLOW mode is controlled by the system control register 2 (SYSCR2).

The following is the methods to switch the mode with the warm-up counter.

(1) Switching from NORMAL2 mode to SLOW1 mode

First, set SYSCR2<SYSCK> to switch the main system clock to the low-frequency clock for SLOW2 mode. Next, clear SYSCR2<XEN> to turn off high-frequency oscillation.

Note: The high-frequency clock can be continued oscillation in order to return to NORMAL2 mode from SLOW mode quickly. Always turn off oscillation of high-frequency clock when switching from SLOW mode to stop mode.

Example 1 :Switching from NORMAL2 mode to SLOW1 mode.

```
        SET     (SYSCR2). 5     ; SYSCR2<SYSCK> ← 1
                                  (Switches the main system clock to the low-frequency
                                  clock for SLOW2)
        CLR     (SYSCR2). 7     ; SYSCR2<XEN> ← 0
                                  (Turns off high-frequency oscillation)
```

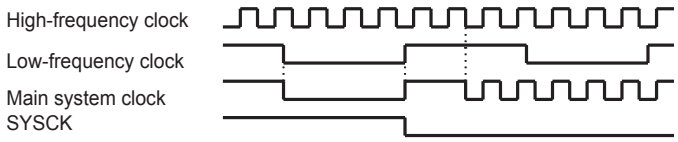
Example 2 :Switching to the SLOW1 mode after low-frequency clock has stabilized.

```
        SET     (SYSCR2). 6     ; SYSCR2<XTEN> ← 1
        LD      (TC5CR), 43H    ; Sets mode for TC6, 5 (16-bit mode, fs for source)
        LD      (TC6CR), 05H    ; Sets warming-up counter mode
        LDW     (TTREG5), 8000H ; Sets warm-up time (Depend on oscillator accompanied)
        DI                      ; IMF ← 0
        SET     (EIRE). 2       ; Enables INTTC6
        EI                      ; IMF ← 1
        SET     (TC6CR). 3      ; Starts TC6, 5
         :
PINTTC6: CLR    (TC6CR). 3      ; Stops TC6, 5
        SET     (SYSCR2). 5     ; SYSCR2<SYSCK> ← 1
                                  (Switches the main system clock to the low-frequency clock)
        CLR     (SYSCR2). 7     ; SYSCR2<XEN> ← 0
                                  (Turns off high-frequency oscillation)
        RETI
         :
VINTTC6: DW     PINTTC6         ; INTTC6 vector table
```

(2) Switching from SLOW1 mode to NORMAL2 mode

First, set SYSCR2<XEN> to turn on the high-frequency oscillation. When time for stabilization (Warm up) has been taken by the timer/counter (TC6,TC5), clear SYSCR2<SYSCK> to switch the main system clock to the high-frequency clock.
SLOW mode can also be released by inputting low level on the $\overline{\text{RESET}}$ pin. After releasing reset, the operation mode is started from NORMAL1 mode.

Note: After SYSCK is cleared to "0", executing the instructions is continiued by the low-frequency clock for the period synchronized with low-frequency and high-frequency clocks.



Example :Switching from the SLOW1 mode to the NORMAL2 mode (fc = 16 MHz, warm-up time is 4.0 ms).

```
                SET     (SYSCR2). 7         ; SYSCR2<XEN> ← 1 (Starts high-frequency oscillation)
                LD      (TC5CR), 63H        ; Sets mode for TC6, 5 (16-bit mode, fc for source)
                LD      (TC6CR), 05H        ; Sets warming-up counter mode
                LD      (TTREG6), 0F8H      ; Sets warm-up time
                DI                          ; IMF ← 0
                SET     (EIRE). 2           ; Enables INTTC6
                EI                          ; IMF ← 1
                SET     (TC6CR). 3          ; Starts TC6, 5
                 :
PINTTC6:        CLR     (TC6CR). 3          ; Stops TC6, 5
                CLR     (SYSCR2). 5         ; SYSCR2<SYSCK> ← 0
                                              (Switches the main system clock to the high-frequency clock)
                RETI
                 :
VINTTC6:        DW      PINTTC6             ; INTTC6 vector table
```

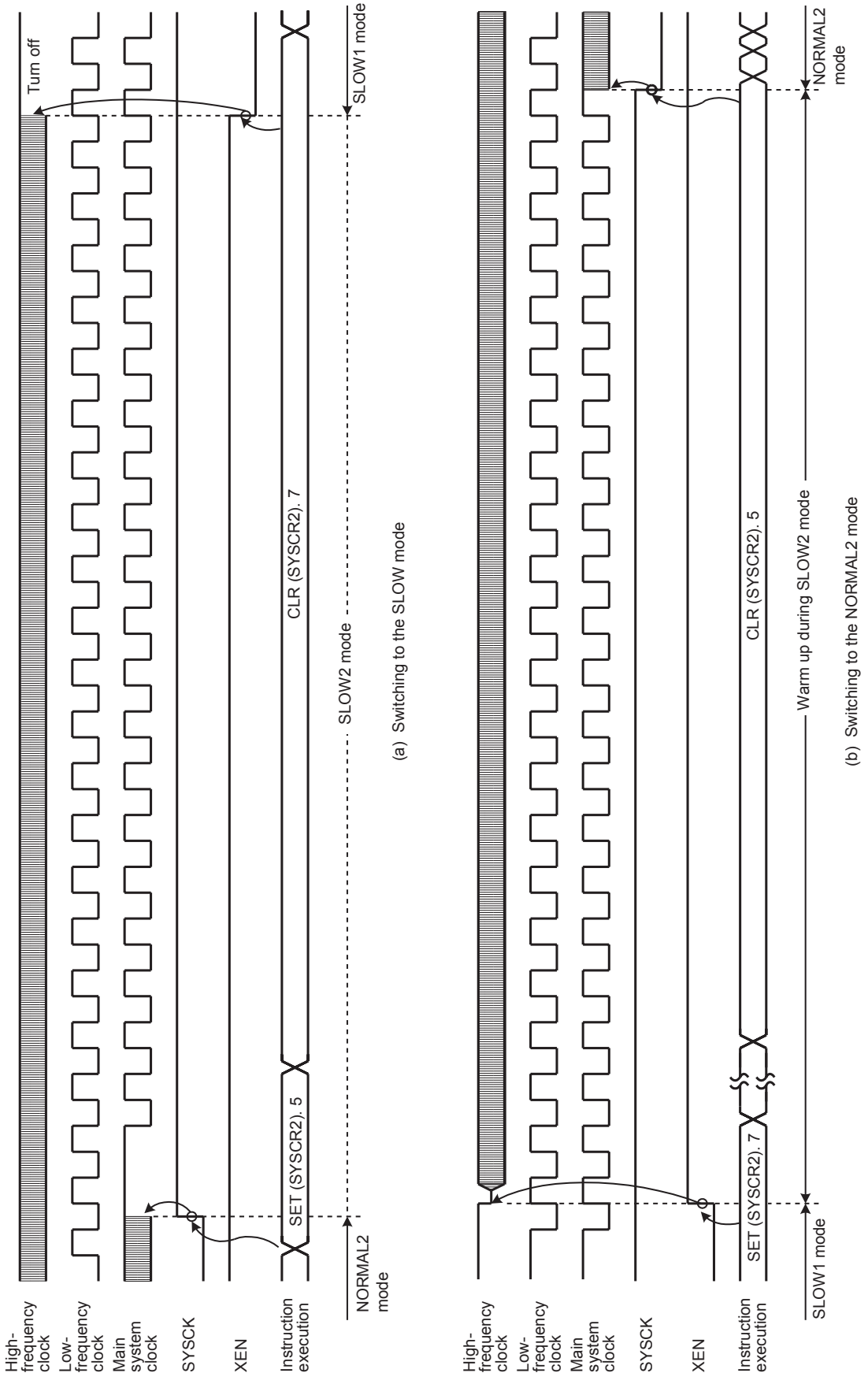


Figure 2-14 Switching between the NORMAL2 and SLOW Modes

2.3 Reset Circuit

The T5CL8 has four types of reset generation procedures: An external reset input, an address trap reset, a watchdog timer reset and a system clock reset. Of these reset, the address trap reset, the watchdog timer and the system clock reset are a malfunction reset. When the malfunction reset request is detected, reset occurs during the maximum 24/fc[s].

The malfunction reset circuit such as watchdog timer reset, address trap reset and system clock reset is not initialized when power is turned on. Therefore, reset may occur during maximum 24/fc[s] (1.5μs at 16.0 MHz) when power is turned on.

Table 2-3 shows on-chip hardware initialization by reset action.

Table 2-3 Initializing Internal Status by Reset Action

On-chip Hardware		Initial Value	On-chip Hardware	Initial Value
Program counter	(PC)	(FFFEH)	Prescaler and divider of timing generator	0
Stack pointer	(SP)	Not initialized		
General-purpose registers (W, A, B, C, D, E, H, L, IX, IY)		Not initialized		
Jump status flag	(JF)	Not initialized	Watchdog timer	Enable
Zero flag	(ZF)	Not initialized	Output latches of I/O ports	Refer to I/O port circuitry
Carry flag	(CF)	Not initialized		
Half carry flag	(HF)	Not initialized		
Sign flag	(SF)	Not initialized		
Overflow flag	(VF)	Not initialized		
Interrupt master enable flag	(IMF)	0		
Interrupt individual enable flags	(EF)	0	Control registers	Refer to each of control register
Interrupt latches	(IL)	0		
			RAM	Not initialized

2.3.1 External Reset Input

The $\overline{\text{RESET}}$ pin contains a Schmitt trigger (Hysteresis) with an internal pull-up resistor.

When the $\overline{\text{RESET}}$ pin is held at "L" level for at least 3 machine cycles (12/fc [s]) with the power supply voltage within the operating voltage range and oscillation stable, a reset is applied and the internal state is initialized.

When the $\overline{\text{RESET}}$ pin input goes high, the reset operation is released and the program execution starts at the vector address stored at addresses FFFEH to FFFFH.

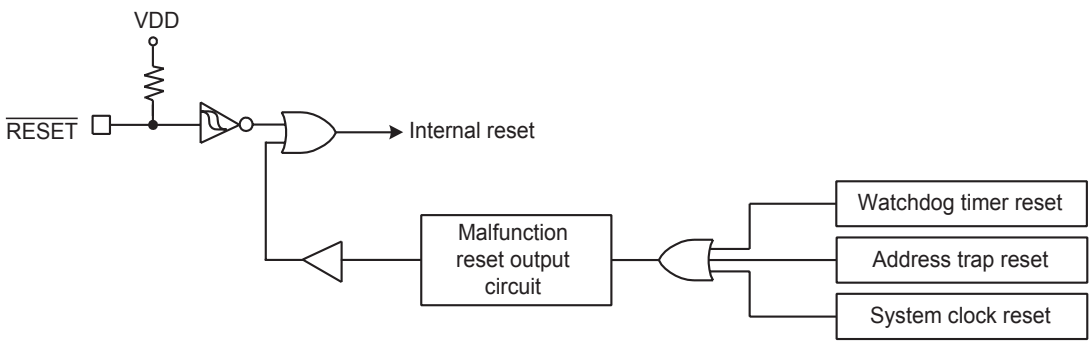
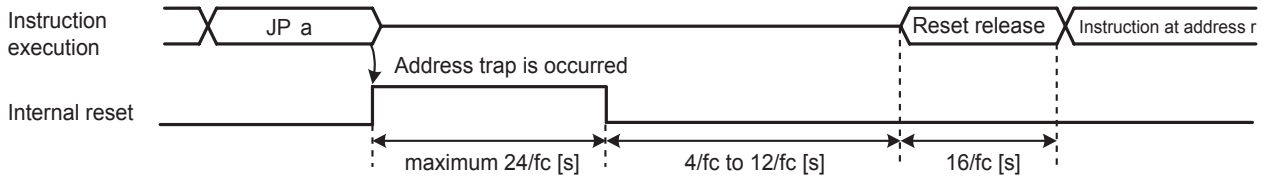


Figure 2-15 Reset Circuit

2.3.2 Address trap reset

If the CPU should start looping for some cause such as noise and an attempt be made to fetch an instruction from the on-chip RAM (when WDTCR1<ATAS> is set to “1”), DBR or the SFR area, address trap reset will be generated. The reset time is maximum 24/fc[s] (1.5μs at 16.0 MHz).

Note: The operating mode under address trapped is alternative of reset or interrupt. The address trap area is alternative.



Note 1: Address “a” is in the SFR, DBR or on-chip RAM (WDTCR1<ATAS> = “1”) space.
Note 2: During reset release, reset vector “r” is read out, and an instruction at address “r” is fetched and decoded.

Figure 2-16 Address Trap Reset

2.3.3 Watchdog timer reset

Refer to Section “Watchdog Timer”.

2.3.4 System clock reset

If the condition as follows is detected, the system clock reset occurs automatically to prevent dead lock of the CPU. (The oscillation is continued without stopping.)

- In case of clearing SYSCR2<XEN> and SYSCR2<XTEN> simultaneously to “0”.
- In case of clearing SYSCR2<XEN> to “0”, when the SYSCR2<SYSCK> is “0”.
- In case of clearing SYSCR2<XTEN> to “0”, when the SYSCR2<SYSCK> is “1”.

The reset time is maximum 24/fc (1.5 μs at 16.0 MHz).

3. Interrupt Control Circuit

The T5CL8 has a total of 24 interrupt sources excluding reset. Interrupts can be nested with priorities. Four of the internal interrupt sources are non-maskable while the rest are maskable.

Interrupt sources are provided with interrupt latches (IL), which hold interrupt requests, and independent vectors. The interrupt latch is set to “1” by the generation of its interrupt request which requests the CPU to accept its interrupts. Interrupts are enabled or disabled by software using the interrupt master enable flag (IMF) and interrupt enable flag (EF). If more than one interrupts are generated simultaneously, interrupts are accepted in order which is dominated by hardware. However, there are no prioritized interrupt factors among non-maskable interrupts.

Interrupt Factors		Enable Condition	Interrupt Latch	Vector Address	Priority
Internal/External	(Reset)	Non-maskable	–	FFFE	1
Internal	INTSWI (Software interrupt)	Non-maskable	–	FFFC	2
Internal	INTUNDEF (Executed the undefined instruction interrupt)	Non-maskable	–	FFFC	2
Internal	INTATRAP (Address trap interrupt)	Non-maskable	IL2	FFFA	2
Internal	INTWDT (Watchdog timer interrupt)	Non-maskable	IL3	FFF8	2
External	$\overline{\text{INT0}}$	IMF• EF4 = 1, INT0EN = 1	IL4	FFF6	5
Internal	INTTC1	IMF• EF5 = 1	IL5	FFF4	6
External	INT1	IMF• EF6 = 1	IL6	FFF2	7
Internal	INTTBT	IMF• EF7 = 1	IL7	FFF0	8
External	INT2	IMF• EF8 = 1	IL8	FFEE	9
Internal	INTTC4	IMF• EF9 = 1	IL9	FFEC	10
Internal	INTTC3	IMF• EF10 = 1	IL10	FFEA	11
Internal	INTSBI	IMF• EF11 = 1	IL11	FFE8	12
External	INT3	IMF• EF12 = 1	IL12	FFE6	13
Internal	INTSIO1	IMF• EF13 = 1	IL13	FFE4	14
Internal	INTSIO2	IMF• EF14 = 1	IL14	FFE2	15
Internal	INTADC	IMF• EF15 = 1	IL15	FFE0	16
Internal	INTRXD1	IMF• EF16 = 1	IL16	FFBE	17
Internal	INTTXD1	IMF• EF17 = 1	IL17	FFBC	18
Internal	INTTC6	IMF• EF18 = 1	IL18	FFBA	19
Internal	INTTC5	IMF• EF19 = 1	IL19	FFB8	20
Internal	INTRXD2	IMF• EF20 = 1	IL20	FFB6	21
Internal	INTTXD2	IMF• EF21 = 1	IL21	FFB4	22
Internal	INTTC2	IMF• EF22 = 1	IL22	FFB2	23
External	$\overline{\text{INT5}}$	IMF• EF23 = 1	IL23	FFB0	24

Note 1: To use the address trap interrupt (INTATRAP), clear WDTCR1<ATOUT> to “0” (It is set for the “reset request” after reset is cancelled). For details, see “Address Trap”.

Note 2: To use the watchdog timer interrupt (INTWDT), clear WDTCR1<WDTOUT> to "0" (It is set for the "Reset request" after reset is released). For details, see "Watchdog Timer".

Note 3: If an INTADC interrupt request is generated while an interrupt with priority lower than the interrupt latch IL15 (INTADC) is being accepted, the INTADC interrupt latch may be cleared without the INTADC interrupt being processed. For details, refer to the corresponding notes in the chapter on the AD converter.

3.1 Interrupt latches (IL23 to IL2)

An interrupt latch is provided for each interrupt source, except for a software interrupt and an executed the undefined instruction interrupt. When interrupt request is generated, the latch is set to “1”, and the CPU is requested to accept the interrupt if its interrupt is enabled. The interrupt latch is cleared to "0" immediately after accepting interrupt. All interrupt latches are initialized to “0” during reset.

The interrupt latches are located on address 002EH, 003CH and 003DH in SFR area. Each latch can be cleared to "0" individually by instruction. However, IL2 and IL3 should not be cleared to "0" by software. For clearing the interrupt latch, load instruction should be used and then IL2 and IL3 should be set to "1". If the read-modify-write instructions such as bit manipulation or operation instructions are used, interrupt request would be cleared inadequately if interrupt is requested while such instructions are executed.

Interrupt latches are not set to “1” by an instruction.

Since interrupt latches can be read, the status for interrupt requests can be monitored by software.

Note: In main program, before manipulating the interrupt enable flag (EF) or the interrupt latch (IL), be sure to clear IMF to "0" (Disable interrupt by DI instruction). Then set IMF newly again as required after operating on the EF or IL (Enable interrupt by EI instruction)
In interrupt service routine, because the IMF becomes "0" automatically, clearing IMF need not execute normally on interrupt service routine. However, if using multiple interrupt on interrupt service routine, manipulating EF or IL should be executed before setting IMF="1".

Example 1 :Clears interrupt latches

```
DI                          ; IMF ← 0
LDW     (ILL), 1110100000111111B    ; IL12, IL10 to IL6 ← 0
EI                          ; IMF ← 1
```

Example 2 :Reads interrupt latchess

```
LD      WA, (ILL)           ; W ← ILH, A ← ILL
```

Example 3 :Tests interrupt latches

```
TEST    (ILL). 7            ; if IL7 = 1 then jump
JR      F, SSET
```

3.2 Interrupt enable register (EIR)

The interrupt enable register (EIR) enables and disables the acceptance of interrupts, except for the non-maskable interrupts (Software interrupt, undefined instruction interrupt, address trap interrupt and watchdog interrupt). Non-maskable interrupt is accepted regardless of the contents of the EIR.

The EIR consists of an interrupt master enable flag (IMF) and the individual interrupt enable flags (EF). These registers are located on address 002CH, 003AH and 003BH in SFR area, and they can be read and written by an instructions (Including read-modify-write instructions such as bit manipulation or operation instructions).

3.2.1 Interrupt master enable flag (IMF)

The interrupt enable register (IMF) enables and disables the acceptance of the whole maskable interrupt. While IMF = “0”, all maskable interrupts are not accepted regardless of the status on each individual interrupt enable flag (EF). By setting IMF to “1”, the interrupt becomes acceptable if the individuals are enabled. When an interrupt is accepted, IMF is cleared to “0” after the latest status on IMF is stacked. Thus the maskable interrupts which follow are disabled. By executing return interrupt instruction [RETI/RETN], the stacked data, which was the status before interrupt acceptance, is loaded on IMF again.

The IMF is located on bit0 in EIRL (Address: 003AH in SFR), and can be read and written by an instruction. The IMF is normally set and cleared by [EI] and [DI] instruction respectively. During reset, the IMF is initialized to “0”.

3.2.2 Individual interrupt enable flags (EF23 to EF4)

Each of these flags enables and disables the acceptance of its maskable interrupt. Setting the corresponding bit of an individual interrupt enable flag to “1” enables acceptance of its interrupt, and setting the bit to “0” disables acceptance. During reset, all the individual interrupt enable flags (EF23 to EF4) are initialized to “0” and all maskable interrupts are not accepted until they are set to “1”.

Note: In main program, before manipulating the interrupt enable flag (EF) or the interrupt latch (IL), be sure to clear IMF to "0" (Disable interrupt by DI instruction). Then set IMF newly again as required after operating on the EF or IL (Enable interrupt by EI instruction)
In interrupt service routine, because the IMF becomes "0" automatically, clearing IMF need not execute normally on interrupt service routine. However, if using multiple interrupt on interrupt service routine, manipulating EF or IL should be executed before setting IMF="1".

Example 1 :Enables interrupts individually and sets IMF

```
DI                                      ; IMF ← 0
LDW         (EIRL), 1110100010100000B   ; EF15 to EF13, EF11, EF7, EF5 ← 1
  :                                       Note: IMF should not be set.
  :
EI                                      ; IMF ← 1
```

Example 2 :C compiler description example

```
unsigned  int  _io (3AH)  EIRL;         /* 3AH shows EIRL address */
_DI();
EIRL = 10100000B;
  :
_EI();
```

Interrupt Latches

(Initial value: 00000000 000000**)

ILH,ILL (003DH, 003CH)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IL15	IL14	IL13	IL12	IL11	IL10	IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2		
ILH (003DH)								ILL (003CH)							

(Initial value: 00000000)

ILE (002EH)

7	6	5	4	3	2	1	0
IL23	IL22	IL21	IL20	IL19	IL18	IL17	IL16
ILE (002EH)							

		at RD	at WR	
IL23 to IL2	Interrupt latches	0: No interrupt request 1: Interrupt request	0: Clears the interrupt request 1: (Interrupt latch is not set.)	R/W

Note 1: To clear any one of bits IL7 to IL4, be sure to write "1" into IL2 and IL3.

Note 2: In main program, before manipulating the interrupt enable flag (EF) or the interrupt latch (IL), be sure to clear IMF to "0" (Disable interrupt by DI instruction). Then set IMF newly again as required after operating on the EF or IL (Enable interrupt by EI instruction)
In interrupt service routine, because the IMF becomes "0" automatically, clearing IMF need not execute normally on interrupt service routine. However, if using multiple interrupt on interrupt service routine, manipulating EF or IL should be executed before setting IMF="1".

Note 3: Do not clear IL with read-modify-write instructions such as bit operations.

Interrupt Enable Registers

(Initial value: 00000000 0000***0)

EIRH,EIRL (003BH, 003AH)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EF15	EF14	EF13	EF12	EF11	EF10	EF9	EF8	EF7	EF6	EF5	EF4				IMF
EIRH (003BH)								EIRL (003AH)							

(Initial value: 00000000)

EIRE (002CH)

7	6	5	4	3	2	1	0
EF23	EF22	EF21	EF20	EF19	EF18	EF17	EF16
EIRE (002CH)							

EF23 to EF4	Individual-interrupt enable flag (Specified for each bit)	0: Disables the acceptance of each maskable interrupt. 1: Enables the acceptance of each maskable interrupt.	R/W
IMF	Interrupt master enable flag	0: Disables the acceptance of all maskable interrupts 1: Enables the acceptance of all maskable interrupts	

Note 1: *: Don’t care

Note 2: Do not set IMF and the interrupt enable flag (EF15 to EF4) to “1” at the same time.

Note 3: In main program, before manipulating the interrupt enable flag (EF) or the interrupt latch (IL), be sure to clear IMF to "0" (Disable interrupt by DI instruction). Then set IMF newly again as required after operating on the EF or IL (Enable interrupt by EI instruction)
In interrupt service routine, because the IMF becomes "0" automatically, clearing IMF need not execute normally on interrupt service routine. However, if using multiple interrupt on interrupt service routine, manipulating EF or IL should be executed before setting IMF="1".

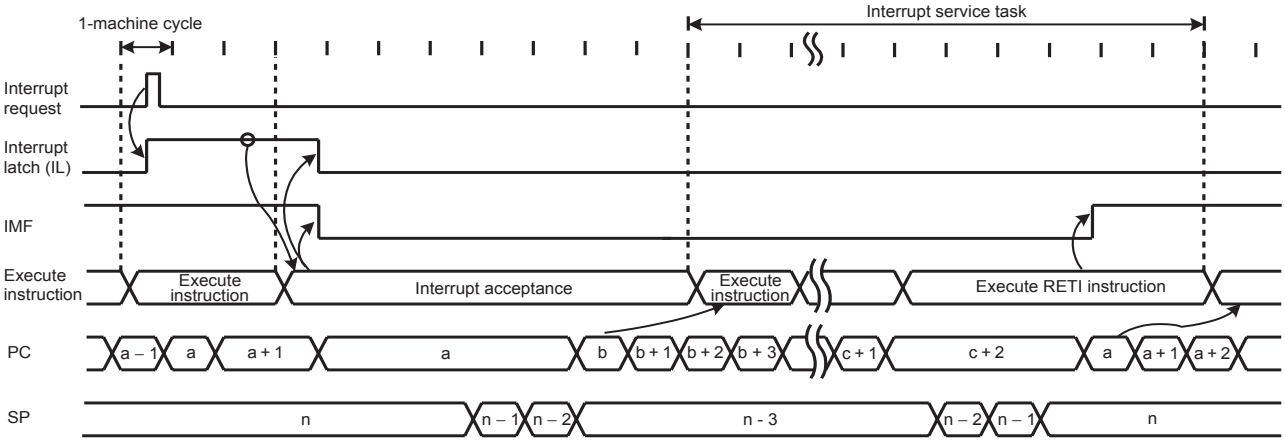
3.3 Interrupt Sequence

An interrupt request, which raised interrupt latch, is held, until interrupt is accepted or interrupt latch is cleared to "0" by resetting or an instruction. Interrupt acceptance sequence requires 8 machine cycles (2 μs @16 MHz) after the completion of the current instruction. The interrupt service task terminates upon execution of an interrupt return instruction [RETI] (for maskable interrupts) or [RETN] (for non-maskable interrupts). Figure 3-1 shows the timing chart of interrupt acceptance processing.

3.3.1 Interrupt acceptance processing is packaged as follows.

a. The interrupt master enable flag (IMF) is cleared to "0" in order to disable the acceptance of any following interrupt.
b. The interrupt latch (IL) for the interrupt source accepted is cleared to "0".
c. The contents of the program counter (PC) and the program status word, including the interrupt master enable flag (IMF), are saved (Pushed) on the stack in sequence of PSW + IMF, PCH, PCL. Meanwhile, the stack pointer (SP) is decremented by 3.
d. The entry address (Interrupt vector) of the corresponding interrupt service program, loaded on the vector table, is transferred to the program counter.
e. The instruction stored at the entry address of the interrupt service program is executed.

Note: When the contents of PSW are saved on the stack, the contents of IMF are also saved.



Note 1: a: Return address entry address, b: Entry address, c: Address which RETI instruction is stored
Note 2: On condition that interrupt is enabled, it takes 38/fc [s] or 38/fs [s] at maximum (If the interrupt latch is set at the first machine cycle on 10 cycle instruction) to start interrupt acceptance processing since its interrupt latch is set.

Figure 3-1 Timing Chart of Interrupt Acceptance/Return Interrupt Instruction

Example: Correspondence between vector table address for INTTBT and the entry address of the interrupt service program

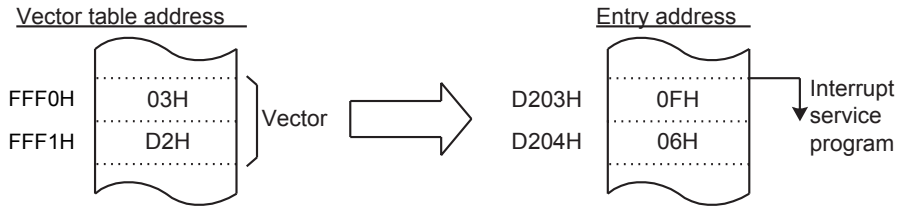


Figure 3-2 Vector table address,Entry address

A maskable interrupt is not accepted until the IMF is set to “1” even if the maskable interrupt higher than the level of current servicing interrupt is requested.

In order to utilize nested interrupt service, the IMF is set to “1” in the interrupt service program. In this case, acceptable interrupt sources are selectively enabled by the individual interrupt enable flags.

To avoid overloaded nesting, clear the individual interrupt enable flag whose interrupt is currently serviced, before setting IMF to “1”. As for non-maskable interrupt, keep interrupt service shorten compared with length between interrupt requests; otherwise the status cannot be recovered as non-maskable interrupt would simply nested.

3.3.2 Saving/restoring general-purpose registers

During interrupt acceptance processing, the program counter (PC) and the program status word (PSW, includes IMF) are automatically saved on the stack, but the accumulator and others are not. These registers are saved by software if necessary. When multiple interrupt services are nested, it is also necessary to avoid using the same data memory area for saving registers. The following methods are used to save/restore the general-purpose registers.

3.3.2.1 Using PUSH and POP instructions

If only a specific register is saved or interrupts of the same source are nested, general-purpose registers can be saved/restored using the PUSH/POP instructions.

Example :Save/store register using PUSH and POP instructions

```
PINTxx:   PUSH   WA          ; Save WA register
          (interrupt processing)
          POP    WA          ; Restore WA register
          RETI               ; RETURN
```

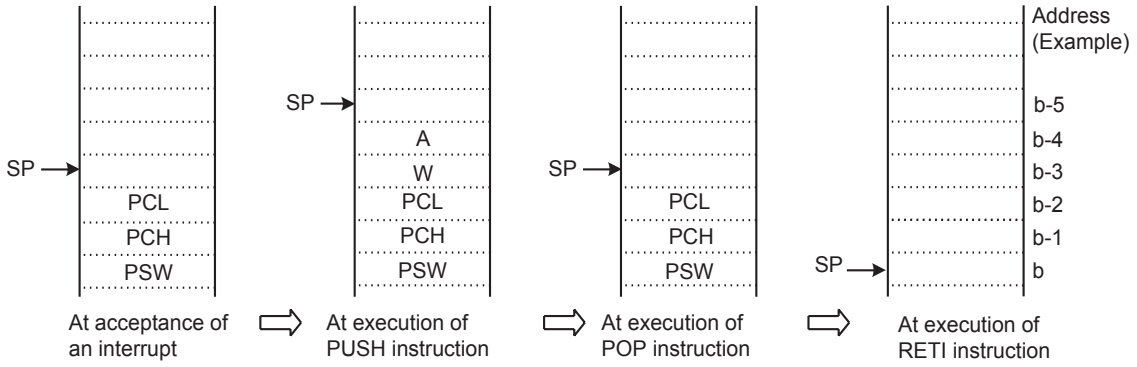


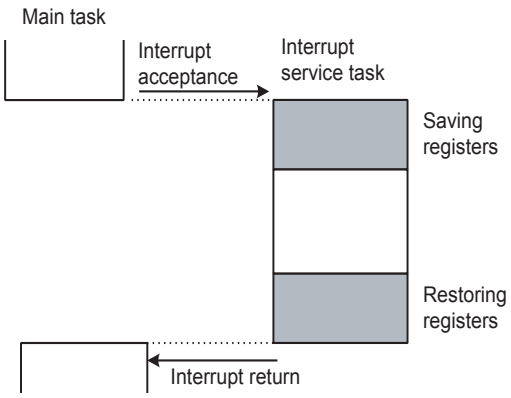
Figure 3-3 Save/store register using PUSH and POP instructions

3.3.2.2 Using data transfer instructions

To save only a specific register without nested interrupts, data transfer instructions are available.

Example :Save/store register using data transfer instructions

```
PINTxx:   LD      (GSAVA), A      ; Save A register
          (interrupt processing)
          LD      A, (GSAVA)      ; Restore A register
          RETI                    ; RETURN
```



Saving/Restoring general-purpose registers using PUSH/POP data transfer instruction

Figure 3-4 Saving/Restoring General-purpose Registers under Interrupt Processing

3.3.3 Interrupt return

Interrupt return instructions [RETI]/[RETN] perform as follows.

[RETI]/[RETN] Interrupt Return
1. Program counter (PC) and program status word (PSW, includes IMF) are restored from the stack. 2. Stack pointer (SP) is incremented by 3.

As for address trap interrupt (INTATRAP), it is required to alter stacked data for program counter (PC) to restarting address, during interrupt service program.

Note: If [RETN] is executed with the above data unaltered, the program returns to the address trap area and INTATRAP occurs again.When interrupt acceptance processing has completed, stacked data for PCL and PCH are located on address (SP + 1) and (SP + 2) respectively.

Example 1 :Returning from address trap interrupt (INTATRAP) service program

```
PINTxx:   POP     WA              ; Recover SP by 2
          LD      WA, Return Address ;
          PUSH    WA              ; Alter stacked data
          (interrupt processing)
          RETN                    ; RETURN
```

Example 2 :Restarting without returning interrupt
(In this case, PSW (Includes IMF) before interrupt acceptance is discarded.)

```
PINTxx:   INC     SP              ; Recover SP by 3
          INC     SP              ;
          INC     SP              ;
          (interrupt processing)
          LD      EIRL, data      ; Set IMF to "1" or clear it to "0"
          JP      Restart Address ; Jump into restarting address
```

Interrupt requests are sampled during the final cycle of the instruction being executed. Thus, the next interrupt can be accepted immediately after the interrupt return instruction is executed.

Note 1: It is recommended that stack pointer be return to rate before INTATRAP (Increment 3 times), if return interrupt instruction [RETN] is not utilized during interrupt service program under INTATRAP (such as Example 2).

Note 2: When the interrupt processing time is longer than the interrupt request generation time, the interrupt service task is performed but not the main task.

3.4 Software Interrupt (INTSW)

Executing the SWI instruction generates a software interrupt and immediately starts interrupt processing (INTSW is highest prioritized interrupt).

Use the SWI instruction only for detection of the address error or for debugging.

3.4.1 Address error detection

FFH is read if for some cause such as noise the CPU attempts to fetch an instruction from a non-existent memory address during single chip mode. Code FFH is the SWI instruction, so a software interrupt is generated and an address error is detected. The address error detection range can be further expanded by writing FFH to unused areas of the program memory. Address trap reset is generated in case that an instruction is fetched from RAM, DBR or SFR areas.

3.4.2 Debugging

Debugging efficiency can be increased by placing the SWI instruction at the software break point setting address.

3.5 Undefined Instruction Interrupt (INTUNDEF)

Taking code which is not defined as authorized instruction for instruction causes INTUNDEF. INTUNDEF is generated when the CPU fetches such a code and tries to execute it. INTUNDEF is accepted even if non-maskable interrupt is in process. Contemporary process is broken and INTUNDEF interrupt process starts, soon after it is requested.

Note: The undefined instruction interrupt (INTUNDEF) forces CPU to jump into vector address, as software interrupt (SWI) does.

3.6 Address Trap Interrupt (INTATRAP)

Fetching instruction from unauthorized area for instructions (Address trapped area) causes reset output or address trap interrupt (INTATRAP). INTATRAP is accepted even if non-maskable interrupt is in process. Contemporary process is broken and INTATRAP interrupt process starts, soon after it is requested.

Note: The operating mode under address trapped, whether to be reset output or interrupt processing, is selected on watchdog timer control register (WDTCR).

3.7 External Interrupts

The T5CL8 has 5 external interrupt inputs. These inputs are equipped with digital noise reject circuits (Pulse inputs of less than a certain time are eliminated as noise).

Edge selection is also possible with INT1 to INT3. The $\overline{\text{INT0}}$/P00 pin can be configured as either an external interrupt input pin or an input/output port, and is configured as an input port during reset.

Edge selection, noise reject control and $\overline{\text{INT0}}$/P00 pin function selection are performed by the external interrupt control register (EINTCR).

Source	Pin	Enable Conditions	Release Edge	Digital Noise Reject
INT0	$\overline{\text{INT0}}$	IMF • EF4 • INT0EN=1	Falling edge	Pulses of less than 2/fc [s] are eliminated as noise. Pulses of 7/fc [s] or more are considered to be signals. In the SLOW or the SLEEP mode, pulses of less than 1/fs [s] are eliminated as noise. Pulses of 3.5/fs [s] or more are considered to be signals.
INT1	INT1	IMF • EF6 = 1	Falling edge or Rising edge	Pulses of less than 15/fc or 63/fc [s] are eliminated as noise. Pulses of 49/fc or 193/fc [s] or more are considered to be signals. In the SLOW or the SLEEP mode, pulses of less than 1/fs [s] are eliminated as noise. Pulses of 3.5/fs [s] or more are considered to be signals.
INT2	INT2	IMF • EF8 = 1	Falling edge or Rising edge	Pulses of less than 7/fc [s] are eliminated as noise. Pulses of 25/fc [s] or more are considered to be signals. In the SLOW or the SLEEP mode, pulses of less than 1/fs [s] are eliminated as noise. Pulses of 3.5/fs [s] or more are considered to be signals.
INT3	INT3	IMF • EF12 = 1	Falling edge or Rising edge	Pulses of less than 7/fc [s] are eliminated as noise. Pulses of 25/fc [s] or more are considered to be signals. In the SLOW or the SLEEP mode, pulses of less than 1/fs [s] are eliminated as noise. Pulses of 3.5/fs [s] or more are considered to be signals.
INT5	$\overline{\text{INT5}}$	IMF • EF23 = 1	Falling edge	Pulses of less than 2/fc [s] are eliminated as noise. Pulses of 7/fc [s] or more are considered to be signals. In the SLOW or the SLEEP mode, pulses of less than 1/fs [s] are eliminated as noise. Pulses of 3.5/fs [s] or more are considered to be signals.

Note 1: In NORMAL1/2 or IDLE1/2 mode, if a signal with no noise is input on an external interrupt pin, it takes a maximum of "signal establishment time + 6/fs[s]" from the input signal's edge to set the interrupt latch.

Note 2: When INT0EN = "0", IL4 is not set even if a falling edge is detected on the $\overline{\text{INT0}}$ pin input.

Note 3: When a pin with more than one function is used as an output and a change occurs in data or input/output status, an interrupt request signal is generated in a pseudo manner. In this case, it is necessary to perform appropriate processing such as disabling the interrupt enable flag.

External Interrupt Control Register

EINTCR	7	6	5	4	3	2	1	0	
(0037H)	INT1NC	INT0EN	-	-	INT3ES	INT2ES	INT1ES		(Initial value: 00** 000*)

INT1NC	Noise reject time select	0: Pulses of less than 63/fc [s] are eliminated as noise 1: Pulses of less than 15/fc [s] are eliminated as noise	R/W
INT0EN	P00/$\overline{\text{INT0}}$ pin configuration	0: P00 input/output port 1: $\overline{\text{INT0}}$ pin (Port P00 should be set to an input mode)	R/W
INT3 ES	INT3 edge select	0: Rising edge 1: Falling edge	R/W
INT2 ES	INT2 edge select	0: Rising edge 1: Falling edge	R/W
INT1 ES	INT1 edge select	0: Rising edge 1: Falling edge	R/W

Note 1: fc: High-frequency clock [Hz], *: Don't care

Note 2: When the system clock frequency is switched between high and low or when the external interrupt control register (EINTCR) is overwritten, the noise canceller may not operate normally. It is recommended that external interrupts are disabled using the interrupt enable register (EIR).

Note 3: The maximum time from modifying INT1NC until a noise reject time is changed is 2^6/fc.

4. Special Function Register (SFR)

The T5CL8 adopts the memory mapped I/O system, and all peripheral control and data transfers are performed through the special function register (SFR) or the data buffer register (DBR). The SFR is mapped on address 0000H to 003FH, DBR is mapped on address 0F80H to 0FFFH.

This chapter shows the arrangement of the special function register (SFR) and data buffer register (DBR) for T5CL8.

4.1 SFR

Address	Read	Write
0000H	P0DR	
0001H	P1DR	
0002H	P2DR	
0003H	P3DR	
0004H	P4DR	
0005H	P5DR	
0006H	P6DR	
0007H	P7DR	
0008H	P0OUTCR	
0009H	P1CR	
000AH	P4OUTCR	
000BH	P0PRD	-
000CH	P2PRD	-
000DH	P3PRD	-
000EH	P4PRD	-
000FH	P5PRD	-
0010H	TC1DRAL	
0011H	TC1DRAH	
0012H	TC1DRBL	
0013H	TC1DRBH	
0014H	TTREG3	
0015H	TTREG4	
0016H	TTREG5	
0017H	TTREG6	
0018H	PWREG3	
0019H	PWREG4	
001AH	PWREG5	
001BH	PWREG6	
001CH	ADCCR1	
001DH	ADCCR2	
001EH	ADCDR2	-
001FH	ADCDR1	-
0020H	SIO1CR	
0021H	SIO1SR	-
0022H	SIO1RDB	SIO1TDB
0023H	TC2CR	
0024H	TC2DRL	
0025H	TC2DRH	

Address	Read	Write
0026H	TC1CR	
0027H	TC3CR	
0028H	TC4CR	
0029H	TC5CR	
002AH	TC6CR	
002BH	SIO2RDB	SIO2TDB
002CH	EIRE	
002DH	Reserved	
002EH	ILE	
002FH	Reserved	
0030H	Reserved	
0031H	SIO2CR	
0032H	SIO2SR	-
0033H	Reserved	
0034H	-	WDTCR1
0035H	-	WDTCR2
0036H	TBTCR	
0037H	EINTCR	
0038H	SYSCR1	
0039H	SYSCR2	
003AH	EIRL	
003BH	EIRH	
003CH	ILL	
003DH	ILH	
003EH	Reserved	
003FH	PSW	

Note 1: Do not access reserved areas by the program.

Note 2: – ; Cannot be accessed.

Note 3: Write-only registers and interrupt latches cannot use the read-modify-write instructions (Bit manipulation instructions such as SET, CLR, etc. and logical operation instructions such as AND, OR, etc.).

4.2 DBR

Address	Read	Write
0F80H	Reserved	
0F81H	Reserved	
0F82H	Reserved	
0F83H	Reserved	
0F84H	Reserved	
0F85H	Reserved	
0F86H	Reserved	
0F87H	Reserved	
0F88H	Reserved	
0F89H	Reserved	
0F8AH	Reserved	
0F8BH	Reserved	
0F8CH	Reserved	
0F8DH	Reserved	
0F8EH	Reserved	
0F8FH	Reserved	
0F90H	SBISRA	SBICRA
0F91H	SBIDBR	
0F92H	-	I2CAR
0F93H	SBISRB	SBICRB
0F94H	Reserved	
0F95H	UART1SR	UART1CR1
0F96H	-	UART1CR2
0F97H	RD1BUF	TD1BUF
0F98H	UART2SR	UART2CR1
0F99H	-	UART2CR2
0F9AH	RD2BUF	TD2BUF
0F9BH	P6CR1	
0F9CH	P6CR2	
0F9DH	P7CR1	
0F9EH	P7CR2	
0F9FH	-	STOPCR

Address	Read	Write
0FA0H	Reserved	
: :	: :	
0FBFH	Reserved	

Address	Read	Write
0FC0H	Reserved	
: :	: :	
0FDFH	Reserved	

Address	Read	Write
0FE0H	Reserved	
0FE1H	Reserved	
0FE2H	Reserved	
0FE3H	Reserved	
0FE4H	Reserved	
0FE5H	Reserved	
0FE6H	Reserved	
0FE7H	Reserved	
0FE8H	Reserved	
0FE9H	Reserved	
0FEAH	Reserved	
0FEBH	Reserved	
0FECH	Reserved	
0FEDH	Reserved	
0FEEH	Reserved	
0FEFH	Reserved	
0FF0H	Reserved	
0FF1H	Reserved	
0FF2H	Reserved	
0FF3H	Reserved	
0FF4H	Reserved	
0FF5H	Reserved	
0FF6H	Reserved	
0FF7H	Reserved	
0FF8H	Reserved	
0FF9H	Reserved	
0FFAH	Reserved	
0FFBH	Reserved	
0FFCH	Reserved	
0FFDH	Reserved	
0FFEH	Reserved	
0FFFH	FLSCR	

Note 1: Do not access reserved areas by the program.

Note 2: – ; Cannot be accessed.

Note 3: Write-only registers and interrupt latches cannot use the read-modify-write instructions (Bit manipulation instructions such as SET, CLR, etc. and logical operation instructions such as AND, OR, etc.).

5. I/O Ports

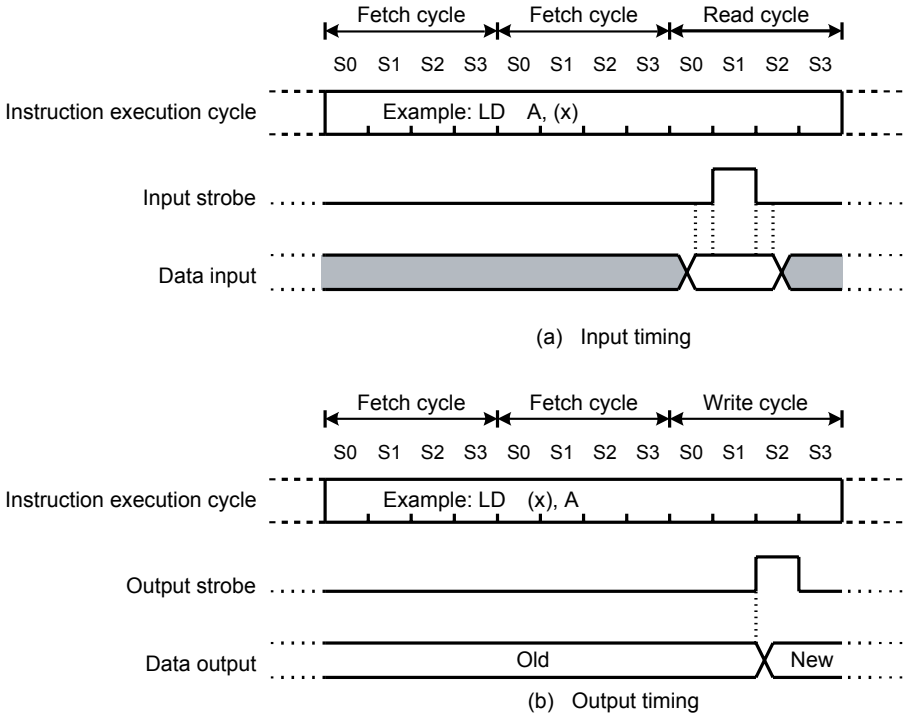
The T5CL8 has 8 parallel input/output ports (56 pins) as follows.

	Primary Function	Secondary Functions
Port P0	8-bit I/O port	External interrupt, Serial PROM mode cotrol input, serial interface input/output, UART input/output.
Port P1	8-bit I/O port	External interrupt, timer counter input/output, divider output.
Port P2	3-bit I/O port	Low-frequency resonator connections, external interrupt input, STOP mode release signal input.
Port P3	8-bit I/O port	
Port P4	8-bit I/O port	Serial interface input/output and UART input/output.
Port P5	5-bit I/O port	Serial bus interface input/output.
Port P6	8-bit I/O port	Analog input and key-on wakeup input.
Port P7	8-bit I/O port	Analog input.

Each output port contains a latch, which holds the output data. All input ports do not have latches, so the external input data should be externally held until the input data is read from outside or reading should be performed several times before processing. Figure 5-1 shows input/output timing examples.

External data is read from an I/O port in the S1 state of the read cycle during execution of the read instruction. This timing cannot be recognized from outside, so that transient input such as chattering must be processed by the program.

Output data changes in the S2 state of the write cycle during execution of the instruction which writes to an I/O port.



Note: The positions of the read and write cycles may vary, depending on the instruction.

Figure 5-1 Input/Output Timing (Example)

5.1 Port P0 (P07 to P00)

Port P0 is an 8-bit input/output port.

Port P0 is also used as an external interrupt input, Serial PROM mode control input, a serial interface input/output and an UART input/output.

When used as an input port, an external interrupt input, a serial interface input/output and an UART input/output, the corresponding output latch (P0DR) should be set to "1".

During reset, the P0DR is initialized to "1", and the P0OUTCR is initialized to "0".

It can be selected whether output circuit of P0 port is a C-MOS output or a sink open drain individually, by setting P0OUTCR. When a corresponding bit of P0OUTCR is "0", the output circuit is selected to a sink open drain and when a corresponding bit of P0OUTCR is "1", the output circuit is selected to a C-MOS output.

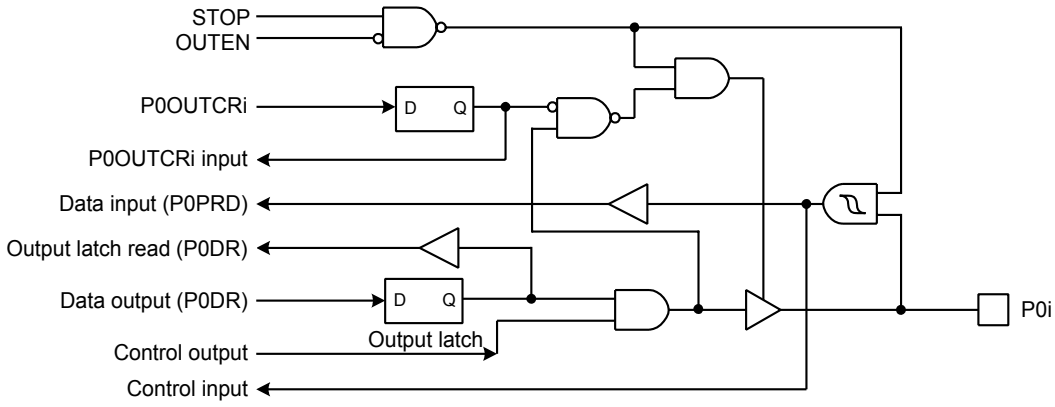
When used as an input port, an external interrupt input, a serial interface input and an UART input, the corresponding output control (P0OUTCR) should be set to "0" after P0DR is set to "1".

P0 port output latch (P0DR) and P0 port terminal input (P0PRD) are located on their respective address.

When read the output latch data, the P0DR should be read. When read the terminal input data, the P0PRD register should be read.

Table 5-1 Register Programming for Multi-function Ports (P07 to P00)

Function	Programmed Value	
	P0DR	P0OUTCR
Port input, external interrupt input, serial interface input or UART input, Serial PROM mode cotrol input	“1”	“0”
Port “0” output	“0”	Programming for each applications
Port “1” output, serial interface output or UART output	“1”	



Note: i = 7 to 0

Figure 5-2 Port 0 and P0OUTCR

P0DR (0000H) R/W

7	6	5	4	3	2	1	0
P07 INT2	P06 $\overline{SCK1}$	P05 SO1	P04 SI1	P03 INT1	P02 TXD1	P01 RXD1 BOOT	P00 $\overline{INT0}$

(Initial value: 1111 1111)

P0OUTCR (0008H)

(Initial value: 0000 0000)

P0OUTCR	Port P0 output circuit control (Set for each bit individually)	0: Sink open-drain output 1: C-MOS output	R/W

P0PRD (000BH) Read only

P07	P06	P05	P04	P03	P02	P01	P00

5.2 Port P1 (P17 to P10)

Port P1 is an 8-bit input/output port which can be configured as an input or output in one-bit unit.

Port P1 is also used as a timer/counter input/output, an external interrupt input and a divider output.

Input/output mode is specified by the P1 control register (P1CR).

During reset, the P1CR is initialized to "0" and port P1 becomes an input mode. And the P1DR is initialized to "0".

When used as an input port, a timer/counter input and an external interrupt input, the corresponding bit of P1CR should be set to "0".

When used as an output port, the corresponding bit of P1CR should be set to "1".

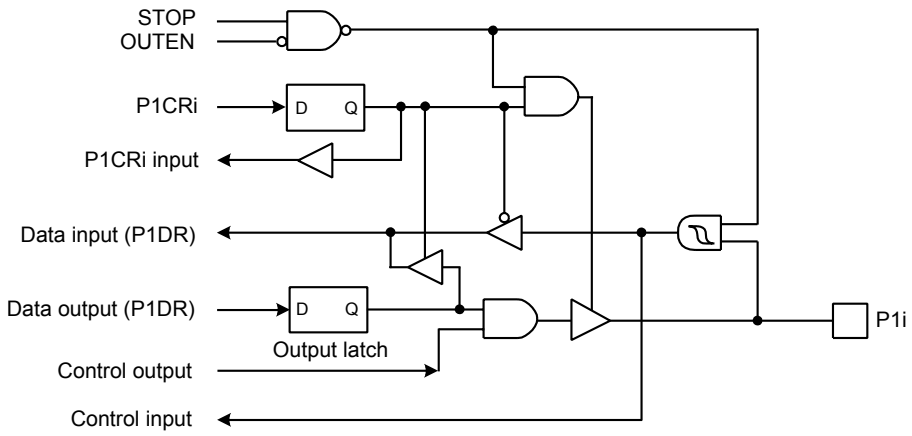
When used as a timer/counter output and a divider output, P1DR is set to "1" beforehand and the corresponding bit of P1CR should be set to "1".

When P1CR is "1", the content of the corresponding output latch is read by reading P1DR.

Table 5-2 Register Programming for Multi-function Ports

Function	Programmed Value	
	P1DR	P1CR
Port input, timer/counter input or external interrupt input	*	“0”
Port “0” output	“0”	“1”
Port “1” output, a timer output or a divider output	“1”	“1”

Note: Asterisk (*) indicates “1” or “0” either of which can be selected.



Note: i = 7 to 0

Figure 5-3 Port 1 and P1CR

Note: The port set to an input mode reads the terminal input data. Therefore, when the input and output modes are used together, the content of the output latch which is specified as input mode might be changed by executing a bit Manipulation instruction.

P1DR (0001H) R/W

7	6	5	4	3	2	1	0
P17 TC6 $\overline{\text{PWM6}}$ $\overline{\text{PDO6}}$ $\overline{\text{PPG6}}$	P16 TC5 $\overline{\text{PWM5}}$ $\overline{\text{PDO5}}$	P15 TC2 INT3	P14 TC4 $\overline{\text{PWM4}}$ $\overline{\text{PDO4}}$ $\overline{\text{PPG4}}$	P13 TC3 $\overline{\text{PWM3}}$ $\overline{\text{PDO3}}$	P12 $\overline{\text{PPG}}$	P11 $\overline{\text{DVO}}$	P10 TC1

(Initial value: 0000 0000)

P1CR (0009H)

7	6	5	4	3	2	1	0

(Initial value: 0000 0000)

P1CR	I/O control for port P1 (Specified for each bit)	0: Input mode 1: Output mode	R/W

5.3 Port P2 (P22 to P20)

Port P2 is a 3-bit input/output port.

It is also used as an external interrupt, a STOP mode release signal input, and low-frequency crystal oscillator connection pins. When used as an input port or a secondary function pins, respective output latch (P2DR) should be set to "1".

During reset, the P2DR is initialized to "1".

A low-frequency crystal oscillator (32.768 kHz) is connected to pins P21 (XTIN) and P22 (XTOUT) in the dual-clock mode. In the single-clock mode, pins P21 and P22 can be used as normal input/output ports.

It is recommended that pin P20 should be used as an external interrupt input, a STOP mode release signal input, or an input port. If it is used as an output port, the interrupt latch is set on the falling edge of the output pulse.

P2 port output latch (P2DR) and P2 port terminal input (P2PRD) are located on their respective address.

When read the output latch data, the P2DR should be read and when read the terminal input data, the P2PRD register should be read. If a read instruction is executed for port P2, read data of bits 7 to 3 are unstable.

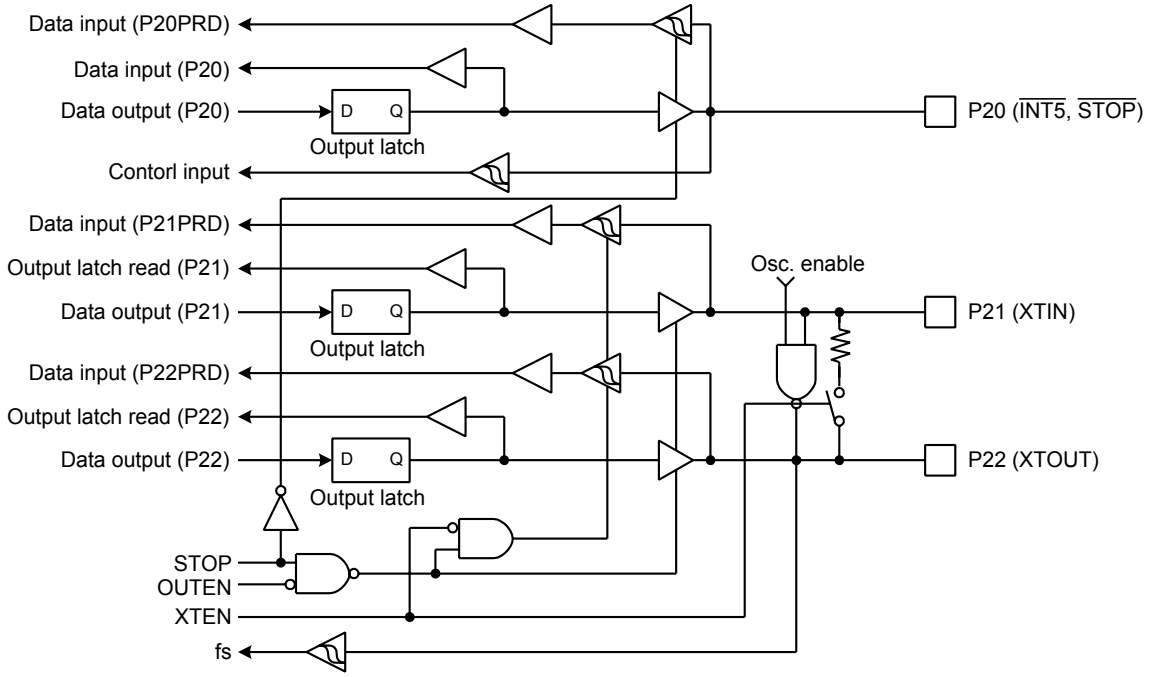


Figure 5-4 Port 2

	7	6	5	4	3	2	1	0	
P2DR (0002H) R/W						P22 XTOUT	P21 XTIN	P20 INT5 STOP	(Initial value: **** *111)
P2PRD (000CH) Read only						P22	P21	P20	

Note: Port P20 is used as $\overline{\text{STOP}}$ pin. Therefore, when stop mode is started, OUTEN does not affect to P20, and P20 becomes high-Z mode.

5.4 Port P3 (P37 to P30) (Large Current Port)

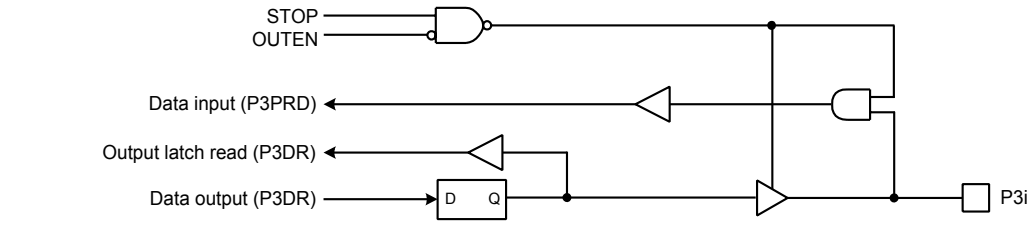
Port P3 is an 8-bit input/output port.

When used as an input port, the corresponding output latch (P3DR) should be set to "1".

During reset, the P3DR is initialized to "1".

P3 port output latch (P3DR) and P3 port terminal input (P3PRD) are located on their respective address.

When read the output latch data, the P3DR should be read. When read the terminal input data, the P3PRD register should be read.



Note: i = 7 to 0

Figure 5-5 Port 3

	7	6	5	4	3	2	1	0	
P3DR (0003H) R/W	P37	P36	P35	P34	P33	P32	P31	P30	(Initial value: 1111 1111)
P3PRD (000DH) Read only	P37	P36	P35	P34	P33	P32	P31	P30	

5.5 Port P4 (P47 to P40)

Port P4 is an 8-bit input/output port.

Port P4 is also used as a serial interface input/output and an UART input/output.

When used as an input port, a serial interface input/output and an UART input/output, the corresponding output latch (P4DR) should be set to "1".

During reset, the P4DR is initialized to "1", and the P4OUTCR is initialized to "0".

It can be selected whether output circuit of P4 port is a C-MOS output or a sink open drain individually, by setting P4OUTCR. When a corresponding bit of P4OUTCR is "0", the output circuit is selected to a sink open drain and when a corresponding bit of P4OUTCR is "1", the output circuit is selected to a C-MOS output.

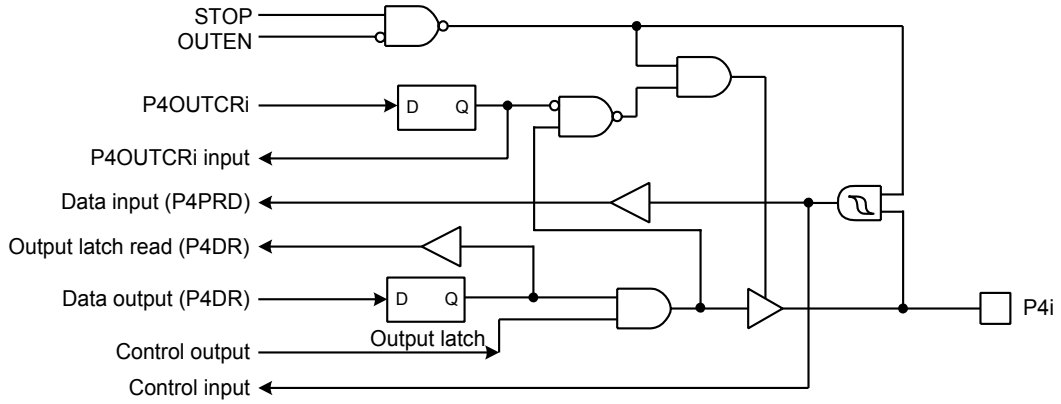
When used as an input port, a serial interface input and an UART input, the corresponding output control (P4OUTCR) should be set to "0" after P4DR is set to "1".

P4 port output latch (P4DR) and P4 port terminal input (P4PRD) are located on their respective address.

When read the output latch data, the P4DR should be read. When read the terminal input data, the P4PRD register should be read.

Table 5-3 Register Programming for Multi-function Ports (P47 to P40)

Function	Programmed Value	
	P4DR	P4OUTCR
Port input UART input or serial interface input	“1”	“0”
Port “0” output	“0”	Programming for each applica-tions
Port “1” output UART output or serial interface output	“1”	



Note: i = 7 to 0

Figure 5-6 Port 4

P4DR (0004H) R/W

7	6	5	4	3	2	1	0
P47	P46 $\overline{SCK2}$	P45 SO2	P44 SI2	P43	P42 TXD2	P41 RXD2	P40

(Initial value: 1111 1111)

P4OUTCR (000AH)

(Initial value: 0000 0000)

P4OUTCR	Port P4 output circuit control (Set for each bit individually)	0: Sink open-drain output 1: C-MOS output	R/W

P4PRD (000EH) Read only

P47	P46	P45	P44	P43	P42	P41	P40

5.6 Port P5 (P54 to P50) (Large Current Port)

Port P5 is an 5-bit input/output port.

Port P5 is also used as an I^2C Bus input/output.

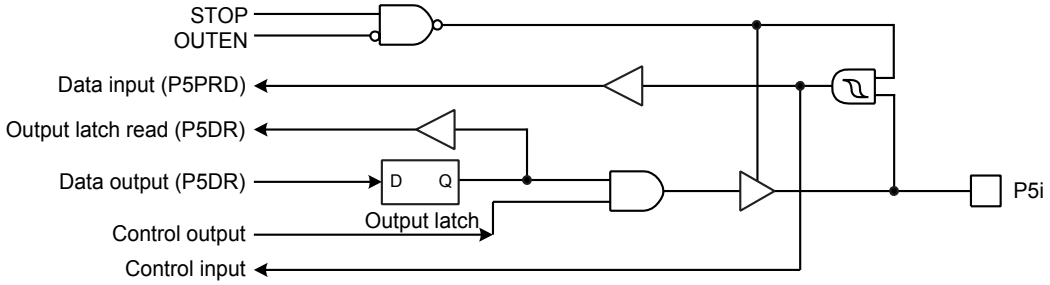
When used as an input port and I^2C Bus input/output, the corresponding output latch (P5DR) should be set to "1".

During reset, the P5DR is initialized to "1".

P5 port output latch (P5DR) and P5 port terminal input (P5PRD) are located on their respective address.

When read the output latch data, the P5DR should be read. When read the terminal input data, the P5PRD register should be read.

If a read instruction is executed for port P5, read data of bit 7 to 5 are unstable.



Note: i = 4 to 0

Figure 5-7 Port 5

P5DR (0005H) R/W

7	6	5	4	3	2	1	0
			P54	P53	P52	P51 SDA	P50 SCL

(Initial value: ***1 1111)

P5PRD (000FH) Read only

			P54	P53	P52	P51	P50

5.7 Port P6 (P67 to P60)

Port P6 is an 8-bit input/output port which can be configured as an input or output in one-bit unit.

Port P6 is also used as an analog input and key-on wakeup input.

Input/output mode is specified by the P6 control register (P6CR1) and P6 input control register (P6CR2).

During reset, the P6CR1 is initialized to "0" the P6CR2 is initialized to "1" and port P6 becomes an input mode. And the P6DR is initialized to "0".

When used as an output port, the corresponding bit of P6CR1 should be set to "1".

When used as an input port , the corresponding bit of P6CR1 should be set to "0" and then, the corresponding bit of P6CR2 should be set to "1".

When used as a key-on wakeup input , the corresponding bit of P6CR1 should be set to "0" and then, the corresponding bit of STOPkEN should be set to "1".

When used as an analog input, the corresponding bit of P6CR1 should be set to "0" and then, the corresponding bit of P6CR2 should be set to "0".

When P6CR1 is "1", the content of the corresponding output latch is read by reading P6DR.

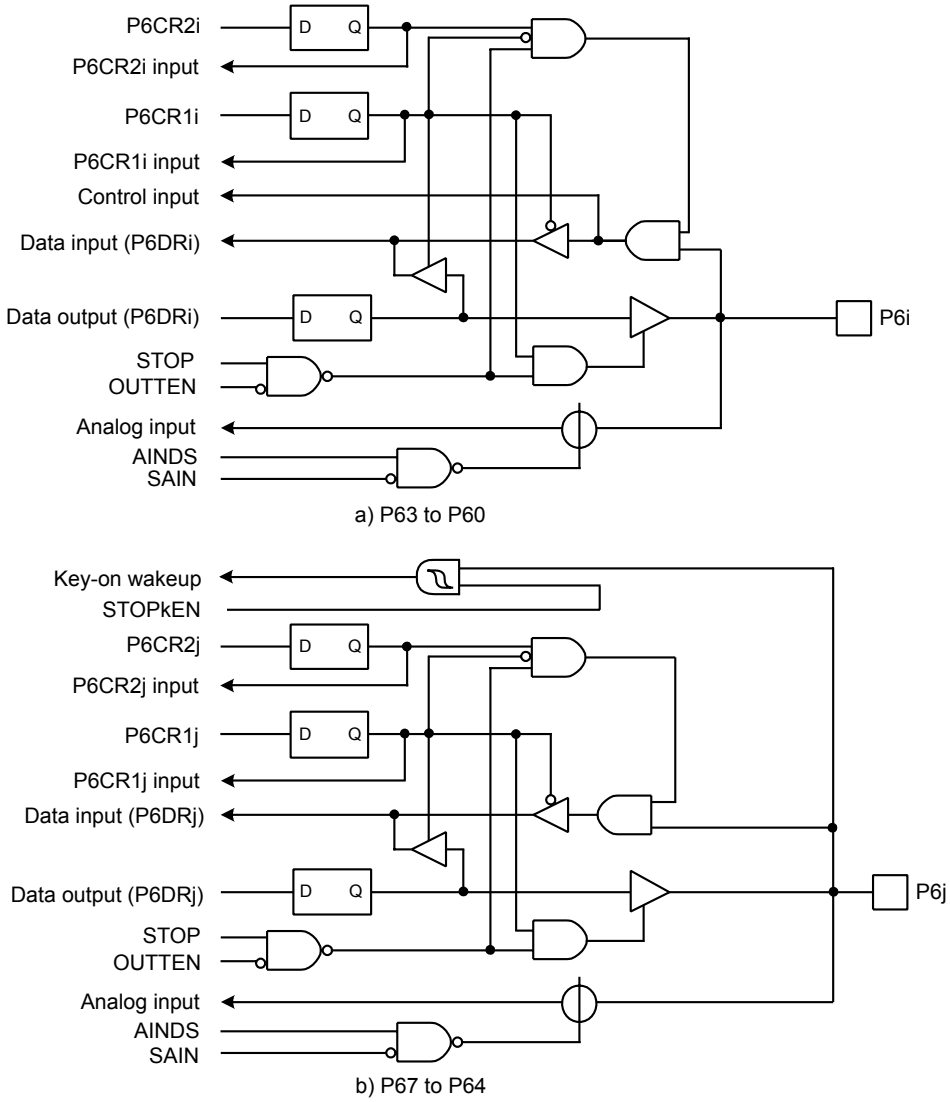
Table 5-4 Register Programming for Multi-function Ports

Function	Programmed Value			
	P6DR	P6CR1	P6CR2	STOPkEN
Port input	*	“0”	“1”	*
Key-on wakeup input	*	"0"	*	"1"
Analog input	*	“0”	“0”	*
Port “0” output	“0”	“1”	*	*
Port “1” output	“1”	“1”	*	*

Note: Asterisk (*) indicates “1” or “0” either of which can be selected.

Table 5-5 Values Read from P6DR and Register Programming

Conditions		Values Read from P6DR
P6CR1	P6CR2	
“0”	“0”	“0”
“0”	“1”	Terminal input data
“1”	“0”	Output latch contents
	“1”	



Note 1: i = 3 to 0, j = 7 to 4, k = 3 to 0
Note 2: STOP is bit7 in SYSCR1.
Note 3: SAIN is AD input select signal.
Note 4: STOPkEN is input select signal in a key-on wakeup.

Figure 5-8 Port 6, P6CR1 and P6CR2

P6DR (0006H) R/W

7	6	5	4	3	2	1	0
P67 AIN7 STOP3	P66 AIN6 STOP2	P65 AIN5 STOP1	P64 AIN4 STOP0	P63 AIN3	P62 AIN2	P61 AIN1	P60 AIN0

(Initial value: 0000 0000)

P6CR1 (0F9BH)

7	6	5	4	3	2	1	0

(Initial value: 0000 0000)

P6CR1	I/O control for port P6 (Specified for each bit)	0: Input mode 1: Output mode	R/W

P6CR2 (0F9CH)

7	6	5	4	3	2	1	0

(Initial value: 1111 1111)

P6CR2	P6 port input control (Specified for each bit)	0: Analog input 1: Port input	R/W

Note 1: The port placed in input mode reads the pin input state. Therefore, when the input and output modes are used together, the output latch contents for the port in input mode might be changed by executing a bit manipulation instruction.

Note 2: When used as an analog inport, be sure to clear the corresponding bit of P6CR2 to disable the port input.

Note 3: Do not set the output mode (P6CR1 = “1”) for the pin used as an analog input pin.

Note 4: Pins not used for analog input can be used as I/O ports. During AD conversion, output instructions should not be executed to keep a precision. In addition, a variable signal should not be input to a port adjacent to the analog input during AD conversion.

5.8 Port P7 (P77 to P70)

Port P7 is an 8-bit input/output port which can be configured as an input or output in one-bit unit.

Port P7 is also used as an analog input.

Input/output mode is specified by the P7 control register (P7CR1) and P7 input control register (P7CR2).

During reset, the P7CR1 is initialized to "0" the P7CR2 is initialized to "1" and port P7 becomes an input mode. And the P7DR is initialized to "0".

When used as an output port, the corresponding bit of P7CR1 should be set to "1".

When used as an input port, the corresponding bit of P7CR1 should be set to "0" and then, the corresponding bit of P7CR2 should be set to "1".

When used as an analog input, the corresponding bit of P7CR1 should be set to "0" and then, the corresponding bit of P7CR2 should be set to "0".

When P7CR1 is "1", the content of the corresponding output latch is read by reading P7DR.

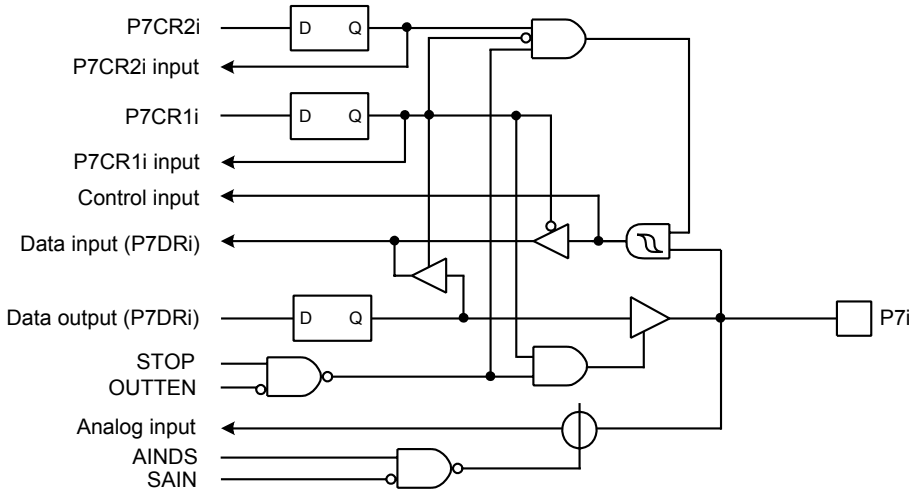
Table 5-6 Register Programming for Multi-function Ports

Function	Programmed Value		
	P7DR	P7CR1	P7CR2
Port input	*	“0”	“1”
Analog input	*	“0”	“0”
Port “0” output	“0”	“1”	*
Port “1” output	“1”	“1”	*

Note: Asterisk (*) indicates “1” or “0” either of which can be selected.

Table 5-7 Values Read from P7DR and Register Programming

Conditions		Values Read from P7DR
P7CR1	P7CR2	
“0”	“0”	“0”
“0”	“1”	Terminal input data
“1”	“0”	Output latch contents
	“1”	



Note 1: i = 7 to 0

Note 2: STOP is bit7 in SYSCR1.

Note 3: SAIN is AD input select signal.

Figure 5-9 Port 7, P7CR1 and P7CR2

P7DR (0007H) R/W

7	6	5	4	3	2	1	0
P77 AIN15	P76 AIN14	P75 AIN13	P74 AIN12	P73 AIN11	P72 AIN10	P71 AIN9	P70 AIN8

(Initial value: 0000 0000)

P7CR1 (0F9DH)

7	6	5	4	3	2	1	0

(Initial value: 0000 0000)

P7CR1	I/O control for port P7 (Specified for each bit)	0: Input mode 1: Output mode	R/W

P7CR2 (0F9EH)

7	6	5	4	3	2	1	0

(Initial value: 1111 1111)

P7CR2	P7 port input control (Specified for each bit)	0: Analog input 1: Port input	R/W

Note 1: The port placed in input mode reads the pin input state. Therefore, when the input and output modes are used together, the output latch contents for the port in input mode might be changed by executing a bit manipulation instruction.

Note 2: When used as an analog inport, be sure to clear the corresponding bit of P7CR2 to disable the port input.

Note 3: Do not set the output mode (P7CR1 = “1”) for the pin used as an analog input pin.

Note 4: Pins not used for analog input can be used as I/O ports. During AD conversion, output instructions should not be executed to keep a precision. In addition, a variable signal should not be input to a port adjacent to the analog input during AD conversion.

6. Watchdog Timer (WDT)

The watchdog timer is a fail-safe system to detect rapidly the CPU malfunctions such as endless loops due to spurious noises or the deadlock conditions, and return the CPU to a system recovery routine.

The watchdog timer signal for detecting malfunctions can be programmed only once as “reset request” or “interrupt request”. Upon the reset release, this signal is initialized to “reset request”.

When the watchdog timer is not used to detect malfunctions, it can be used as the timer to provide a periodic interrupt.

Note: Care must be taken in system design since the watchdog timer functions are not be operated completely due to effect of disturbing noise.

6.1 Watchdog Timer Configuration

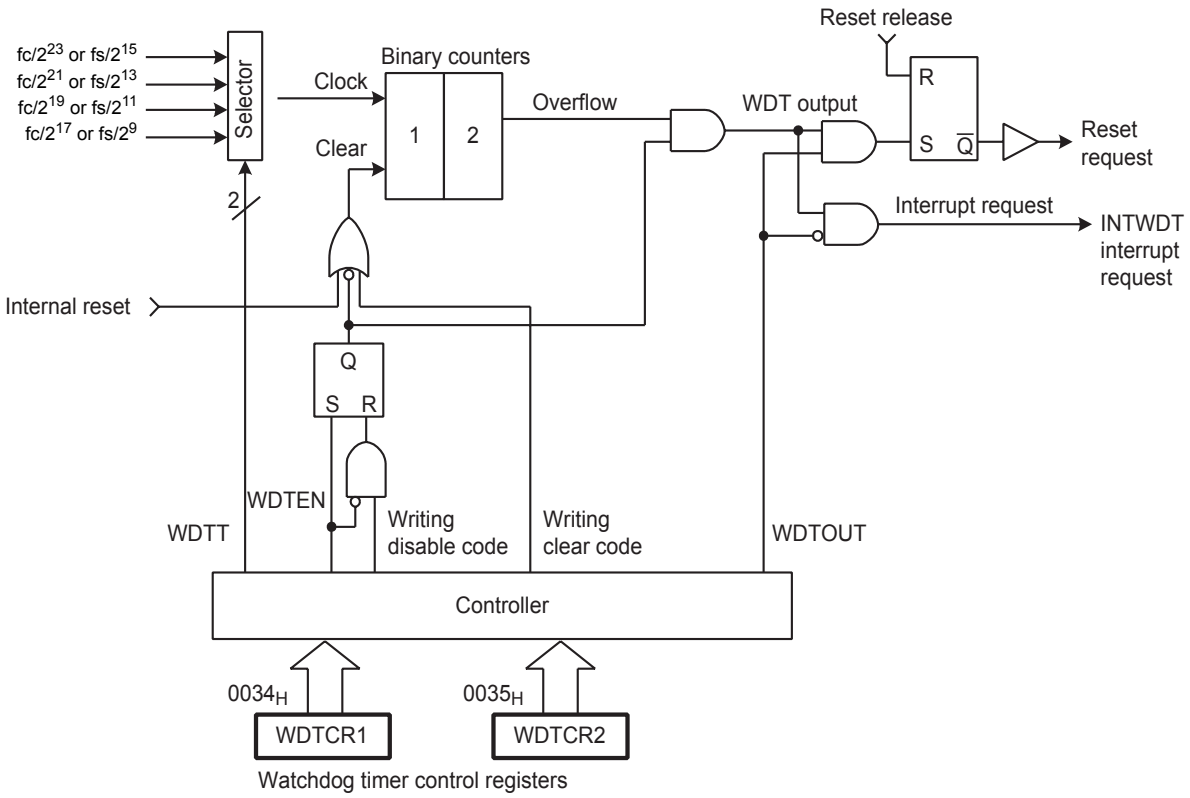


Figure 6-1 Watchdog Timer Configuration

6.2 Watchdog Timer Control

The watchdog timer is controlled by the watchdog timer control registers (WDTCR1 and WDTCR2). The watchdog timer is automatically enabled after the reset release.

6.2.1 Malfunction Detection Methods Using the Watchdog Timer

The CPU malfunction is detected, as shown below.

1. Set the detection time, select the output, and clear the binary counter.
2. Clear the binary counter repeatedly within the specified detection time.

If the CPU malfunctions such as endless loops or the deadlock conditions occur for some reason, the watchdog timer output is activated by the binary-counter overflow unless the binary counters are cleared. When WDTCR1<WDTOUT> is set to "1" at this time, the reset request is generated and then internal hardware is initialized. When WDTCR1<WDTOUT> is set to "0", a watchdog timer interrupt (INTWDT) is generated.

The watchdog timer temporarily stops counting in the STOP mode including the warm-up or IDLE/SLEEP mode, and automatically restarts (continues counting) when the STOP/IDLE/SLEEP mode is inactivated.

Note: The watchdog timer consists of an internal divider and a two-stage binary counter. When the clear code 4EH is written, only the binary counter is cleared, but not the internal divider. The minimum binary-counter overflow time, that depends on the timing at which the clear code (4EH) is written to the WDTCR2 register, may be 3/4 of the time set in WDTCR1<WDTT>. Therefore, write the clear code using a cycle shorter than 3/4 of the time set to WDTCR1<WDTT>.

Example :Setting the watchdog timer detection time to 2^{21}/fc [s], and resetting the CPU malfunction detection

```
        LD      (WDTCR2), 4EH       : Clears the binary counters.
        LD      (WDTCR1), 00001101B : WDTT ← 10, WDTOUT ← 1
        LD      (WDTCR2), 4EH       : Clears the binary counters (always clears immediately before and
                                      after changing WDTT).
Within  :
3/4 of  :
WDT
detect  LD      (WDTCR2), 4EH       : Clears the binary counters.
time
        :
Within  :
3/4 of
WDT     LD      (WDTCR2), 4EH       : Clears the binary counters.
detect
time
```

Watchdog Timer Control Register 1

WDTCR1 (0034H)

7	6	5	4	3	2	1	0
		(ATAS)	(ATOUT)	WDTEN	WDTT		WDTOUT

(Initial value: **11 1001)

WDTEN	Watchdog timer enable/disable	0: Disable (Writing the disable code to WDTCR2 is required.) 1: Enable				Write only
WDTT	Watchdog timer detection time [s]		NORMAL1/2 mode		SLOW1/2 mode	Write only
			DV7CK = 0	DV7CK = 1		
		00	2^{25}/fc	2^{17}/fs	2^{17}/fs	
		01	2^{23}/fc	2^{15}/fs	2^{15}fs	
		10	2^{21}fc	2^{13}/fs	2^{13}fs	
		11	2^{19}/fc	2^{11}/fs	2^{11}/fs	
WDTOUT	Watchdog timer output select	0: Interrupt request 1: Reset request				Write only

Note 1: After clearing WDTOUT to “0”, the program cannot set it to “1”.

Note 2: fc: High-frequency clock [Hz], fs: Low-frequency clock [Hz], *: Don’t care

Note 3: WDTCR1 is a write-only register and must not be used with any of read-modify-write instructions. If WDTCR1 is read, a don’t care is read.

Note 4: To activate the STOP mode, disable the watchdog timer or clear the counter immediately before entering the STOP mode. After clearing the counter, clear the counter again immediately after the STOP mode is inactivated.

Note 5: To clear WDTEN, set the register in accordance with the procedures shown in “6.2.3 Watchdog Timer Disable”.

Watchdog Timer Control Register 2

WDTCR2 (0035H)

7	6	5	4	3	2	1	0

(Initial value: **** ****)

WDTCR2	Write Watchdog timer control code	4EH: Clear the watchdog timer binary counter (Clear code) B1H: Disable the watchdog timer (Disable code) D2H: Enable assigning address trap area Others: Invalid	Write only

Note 1: The disable code is valid only when WDTCR1<WDTEN> = 0.

Note 2: *: Don’t care

Note 3: The binary counter of the watchdog timer must not be cleared by the interrupt task.

Note 4: Write the clear code 4EH using a cycle shorter than 3/4 of the time set in WDTCR1<WDTT>.

6.2.2 Watchdog Timer Enable

Setting WDTCR1<WDTEN> to “1” enables the watchdog timer. Since WDTCR1<WDTEN> is initialized to “1” during reset, the watchdog timer is enabled automatically after the reset release.

6.2.3 Watchdog Timer Disable

To disable the watchdog timer, set the register in accordance with the following procedures. Setting the register in other procedures causes a malfunction of the microcontroller.

1. Set the interrupt master flag (IMF) to “0”.
2. Set WDTCR2 to the clear code (4EH).
3. Set WDTCR1<WDTEN> to “0”.
4. Set WDTCR2 to the disable code (B1H).

Note: While the watchdog timer is disabled, the binary counters of the watchdog timer are cleared.

Example :Disabling the watchdog timer

```
DI                          : IMF ← 0
LD      (WDTCR2), 04EH      : Clears the binary counter
LDW     (WDTCR1), 0B101H    : WDTEN ← 0, WDTCR2 ← Disable code
```

Table 6-1 Watchdog Timer Detection Time (Example: fc = 16.0 MHz, fs = 32.768 kHz)

WDTT	Watchdog Timer Detection Time[s]		
	NORMAL1/2 mode		SLOW mode
	DV7CK = 0	DV7CK = 1	
00	2.097	4	4
01	524.288 m	1	1
10	131.072 m	250 m	250 m
11	32.768 m	62.5 m	62.5 m

6.2.4 Watchdog Timer Interrupt (INTWDT)

When WDTCR1<WDTOUT> is cleared to “0”, a watchdog timer interrupt request (INTWDT) is generated by the binary-counter overflow.

A watchdog timer interrupt is the non-maskable interrupt which can be accepted regardless of the interrupt master flag (IMF).

When a watchdog timer interrupt is generated while the other interrupt including a watchdog timer interrupt is already accepted, the new watchdog timer interrupt is processed immediately and the previous interrupt is held pending. Therefore, if watchdog timer interrupts are generated continuously without execution of the RETN instruction, too many levels of nesting may cause a malfunction of the microcontroller.

To generate a watchdog timer interrupt, set the stack pointer before setting WDTCR1<WDTOUT>.

Example :Setting watchdog timer interrupt

```
LD      SP, 083FH           : Sets the stack pointer
LD      (WDTCR1), 00001000B : WDTOUT ← 0
```

6.2.5 Watchdog Timer Reset

When a binary-counter overflow occurs while WDTCR1<WDTOUT> is set to “1”, a watchdog timer reset request is generated. When a watchdog timer reset request is generated, the internal hardware is reset. The reset time is maximum 24/fc [s] (1.5 μs @ fc = 16.0 MHz).

Note: When a watchdog timer reset is generated in the SLOW1 mode, the reset time is maximum 24/fc (high-frequency clock) since the high-frequency clock oscillator is restarted. However, when crystals have inaccuracies upon start of the high-frequency clock oscillator, the reset time should be considered as an approximate value because it has slight errors.

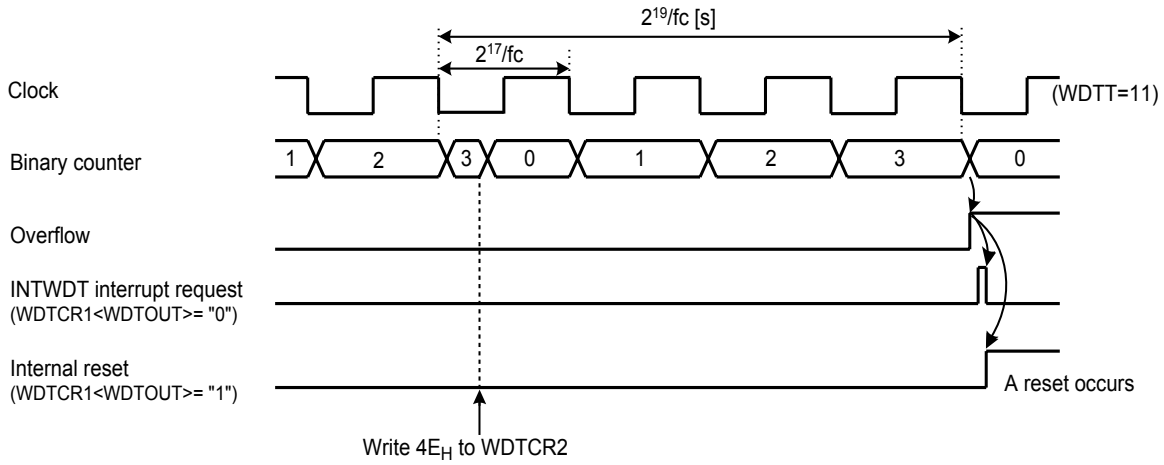


Figure 6-2 Watchdog Timer Interrupt

6.3 Address Trap

The Watchdog Timer Control Register 1 and 2 share the addresses with the control registers to generate address traps.

Watchdog Timer Control Register 1

WDTCR1 (0034H)	7	6	5	4	3	2	1	0
			ATAS	ATOUT	(WDTEN)	(WDTT)		(WDTOUT)

(Initial value: **11 1001)

ATAS	Select address trap generation in the internal RAM area	0: Generate no address trap 1: Generate address traps (After setting ATAS to "1", writing the control code D2H to WDTCR2 is required)	Write only
ATOUT	Select operation at address trap	0: Interrupt request 1: Reset request	

Watchdog Timer Control Register 2

WDTCR2 (0035H)	7	6	5	4	3	2	1	0

(Initial value: **** ****)

WDTCR2	Write Watchdog timer control code and address trap area control code	D2H: Enable address trap area selection (ATRAP control code) 4EH: Clear the watchdog timer binary counter (WDT clear code) B1H: Disable the watchdog timer (WDT disable code) Others: Invalid	Write only

6.3.1 Selection of Address Trap in Internal RAM (ATAS)

WDTCR1<ATAS> specifies whether or not to generate address traps in the internal RAM area. To execute an instruction in the internal RAM area, clear WDTCR1<ATAS> to "0". To enable the WDTCR1<ATAS> setting, set WDTCR1<ATAS> and then write D2H to WDTCR2.

Executing an instruction in the SFR or DBR area generates an address trap unconditionally regardless of the setting in WDTCR1<ATAS>.

6.3.2 Selection of Operation at Address Trap (ATOUT)

When an address trap is generated, either the interrupt request or the reset request can be selected by WDTCR1<ATOUT>.

6.3.3 Address Trap Interrupt (INTATRAP)

While WDTCR1<ATOUT> is "0", if the CPU should start looping for some cause such as noise and an attempt be made to fetch an instruction from the on-chip RAM (while WDTCR1<ATAS> is "1"), DBR or the SFR area, address trap interrupt (INTATRAP) will be generated.

An address trap interrupt is a non-maskable interrupt which can be accepted regardless of the interrupt master flag (IMF).

When an address trap interrupt is generated while the other interrupt including an address trap interrupt is already accepted, the new address trap is processed immediately and the previous interrupt is held pending. Therefore, if address trap interrupts are generated continuously without execution of the RETN instruction, too many levels of nesting may cause a malfunction of the microcontroller.

To generate address trap interrupts, set the stack pointer beforehand.

6.3.4 Address Trap Reset

While WDTCR1<ATOUT> is “1”, if the CPU should start looping for some cause such as noise and an attempt be made to fetch an instruction from the on-chip RAM (while WDTCR1<ATAS> is “1”), DBR or the SFR area, address trap reset will be generated.

When an address trap reset request is generated, the internal hardware is reset. The reset time is maximum 24/fc [s] (1.5 μs @ fc = 16.0 MHz).

Note: When an address trap reset is generated in the SLOW1 mode, the reset time is maximum 24/fc (high-frequency clock) since the high-frequency clock oscillator is restarted. However, when crystals have inaccuracies upon start of the high-frequency clock oscillator, the reset time should be considered as an approximate value because it has slight errors.

7. Time Base Timer (TBT)

The time base timer generates time base for key scanning, dynamic displaying, etc. It also provides a time base timer interrupt (INTTBT).

7.1 Time Base Timer

7.1.1 Configuration

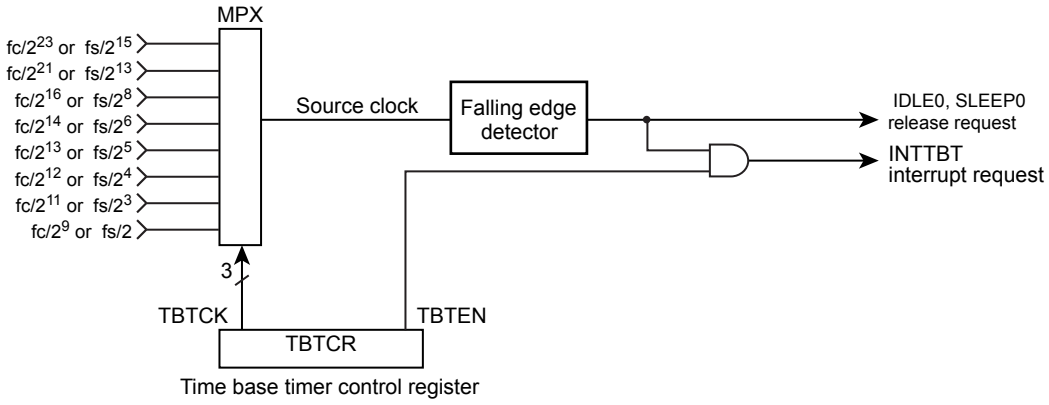


Figure 7-1 Time Base Timer configuration

7.1.2 Control

Time Base Timer is controlled by Time Base Timer control register (TBTCR).

Time Base Timer Control Register

	7	6	5	4	3	2	1	0	
TBTCR (0036H)	(DVOEN)	(DVOCK)		(DV7CK)	TBTEN	TBTCK			(Initial Value: 0000 0000)

TBTEN	Time Base Timer enable / disable	0: Disable 1: Enable				
TBTCK	Time Base Timer interrupt Frequency select : [Hz]		NORMAL1/2, IDLE1/2 Mode		SLOW1/2 SLEEP1/2 Mode	R/W
			DV7CK = 0	DV7CK = 1		
		000	fc/2^{23}	fs/2^{15}	fs/2^{15}	
		001	fc/2^{21}	fs/2^{13}	fs/2^{13}	
		010	fc/2^{16}	fs/2^{8}	–	
		011	fc/2^{14}	fs/2^{6}	–	
		100	fc/2^{13}	fs/2^{5}	–	
		101	fc/2^{12}	fs/2^{4}	–	
		110	fc/2^{11}	fs/2^{3}	–	
		111	fc/2^{9}	fs/2	–	

Note 1: fc; High-frequency clock [Hz], fs; Low-frequency clock [Hz], *; Don't care

Note 2: The interrupt frequency (TBTCK) must be selected with the time base timer disabled (TBTEN="0"). (The interrupt frequency must not be changed with the disable from the enable state.) Both frequency selection and enabling can be performed simultaneously.

Example :Set the time base timer frequency to fc/2^{16} [Hz] and enable an INTTBT interrupt.

```
LD      (TBTCR) ,  00000010B        ; TBTCK ← 010
LD      (TBTCR) ,  00001010B        ; TBTEN ← 1
DI                                  ; IMF ← 0
SET     (EIRL) . 7
```

Table 7-1 Time Base Timer Interrupt Frequency (Example : fc = 16.0 MHz, fs = 32.768 kHz)

TBTCK	Time Base Timer Interrupt Frequency [Hz]		
	NORMAL1/2, IDLE1/2 Mode	NORMAL1/2, IDLE1/2 Mode	SLOW1/2, SLEEP1/2 Mode
	DV7CK = 0	DV7CK = 1	
000	1.91	1	1
001	7.63	4	4
010	244.14	128	–
011	976.56	512	–
100	1953.13	1024	–
101	3906.25	2048	–
110	7812.5	4096	–
111	31250	16384	–

7.1.3 Function

An INTTBT (Time Base Timer Interrupt) is generated on the first falling edge of source clock (The divider output of the timing generator which is selected by TBTCK.) after time base timer has been enabled.

The divider is not cleared by the program; therefore, only the first interrupt may be generated ahead of the set interrupt period (Figure 7-2).

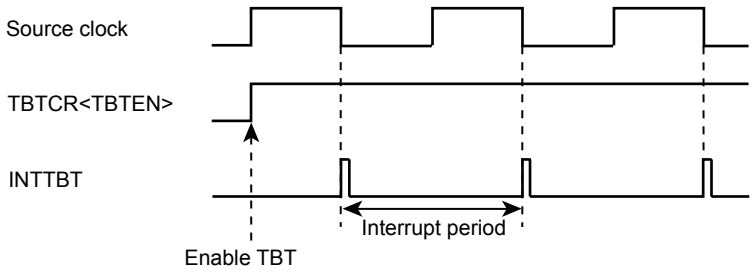


Figure 7-2 Time Base Timer Interrupt

7.2 Divider Output ($\overline{DVO}$)

Approximately 50% duty pulse can be output using the divider output circuit, which is useful for piezoelectric buzzer drive. Divider output is from $\overline{DVO}$ pin.

7.2.1 Configuration

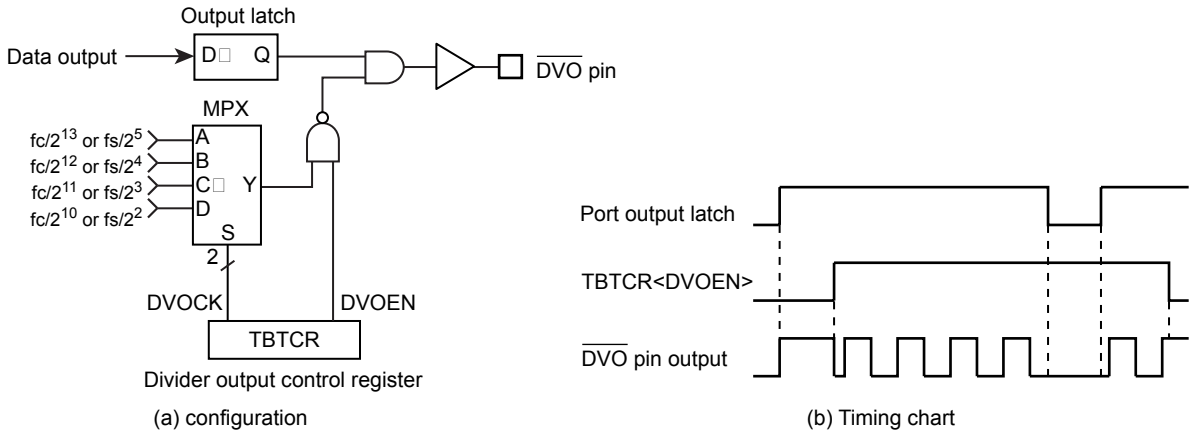


Figure 7-3 Divider Output

7.2.2 Control

The Divider Output is controlled by the Time Base Timer Control Register.

Time Base Timer Control Register

	7	6	5	4	3	2	1	0	
TBTCR (0036H)	DVOEN	DVOCK		(DV7CK)	(TBTEN)	(TBTCK)			(Initial value: 0000 0000)

DVOEN	Divider output enable / disable	0: Disable 1: Enable			R/W
DVOCK	Divider Output ($\overline{DVO}$) frequency selection: [Hz]		NORMAL1/2, IDLE1/2 Mode		SLOW1/2 SLEEP1/2 Mode	R/W
			DV7CK = 0	DV7CK = 1		
		00	fc/2^{13}	fs/2^5	fs/2^5	
		01	fc/2^{12}	fs/2^4	fs/2^4	
		10	fc/2^{11}	fs/2^3	fs/2^3	
		11	fc/2^{10}	fs/2^2	fs/2^2	

Note: Selection of divider output frequency (DVOCK) must be made while divider output is disabled (DVOEN="0"). Also, in other words, when changing the state of the divider output frequency from enabled (DVOEN="1") to disable(DVOEN="0"), do not change the setting of the divider output frequency.

Example :1.95 kHz pulse output (fc = 16.0 MHz)

```
LD      (TBTCR) ,  00000000B        ; DVOCK ← "00"
LD      (TBTCR) ,  10000000B        ; DVOEN ← "1"
```

Table 7-2 Divider Output Frequency (Example : fc = 16.0 MHz, fs = 32.768 kHz)

DVOCK	Divider Output Frequency [Hz]		
	NORMAL1/2, IDLE1/2 Mode		SLOW1/2, SLEEP1/2 Mode
	DV7CK = 0	DV7CK = 1	
00	1.953 k	1.024 k	1.024 k
01	3.906 k	2.048 k	2.048 k
10	7.813 k	4.096 k	4.096 k
11	15.625 k	8.192 k	8.192 k

8. 16-Bit TimerCounter 1 (TC1)

8.1 Configuration

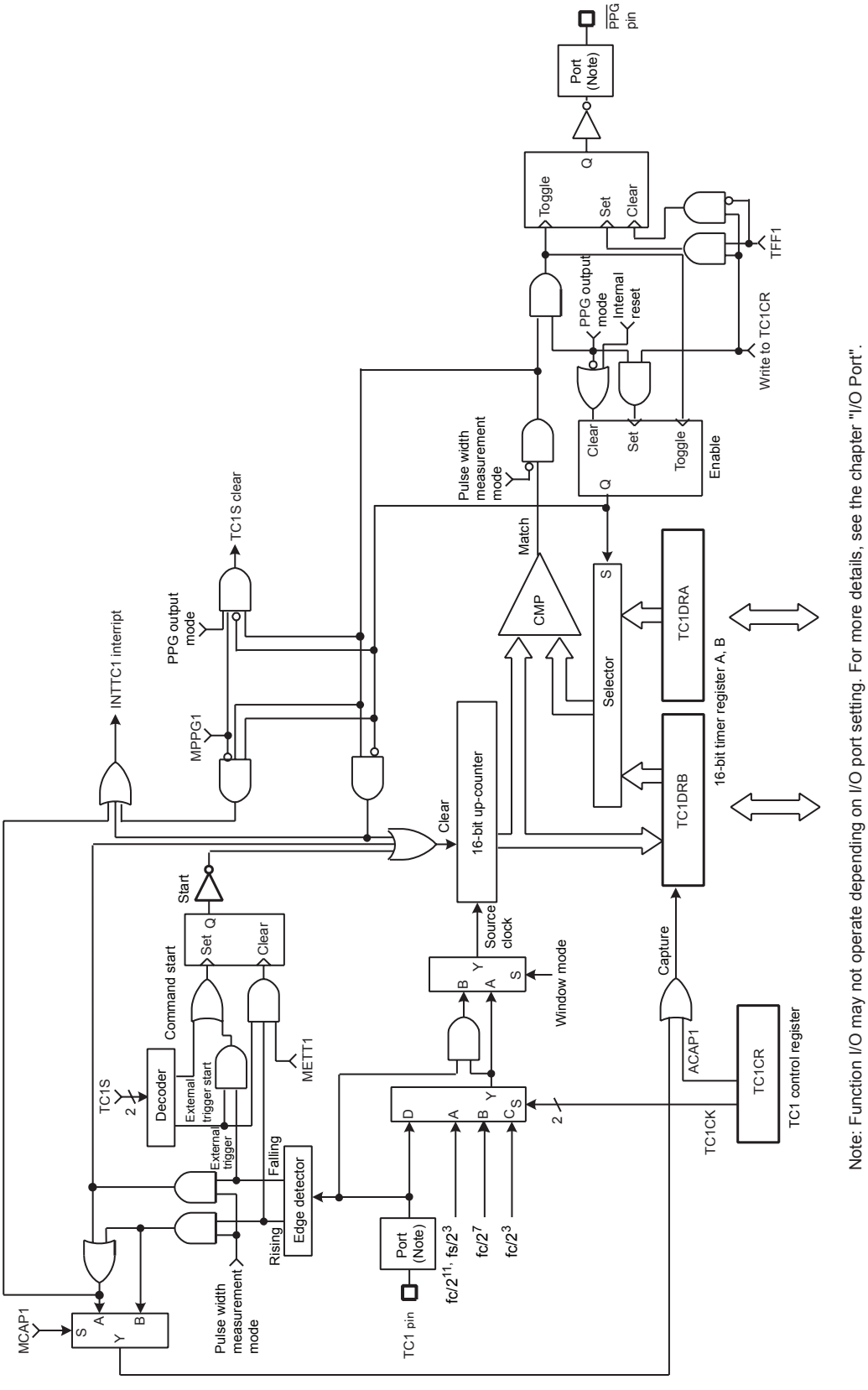


Figure 8-1 TimerCounter 1 (TC1)

8.2 TimerCounter Control

The TimerCounter 1 is controlled by the TimerCounter 1 control register (TC1CR) and two 16-bit timer registers (TC1DRA and TC1DRB).

Timer Register

	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
TC1DRA (0011H, 0010H)	TC1DRAH (0011H)	TC1DRAL (0010H)
	(Initial value: 1111 1111 1111 1111)	Read/Write
TC1DRB (0013H, 0012H)	TC1DRBH (0013H)	TC1DRBL (0012H)
	(Initial value: 1111 1111 1111 1111)	Read/Write (Write enabled only in the PPG output mode)

TimerCounter 1 Control Register

	7	6	5 4	3 2	1 0	
TC1CR (0026H)	TFF1	ACAP1 MCAP1 METT1 MPPG1	TC1S	TC1CK	TC1M	Read/Write (Initial value: 0000 0000)

TFF1	Timer F/F1 control	0: Clear			1: Set				R/W
ACAP1	Auto capture control	0:Auto-capture disable			1:Auto-capture enable				R/W
MCAP1	Pulse width measurement mode control	0:Double edge capture			1:Single edge capture				
METT1	External trigger timer mode control	0:Trigger start			1:Trigger start and stop				
MPPG1	PPG output control	0:Continuous pulse generation			1:One-shot				
TC1S	TC1 start control		Timer	Extrig-ger	Event	Win-dow	Pulse	PPG	R/W
		00: Stop and counter clear	O	O	O	O	O	O	
		01: Command start	O	–	–	–	–	O	
		10: Rising edge start (Ex-trigger/Pulse/PPG) Rising edge count (Event) Positive logic count (Window)	–	O	O	O	O	O	
		11: Falling edge start (Ex-trigger/Pulse/PPG) Falling edge count (Event) Negative logic count (Window)	–	O	O	O	O	O	
TC1CK	TC1 source clock select [Hz]		NORMAL1/2, IDLE1/2 mode				Divider	SLOW, SLEEP mode	R/W
			DV7CK = 0		DV7CK = 1				
		00	$fc/2^{11}$		$fs/2^3$		DV9	$fs/2^3$	
		01	$fc/2^7$		$fc/2^7$		DV5	–	
		10	$fc/2^3$		$fc/2^3$		DV1	–	
		11	External clock (TC1 pin input)						
TC1M	TC1 operating mode select	00: Timer/external trigger timer/event counter mode 01: Window mode 10: Pulse width measurement mode 11: PPG (Programmable pulse generate) output mode							R/W

Note 1: fc: High-frequency clock [Hz], fs: Low-frequency clock [Hz]

Note 2: The timer register consists of two shift registers. A value set in the timer register becomes valid at the rising edge of the first source clock pulse that occurs after the upper byte (TC1DRAH and TC1DRBH) is written. Therefore, write the lower byte and the upper byte in this order (it is recommended to write the register with a 16-bit access instruction). Writing only the lower byte (TC1DRAL and TC1DRBL) does not enable the setting of the timer register.

Note 3: To set the mode, source clock, PPG output control and timer F/F control, write to TC1CR during TC1S=00. Set the timer F/F1 control until the first timer start after setting the PPG mode.

Note 4: Auto-capture can be used only in the timer, event counter, and window modes.

Note 5: To set the timer registers, the following relationship must be satisfied.
TC1DRA > TC1DRB > 1 (PPG output mode), TC1DRA > 1 (other modes)

Note 6: Set TFF1 to “0” in the mode except PPG output mode.

Note 7: Set TC1DRB after setting TC1M to the PPG output mode.

Note 8: When the STOP mode is entered, the start control (TC1S) is cleared to “00” automatically, and the timer stops. After the STOP mode is exited, set the TC1S to use the timer counter again.

Note 9: Use the auto-capture function in the operative condition of TC1. A captured value may not be fixed if it's read after the execution of the timer stop or auto-capture disable. Read the capture value in a capture enabled condition.

Note 10:Since the up-counter value is captured into TC1DRB by the source clock of up-counter after setting TC1CR<ACAP1> to "1". Therefore, to read the captured value, wait at least one cycle of the internal source clock before reading TC1DRB for the first time.

8.3 Function

TimerCounter 1 has six types of operating modes: timer, external trigger timer, event counter, window, pulse width measurement, programmable pulse generator output modes.

8.3.1 Timer mode

In the timer mode, the up-counter counts up using the internal clock. When a match between the up-counter and the timer register 1A (TC1DRA) value is detected, an INTTC1 interrupt is generated and the up-counter is cleared. After being cleared, the up-counter restarts counting. Setting TC1CR<ACAP1> to “1” captures the up-counter value into the timer register 1B (TC1DRB) with the auto-capture function. Use the auto-capture function in the operative condition of TC1. A captured value may not be fixed if it's read after the execution of the timer stop or auto-capture disable. Read the capture value in a capture enabled condition. Since the up-counter value is captured into TC1DRB by the source clock of up-counter after setting TC1CR<ACAP1> to "1". Therefore, to read the captured value, wait at least one cycle of the internal source clock before reading TC1DRB for the first time.

Table 8-1 Internal Source Clock for TimerCounter 1 (Example: fc = 16 MHz, fs = 32.768 kHz)

TC1CK	NORMAL1/2, IDLE1/2 mode				SLOW, SLEEP mode	
	DV7CK = 0		DV7CK = 1			
	Resolution [μs]	Maximum Time Setting [s]	Resolution [μs]	Maximum Time Setting [s]	Resolution [μs]	Maximum Time Setting [s]
00	128	8.39	244.14	16.0	244.14	16.0
01	8.0	0.524	8.0	0.524	–	–
10	0.5	32.77 m	0.5	32.77 m	–	–

Example 1 :Setting the timer mode with source clock fc/2^{11} [Hz] and generating an interrupt 1 second later (fc = 16 MHz, TBTCR<DV7CK> = “0”)

```
LDW     (TC1DRA), 1E84H     ; Sets the timer register (1 s ÷ 2^11/fc = 1E84H)
DI                          ; IMF= “0”
SET     (EIRL). 5           ; Enables INTTC1
EI                          ; IMF= “1”
LD      (TC1CR), 00000000B  ; Selects the source clock and mode
LD      (TC1CR), 00010000B  ; Starts TC1
```

Example 2 :Auto-capture

```
LD      (TC1CR), 01010000B  ; ACAP1 ← 1
:       :
LD      WA, (TC1DRB)        ; Reads the capture value
```

Note: Since the up-counter value is captured into TC1DRB by the source clock of up-counter after setting TC1CR<ACAP1> to "1". Therefore, to read the captured value, wait at least one cycle of the internal source clock before reading TC1DRB for the first time.

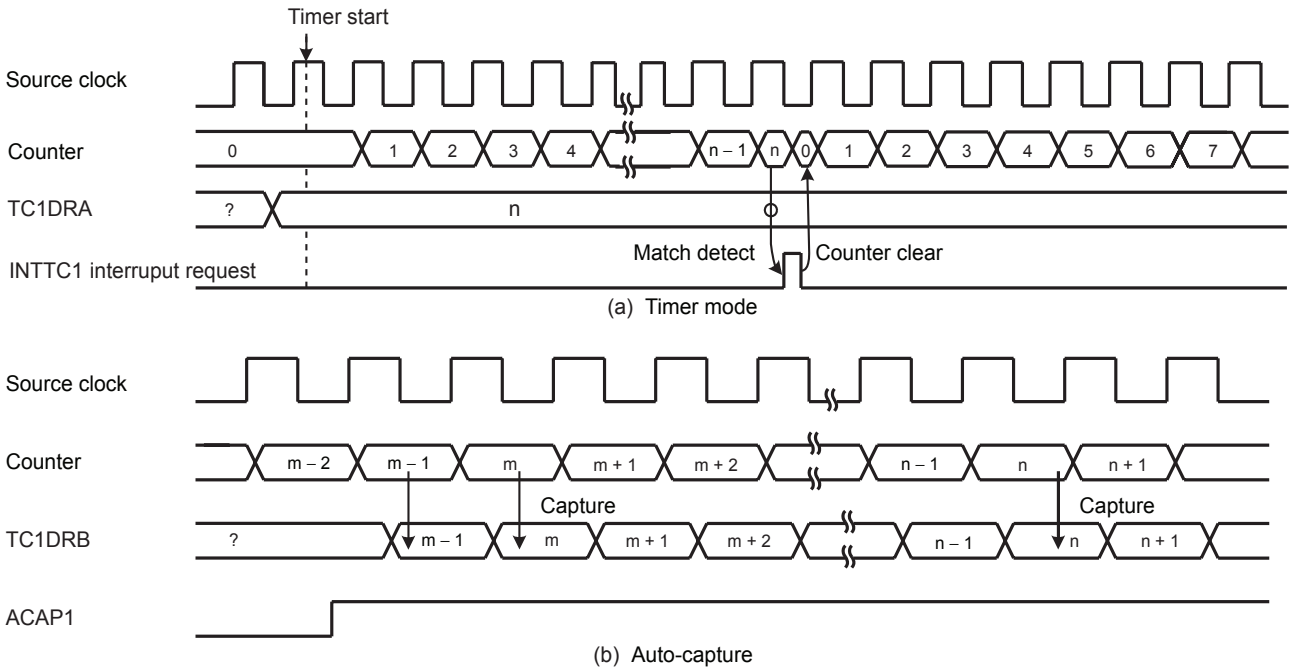


Figure 8-2 Timer Mode Timing Chart

8.3.2 External Trigger Timer Mode

In the external trigger timer mode, the up-counter starts counting by the input pulse triggering of the TC1 pin, and counts up at the edge of the internal clock. For the trigger edge used to start counting, either the rising or falling edge is defined in TC1CR<TC1S>.

- When TC1CR<METT1> is set to "1" (trigger start and stop)

  When a match between the up-counter and the TC1DRA value is detected after the timer starts, the up-counter is cleared and halted and an INTTC1 interrupt request is generated.

  If the edge opposite to trigger edge is detected before detecting a match between the up-counter and the TC1DRA, the up-counter is cleared and halted without generating an interrupt request. Therefore, this mode can be used to detect exceeding the specified pulse by interrupt.

  After being halted, the up-counter restarts counting when the trigger edge is detected.

- When TC1CR<METT1> is set to "0" (trigger start)

  When a match between the up-counter and the TC1DRA value is detected after the timer starts, the up-counter is cleared and halted and an INTTC1 interrupt request is generated.

  The edge opposite to the trigger edge has no effect in count up. The trigger edge for the next counting is ignored if detecting it before detecting a match between the up-counter and the TC1DRA.

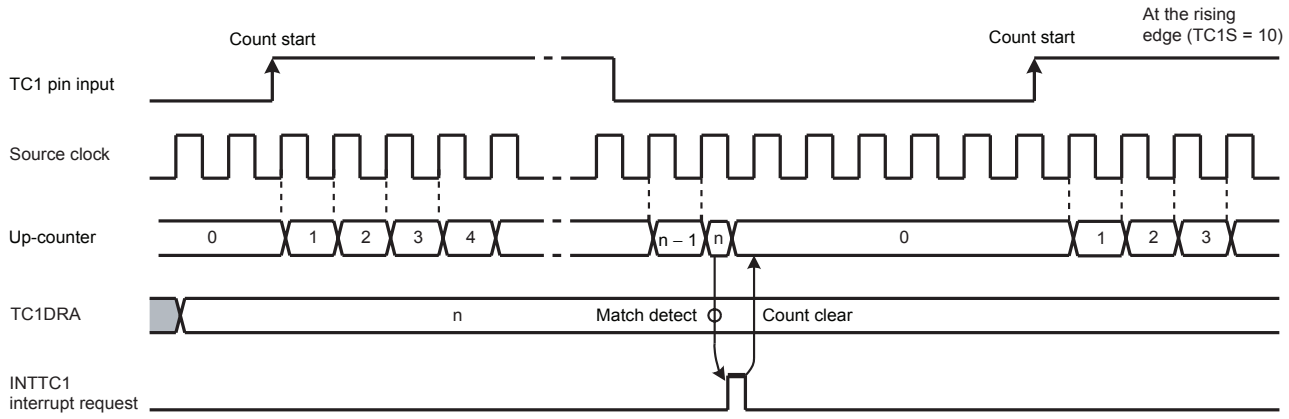
Since the TC1 pin input has the noise rejection, pulses of 4/fc [s] or less are rejected as noise. A pulse width of 12/fc [s] or more is required to ensure edge detection. The rejection circuit is turned off in the SLOW1/2 or SLEEP1/2 mode, but a pulse width of one machine cycle or more is required.

Example 1 :Generating an interrupt 1 ms after the rising edge of the input pulse to the TC1 pin (fc =16 MHz)

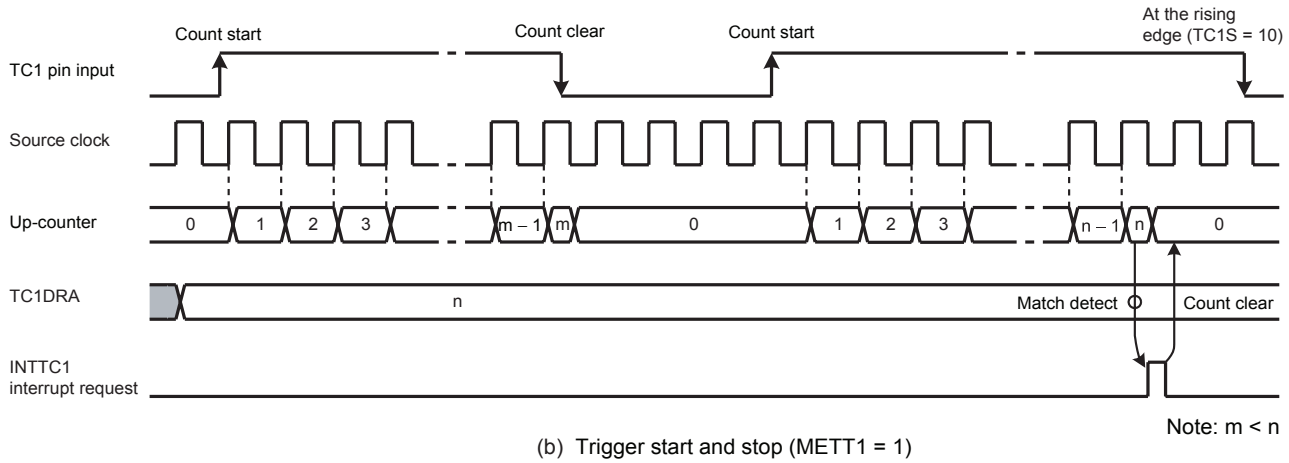
```
LDW     (TC1DRA), 007DH     ; 1ms ÷ 2^7/fc = 7DH
DI                          ; IMF= "0"
SET     (EIRL). 5           ; Enables INTTC1 interrupt
EI                          ; IMF= "1"
LD      (TC1CR), 00000100B  ; Selects the source clock and mode
LD      (TC1CR), 00100100B  ; Starts TC1 external trigger, METT1 = 0
```

Example 2 :Generating an interrupt when the low-level pulse with 4 ms or more width is input to the TC1 pin (fc =16 MHz)

```
LDW     (TC1DRA), 01F4H     ; 4 ms ÷ 2^7/fc = 1F4H
DI                          ; IMF= "0"
SET     (EIRL). 5           ; Enables INTTC1 interrupt
EI                          ; IMF= "1"
LD      (TC1CR), 00000100B  ; Selects the source clock and mode
LD      (TC1CR), 01110100B  ; Starts TC1 external trigger, METT1 = 1
```



(a) Trigger start (METT1 = 0)



(b) Trigger start and stop (METT1 = 1)

Figure 8-3 External Trigger Timer Mode Timing Chart

8.3.3 Event Counter Mode

In the event counter mode, the up-counter counts up at the edge of the input pulse to the TC1 pin. Either the rising or falling edge of the input pulse is selected as the count up edge in TC1CR<TC1S>.

When a match between the up-counter and the TC1DRA value is detected, an INTTC1 interrupt is generated and the up-counter is cleared. After being cleared, the up-counter restarts counting at each edge of the input pulse to the TC1 pin. Since a match between the up-counter and the value set to TC1DRA is detected at the edge opposite to the selected edge, an INTTC1 interrupt request is generated after a match of the value at the edge opposite to the selected edge.

Two or more machine cycles are required for the low-or high-level pulse input to the TC1 pin.

Setting TC1CR<ACAP1> to “1” captures the up-counter value into TC1DRB with the auto capture function. Use the auto-capture function in the operative condition of TC1. A captured value may not be fixed if it's read after the execution of the timer stop or auto-capture disable. Read the capture value in a capture enabled condition. Since the up-counter value is captured into TC1DRB by the source clock of up-counter after setting TC1CR<ACAP1> to "1". Therefore, to read the captured value, wait at least one cycle of the internal source clock before reading TC1DRB for the first time.

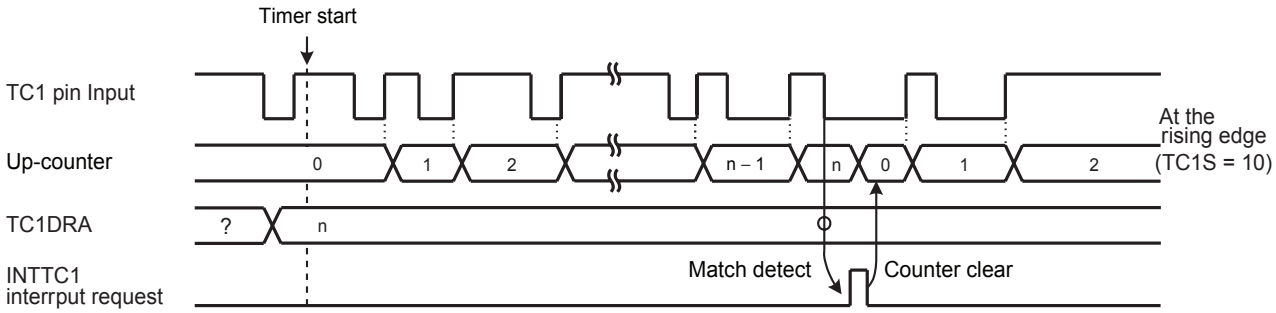


Figure 8-4 Event Counter Mode Timing Chart

Table 8-2 Input Pulse Width to TC1 Pin

	Minimum Pulse Width [s]	
	NORMAL1/2, IDLE1/2 Mode	SLOW1/2, SLEEP1/2 Mode
High-going	2^3/fc	2^3/fs
Low-going	2^3/fc	2^3/fs

8.3.4 Window Mode

In the window mode, the up-counter counts up at the rising edge of the pulse that is logical ANDed product of the input pulse to the TC1 pin (window pulse) and the internal source clock. Either the positive logic (count up during high-going pulse) or negative logic (count up during low-going pulse) can be selected.

When a match between the up-counter and the TC1DRA value is detected, an INTTC1 interrupt is generated and the up-counter is cleared.

Define the window pulse to the frequency which is sufficiently lower than the internal source clock programmed with TC1CR<TC1CK>.

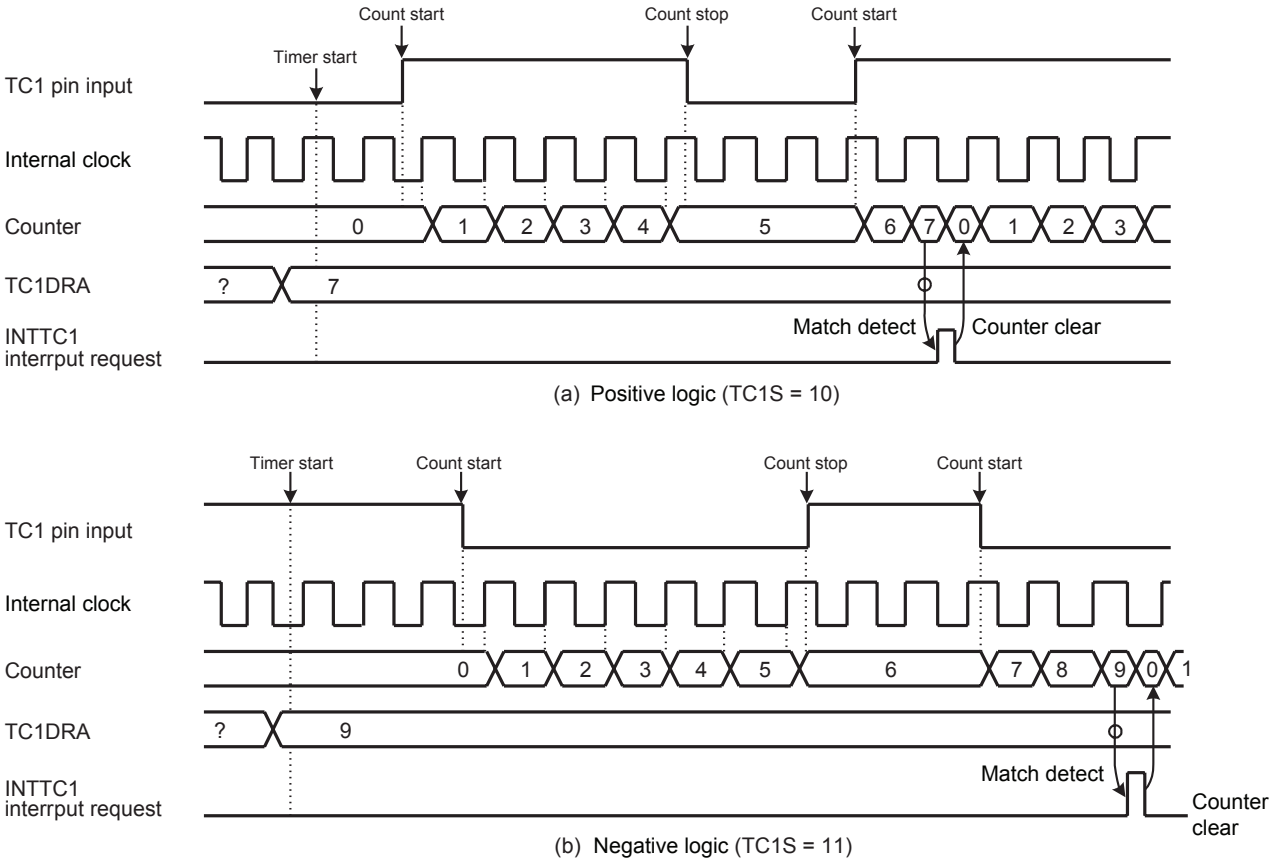


Figure 8-5 Window Mode Timing Chart

8.3.5 Pulse Width Measurement Mode

In the pulse width measurement mode, the up-counter starts counting by the input pulse triggering of the TC1 pin, and counts up at the edge of the internal clock. Either the rising or falling edge of the internal clock is selected as the trigger edge in TC1CR<TC1S>. Either the single- or double-edge capture is selected as the trigger edge in TC1CR<MCAP1>.

- When TC1CR<MCAP1> is set to “1” (single-edge capture)

  Either high- or low-level input pulse width can be measured. To measure the high-level input pulse width, set the rising edge to TC1CR<TC1S>. To measure the low-level input pulse width, set the falling edge to TC1CR<TC1S>.

  When detecting the edge opposite to the trigger edge used to start counting after the timer starts, the up-counter captures the up-counter value into TC1DRB and generates an INTTC1 interrupt request. The up-counter is cleared at this time, and then restarts counting when detecting the trigger edge used to start counting.

- When TC1CR<MCAP1> is set to “0” (double-edge capture)

  The cycle starting with either the high- or low-going input pulse can be measured. To measure the cycle starting with the high-going pulse, set the rising edge to TC1CR<TC1S>. To measure the cycle starting with the low-going pulse, set the falling edge to TC1CR<TC1S>.

  When detecting the edge opposite to the trigger edge used to start counting after the timer starts, the up-counter captures the up-counter value into TC1DRB and generates an INTTC1 interrupt request. The up-counter continues counting up, and captures the up-counter value into TC1DRB and generates an INTTC1 interrupt request when detecting the trigger edge used to start counting. The up-counter is cleared at this time, and then continues counting.

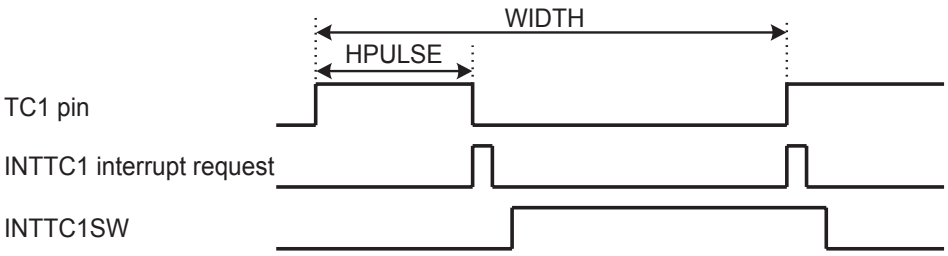
Note 1: The captured value must be read from TC1DRB until the next trigger edge is detected. If not read, the captured value becomes a don’t care. It is recommended to use a 16-bit access instruction to read the captured value from TC1DRB.

Note 2: For the single-edge capture, the counter after capturing the value stops at “1” until detecting the next edge. Therefore, the second captured value is “1” larger than the captured value immediately after counting starts.

Note 3: The first captured value after the timer starts may be read incorrectively, therefore, ignore the first captured value.

Example :Duty measurement (resolution fc/2^7 [Hz])

```
                CLR     (INTTC1SW). 0       ; INTTC1 service switch initial setting
                                              Address set to convert INTTC1SW at each INTTC1
                LD      (TC1CR), 00000110B  ; Sets the TC1 mode and source clock
                DI                          ; IMF= "0"
                SET     (EIRL). 5           ; Enables INTTC1
                EI                          ; IMF= "1"
                LD      (TC1CR), 00100110B  ; Starts TC1 with an external trigger at MCAP1 = 0
                :
PINTTC1:        CPL     (INTTC1SW). 0       ; INTTC1 interrupt, inverts and tests INTTC1 service switch
                JRS     F, SINTTC1
                LD      A, (TC1DRBL)        ; Reads TC1DRB (High-level pulse width)
                LD      W,(TC1DRBH)
                LD      (HPULSE), WA        ; Stores high-level pulse width in RAM
                RETI
SINTTC1:        LD      A, (TC1DRBL)        ; Reads TC1DRB (Cycle)
                LD      W,(TC1DRBH)
                LD      (WIDTH), WA         ; Stores cycle in RAM
                :
                RETI                        ; Duty calculation
                :
VINTTC1:        DW      PINTTC1             ; INTTC1 Interrupt vector
```



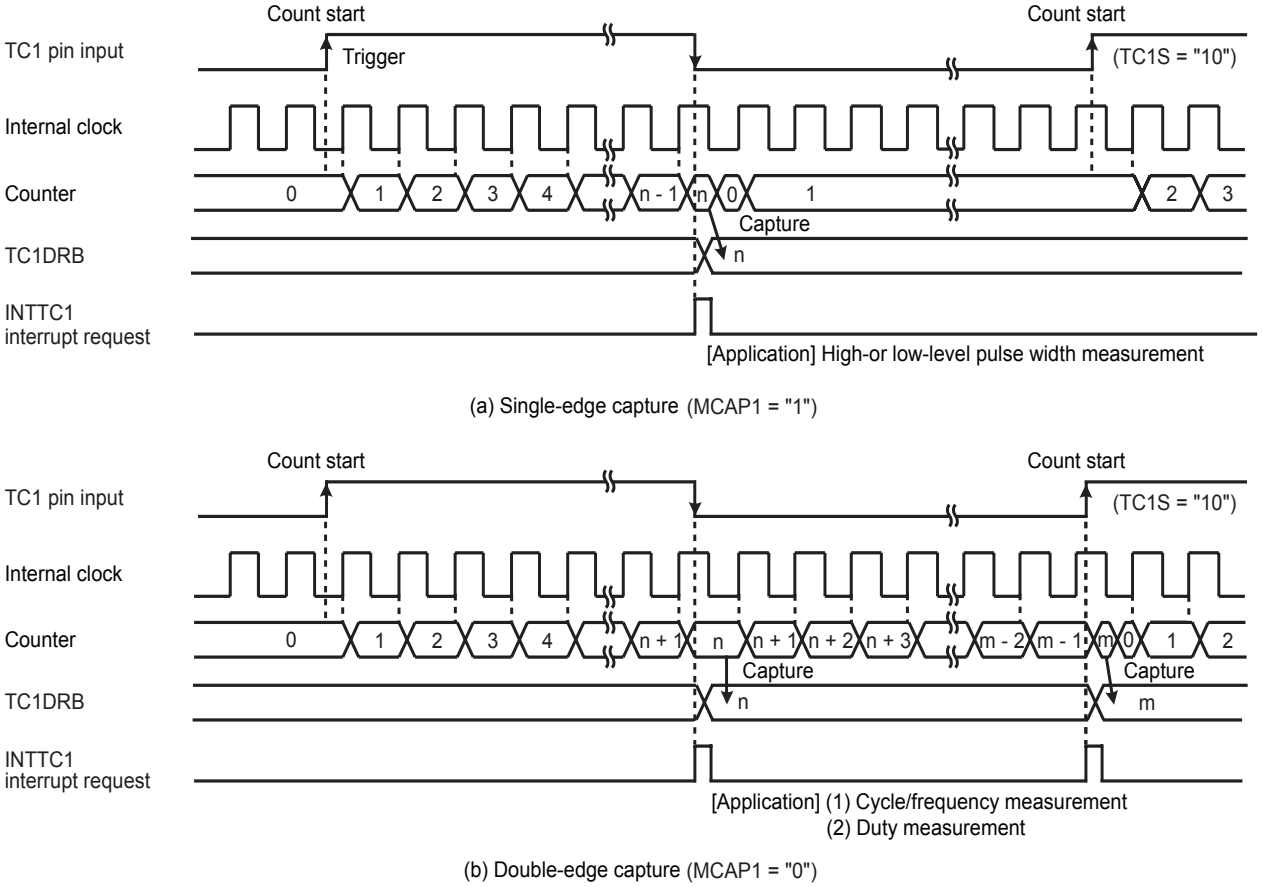


Figure 8-6 Pulse Width Measurement Mode

8.3.6 Programmable Pulse Generate (PPG) Output Mode

In the programmable pulse generation (PPG) mode, an arbitrary duty pulse is generated by counting performed in the internal clock. To start the timer, TC1CR<TC1S> specifies either the edge of the input pulse to the TC1 pin or the command start. TC1CR<MPPG1> specifies whether a duty pulse is produced continuously or not (one-shot pulse).

- When TC1CR<MPPG1> is set to "0" (Continuous pulse generation)

  When a match between the up-counter and the TC1DRB value is detected after the timer starts, the level of the $\overline{PPG}$ pin is inverted and an INTTC1 interrupt request is generated. The up-counter continues counting. When a match between the up-counter and the TC1DRA value is detected, the level of the $\overline{PPG}$ pin is inverted and an INTTC1 interrupt request is generated. The up-counter is cleared at this time, and then continues counting and pulse generation.

  When TC1S is cleared to "00" during PPG output, the $\overline{PPG}$ pin retains the level immediately before the counter stops.

- When TC1CR<MPPG1> is set to "1" (One-shot pulse generation)

  When a match between the up-counter and the TC1DRB value is detected after the timer starts, the level of the $\overline{PPG}$ pin is inverted and an INTTC1 interrupt request is generated. The up-counter continues counting. When a match between the up-counter and the TC1DRA value is detected, the level of the $\overline{PPG}$ pin is inverted and an INTTC1 interrupt request is generated. TC1CR<TC1S> is cleared to "00" automatically at this time, and the timer stops. The pulse generated by PPG retains the same level as that when the timer stops.

Since the output level of the $\overline{PPG}$ pin can be set with TC1CR<TFF1> when the timer starts, a positive or negative pulse can be generated. Since the inverted level of the timer F/F1 output level is output to the $\overline{PPG}$ pin, specify TC1CR<TFF1> to "0" to set the high level to the $\overline{PPG}$ pin, and "1" to set the low level to the $\overline{PPG}$ pin. Upon reset, the timer F/F1 is initialized to "0".

Note 1: To change TC1DRA or TC1DRB during a run of the timer, set a value sufficiently larger than the count value of the counter. Setting a value smaller than the count value of the counter during a run of the timer may generate a pulse different from that specified.

Note 2: Do not change TC1CR<TFF1> during a run of the timer. TC1CR<TFF1> can be set correctly only at initialization (after reset). When the timer stops during PPG, TC1CR<TFF1> can not be set correctly from this point onward if the PPG output has the level which is inverted of the level when the timer starts. (Setting TC1CR<TFF1> specifies the timer F/F1 to the level inverted of the programmed value.) Therefore, the timer F/F1 needs to be initialized to ensure an arbitrary level of the PPG output. To initialize the timer F/F1, change TC1CR<TC1M> to the timer mode (it is not required to start the timer mode), and then set the PPG mode. Set TC1CR<TFF1> at this time.

Note 3: In the PPG mode, the following relationship must be satisfied.
TC1DRA > TC1DRB

Note 4: Set TC1DRB after changing the mode of TC1M to the PPG mode.

Example :Generating a pulse which is high-going for 800 μs and low-going for 200 μs
(fc = 16 MHz)

```
                Setting port
LD              (TC1CR), 10000111B      ; Sets the PPG mode, selects the source clock
LDW             (TC1DRA), 007DH         ; Sets the cycle (1 ms ÷ 2^7/fc ms = 007DH)
LDW             (TC1DRB), 0019H         ; Sets the low-level pulse width (200 μs ÷ 2^7/fc = 0019H)
LD              (TC1CR), 10010111B      ; Starts the timer
```

Example :After stopping PPG, setting the PPG pin to a high-level to restart PPG
(fc = 16 MHz)

```
                Setting port
LD              (TC1CR), 10000111B      ; Sets the PPG mode, selects the source clock
LDW             (TC1DRA), 007DH         ; Sets the cycle (1 ms ÷ 2^7/fc μs = 007DH)
LDW             (TC1DRB), 0019H         ; Sets the low-level pulse width (200 μs ÷ 2^7/fc = 0019H)
LD              (TC1CR), 10010111B      ; Starts the timer
:               :
LD              (TC1CR), 10000111B      ; Stops the timer
LD              (TC1CR), 10000100B      ; Sets the timer mode
LD              (TC1CR), 00000111B      ; Sets the PPG mode, TFF1 = 0
LD              (TC1CR), 00010111B      ; Starts the timer
```

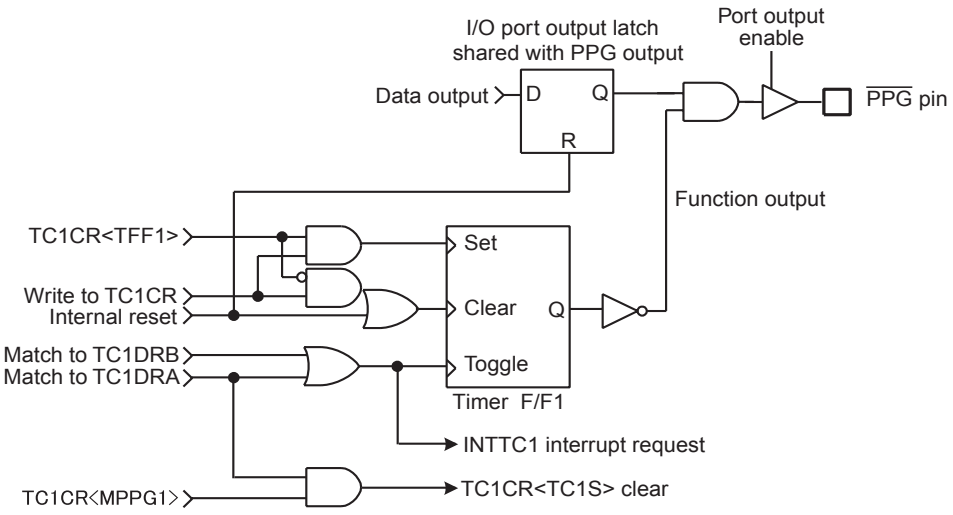


Figure 8-7 $\overline{\text{PPG}}$ Output

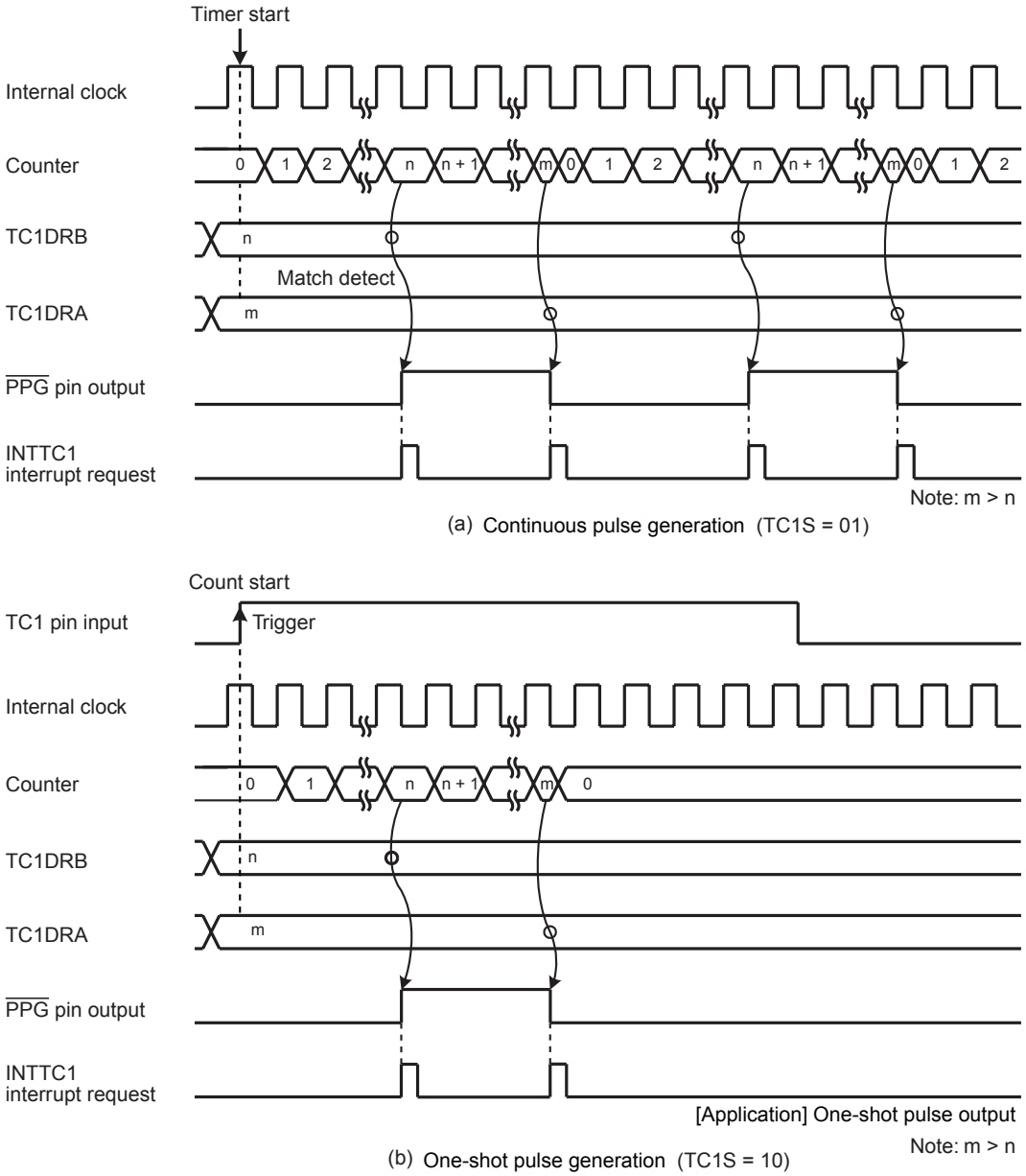
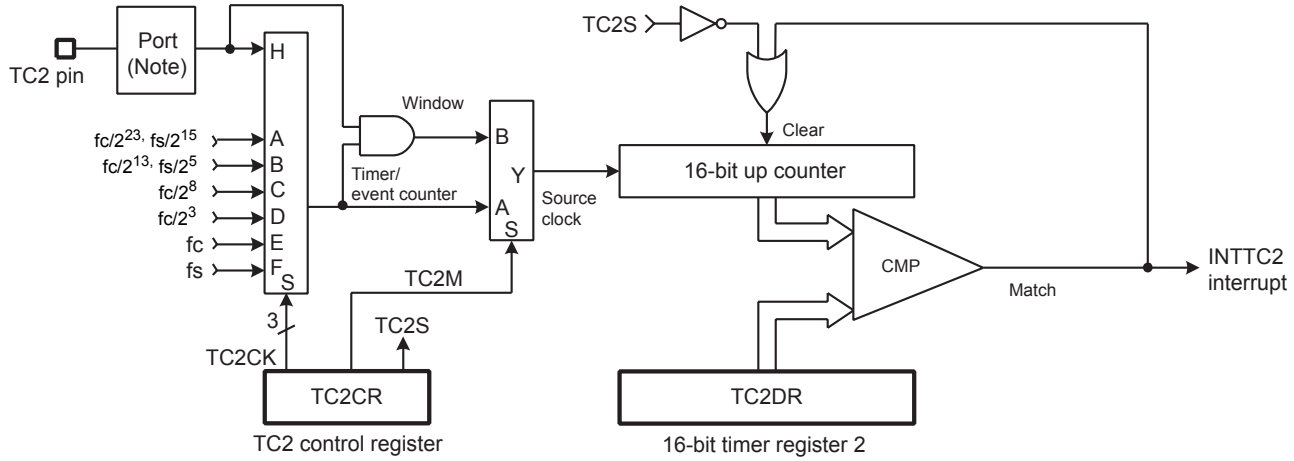


Figure 8-8 PPG Mode Timing Chart

T5CL8

9. 16-Bit Timer/Counter2 (TC2)

9.1 Configuration



Note: When control input/output is used, I/O port setting should be set correctly. For details, refer to the section "I/O ports".

Figure 9-1 Timer/Counter2 (TC2)

9.2 Control

The timer/counter 2 is controlled by a timer/counter 2 control register (TC2CR) and a 16-bit timer register 2 (TC2DR).

TC2DR (0025H, 0024H)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC2DRH (0025H)								TC2DRL (0024H)							
(Initial value: 1111 1111 1111 1111)								R/W							

TC2CR (0023H)

7	6	5	4	3	2	1	0
		TC2S	TC2CK				TC2M

(Initial value: **00 00*0)

TC2S	TC2 start control	0:Stop and counter clear 1:Start					R/W
TC2CK	TC2 source clock select Unit : [Hz]		NORMAL1/2, IDLE1/2 mode		Divider	SLOW1/2 mode	SLEEP1/2 mode	R/W
			DV7CK = 0	DV7CK = 1			
		000	$fc/2^{23}$	$fs/2^{15}$	DV21	$fs/2^{15}$	$fs/2^{15}$	
		001	$fc/2^{13}$	$fs/2^{5}$	DV11	$fs/2^{5}$	$fs/2^{5}$	
		010	$fc/2^{8}$	$fc/2^{8}$	DV6	–	–	
		011	$fc/2^{3}$	$fc/2^{3}$	DV1	–	–	
		100	–	–	–	fc (Note7)	–	
		101	fs	fs	–	–	–	
		110	Reserved					
		111	External clock (TC2 pin input)					
TC2M	TC2 operating mode select	0:Timer/event counter mode 1:Window mode					R/W

Note 1: fc: High-frequency clock [Hz], fs: Low-frequency clock [Hz], *: Don't care

Note 2: When writing to the Timer Register 2 (TC2DR), always write to the lower side (TC2DRL) and then the upper side (TC2DRH) in that order. Writing to only the lower side (TC2DRL) or the upper side (TC2DRH) has no effect.

Note 3: The timer register 2 (TC2DR) uses the value previously set in it for coincidence detection until data is written to the upper side (TC2DRH) after writing data to the lower side (TC2DRL).

Note 4: Set the mode and source clock when the TC2 stops (TC2S = 0).

Note 5: Values to be loaded to the timer register must satisfy the following condition.
TC2DR > 1 ($TC2DR_{15}$ to $TC2DR_{11}$ > 1 at warm up)

Note 6: If a read instruction is executed for TC2CR, read data of bit 7, 6 and 1 are unstable.

Note 7: The high-frequency clock (fc) canbe selected only when the time mode at SLOW2 mode is selected.

Note 8: On entering STOP mode, the TC2 start control (TC2S) is cleared to "0" automatically. So, the timer stops. Once the STOP mode has been released, to start using the timer counter, set TC2S again.

9.3 Function

The timer/counter 2 has three operating modes: timer, event counter and window modes.

And if fc or fs is selected as the source clock in timer mode, when switching the timer mode from SLOW1 to NORMAL2, the timer/counter2 can generate warm-up time until the oscillator is stable.

9.3.1 Timer mode

In this mode, the internal clock is used for counting up. The contents of TC2DR are compared with the contents of up counter. If a match is found, a timer/counter 2 interrupt (INTTC2) is generated, and the counter is cleared. Counting up is resumed after the counter is cleared.

When fc is selected for source clock at SLOW2 mode, lower 11-bits of TC2DR are ignored and generated a interrupt by matching upper 5-bits only. Though, in this situation, it is necessary to set TC2DRH only.

Table 9-1 Source Clock (Internal clock) for Timer/Counter2 (at fc = 16 MHz, DV7CK=0)

TC2CK	NORMAL1/2, IDLE1/2 mode				SLOW1/2 mode		SLEEP1/2 mode	
	DV7CK = 0		DV7CK = 1					
	Resolution	Maximum Time Setting	Resolution	Maximum Time Setting	Resolution	Maximum Time Setting	Resolution	Maximum Time Setting
000	524.29 [ms]	9.54 [h]	1 [s]	18.2 [h]	1 [s]	18.2 [h]	1 [s]	18.2 [h]
001	512.0 [ms]	33.55 [s]	0.98 [ms]	1.07 [min]	0.98 [ms]	1.07 [min]	0.98 [ms]	1.07 [min]
010	16.0 [ms]	1.05 [s]	16.0 [ms]	1.05 [s]	–	–	–	–
011	0.5 [ms]	32.77 [ms]	0.5 [ms]	32.77 [ms]	–	–	–	–
100	–	–	–	–	62.5 [ns]	–	–	–
101	30.52 [ms]	2 [s]	30.52 [ms]	2 [s]	–	–	–	–

Note: When fc is selected as the source clock in timer mode, it is used at warm-up for switching from SLOW1 mode to NORMAL2 mode.

Example :Sets the timer mode with source clock fc/2^3 [Hz] and generates an interrupt every 25 ms (at fc = 16 MHz)

```
LDW     (TC2DR), 061AH      ; Sets  TC2DR (25 ms ³ 2^8/fc = 061AH)
DI                          ; IMF= “0”
SET     (EIRE). 6           ; Enables INTTC2 interrupt
EI                          ; IMF= “1”
LD      (TC2CR), 00001000B  ; Source clock / mode select
LD      (TC2CR), 00101000B  ; Starts Timer
```

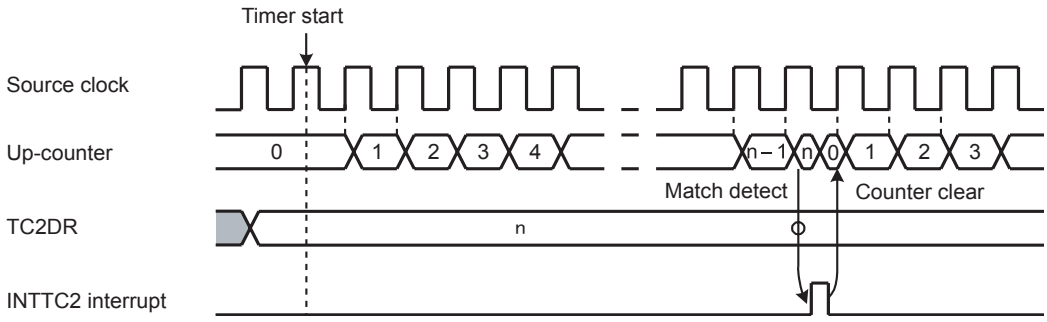


Figure 9-2 Timer Mode Timing Chart

9.3.2 Event counter mode

In this mode, events are counted on the rising edge of the TC2 pin input. The contents of TC2DR are compared with the contents of the up counter. If a match is found, an INTTC2 interrupt is generated, and the counter is cleared. Counting up is resumed every the rising edge of the TC2 pin input after the up counter is cleared.

Match detect is executed on the falling edge of the TC2 pin. Therefore, an INTTC2 interrupt is generated at the falling edge after the match of TC2DR and up counter.

The minimum input pulse width of TC2 pin is shown in Table 9-2. Two or more machine cycles are required for both the "H" and "L" levels of the pulse width.

Example :Sets the event counter mode and generates an INTTC2 interrupt 640 counts later.

```
LDW     (TC2DR), 640            ; Sets TC2DR
DI                              ; IMF= "0"
SET     (EIRE). 6               ;Enables  INTTC2 interrupt
EI                              ; IMF= "1"
LD      (TC2CR), 00011100B      ; TC2 source vclock / mode select
LD      (TC2CR), 00111100B      ; Starts TC2
```

Table 9-2 Timer/Counter 2 External Input Clock Pulse Width

	Minimum Input Pulse Width [s]	
	NORMAL1/2, IDLE1/2 mode	SLOW1/2, SLEEP1/2 mode
"H" width	2^3/fc	2^3/fs
"L" width	2^3/fc	2^3/fs

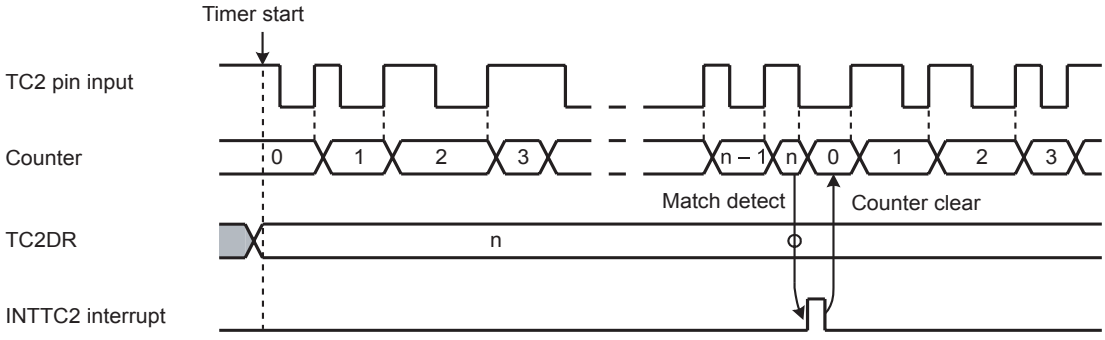


Figure 9-3 Event Counter Mode Timing Chart

9.3.3 Window mode

In this mode, counting up performed on the rising edge of an internal clock during TC2 external pin input (Window pulse) is "H" level. The contents of TC2DR are compared with the contents of up counter. If a match found, an INTTC2 interrupt is generated, and the up-counter is cleared.

The maximum applied frequency (TC2 input) must be considerably slower than the selected internal clock by the TC2CR<TC2CK>.

Note: It is not available window mode in the SLOW/SLEEP mode. Therefore, at the window mode in NORMAL mode, the timer should be halted by setting TC2CR<TC2S> to "0" before the SLOW/SLEEP mode is entered.

Example :Generates an interrupt, inputting “H” level pulse width of 120 ms or more. (at fc = 16 MHz, TBTCR<DV7CK> = “0”)

```
LDW     (TC2DR), 00EAH          ; Sets TC2DR (120 ms ³ 213/fc = 00EAH)
DI                              ; IMF= “0”
SET     (EIRE). 6               ; Enables  INTTC2 interrupt
EI                              ; IMF= “1”
LD      (TC2CR), 00000101B      ; TC2sorce clock / mode select
LD      (TC2CR), 00100101B      ; Starts TC2
```

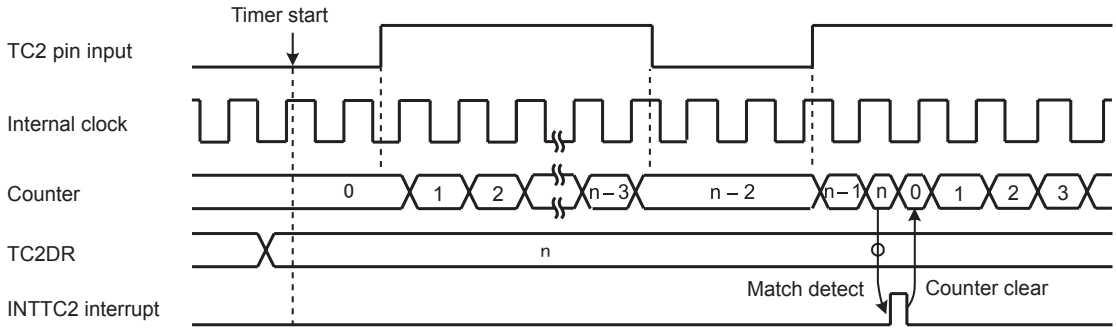


Figure 9-4 Window Mode Timing Chart

10. 8-Bit TimerCounter (TC3, TC4)

10.1 Configuration

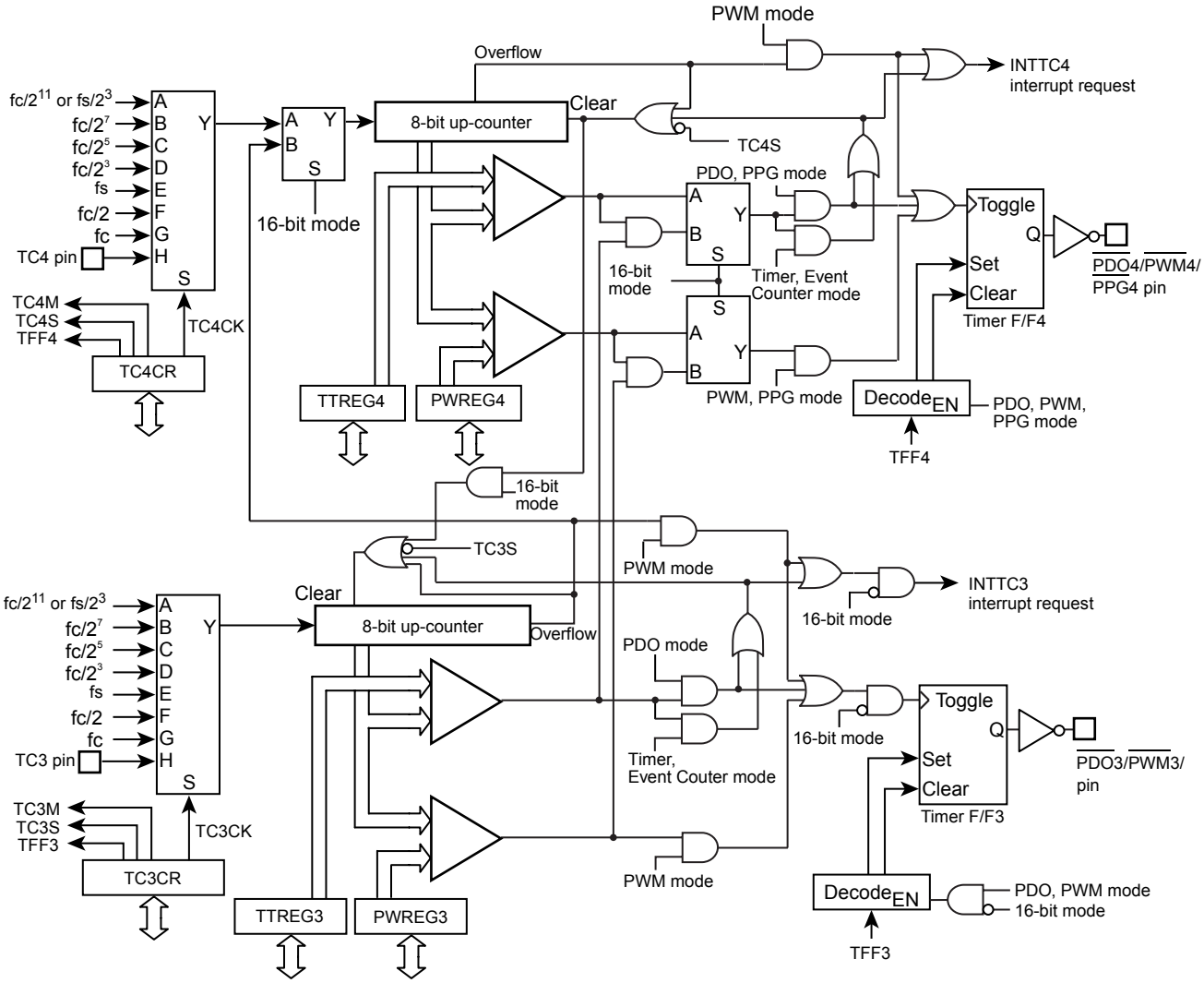


Figure 10-1 8-Bit TimerCounter 3, 4

10.2 TimerCounter Control

The TimerCounter 3 is controlled by the TimerCounter 3 control register (TC3CR) and two 8-bit timer registers (TTREG3, PWREG3).

TimerCounter 3 Timer Register

	7	6	5	4	3	2	1	0	
TTREG3 (0014H) R/W									(Initial value: 1111 1111)
PWREG3 (0018H) R/W									(Initial value: 1111 1111)

Note 1: Do not change the timer register (TTREG3) setting while the timer is running.

Note 2: Do not change the timer register (PWREG3) setting in the operating mode except the 8-bit and 16-bit PWM modes while the timer is running.

TimerCounter 3 Control Register

TC3CR (0027H)	7	6	5	4	3	2	1	0	
	TFF3	TC3CK			TC3S	TC3M			(Initial value: 0000 0000)

TFF3	Time F/F3 control	0: Clear 1: Set			R/W
TC3CK	Operating clock selection [Hz]		NORMAL1/2, IDLE1/2 mode	SLOW1/2 SLEEP1/2 mode	R/W
			DV7CK = 0	DV7CK = 1	
		000	$fc/2^{11}$	$fs/2^3$	$fs/2^3$
		001	$fc/2^7$	$fc/2^7$	–
		010	$fc/2^5$	$fc/2^5$	–
		011	$fc/2^3$	$fc/2^3$	–
		100	fs	fs	fs
		101	fc/2	fc/2	–
		110	fc	fc	fc (Note 8)
		111	TC3 pin input		
TC3S	TC3 start control	0: Operation stop and counter clear 1: Operation start			R/W
TC3M	TC3M operating mode select	000: 8-bit timer/event counter mode 001: 8-bit programmable divider output (PDO) mode 010: 8-bit pulse width modulation (PWM) output mode 011: 16-bit mode (Each mode is selectable with TC4M.) 1**: Reserved			R/W

Note 1: fc: High-frequency clock [Hz] fs: Low-frequency clock[Hz]

Note 2: Do not change the TC3M, TC3CK and TFF3 settings while the timer is running.

Note 3: To stop the timer operation (TC3S= 1 → 0), do not change the TC3M, TC3CK and TFF3 settings. To start the timer operation (TC3S= 0 → 1), TC3M, TC3CK and TFF3 can be programmed.

Note 4: To use the TimerCounter in the 16-bit mode, set the operating mode by programming TC4CR<TC4M>, where TC3M must be fixed to 011.

Note 5: To use the TimerCounter in the 16-bit mode, select the source clock by programming TC3CK. Set the timer start control and timer F/F control by programming TC4CR<TC4S> and TC4CR<TFF4>, respectively.

Note 6: The operating clock settings are limited depending on the timer operating mode. For the detailed descriptions, see Table 10-1 and Table 10-2.

Note 7: The timer register settings are limited depending on the timer operating mode. For the detailed descriptions, see Table 10-3.

Note 8: The operating clock fc in the SLOW or SLEEP mode can be used only as the high-frequency warm-up mode.

The TimerCounter 4 is controlled by the TimerCounter 4 control register (TC4CR) and two 8-bit timer registers (TTREG4 and PWREG4).

TimerCounter 4 Timer Register

	7	6	5	4	3	2	1	0	
TTREG4 (0015H) R/W									(Initial value: 1111 1111)
PWREG4 (0019H) R/W									(Initial value: 1111 1111)

Note 1: Do not change the timer register (TTREG4) setting while the timer is running.

Note 2: Do not change the timer register (PWREG4) setting in the operating mode except the 8-bit and 16-bit PWM modes while the timer is running.

TimerCounter 4 Control Register

TC4CR (0028H)	7	6	5	4	3	2	1	0	
	TFF4	TC4CK			TC4S	TC4M			(Initial value: 0000 0000)

TFF4	Timer F/F4 control	0: Clear 1: Set			R/W
TC4CK	Operating clock selection [Hz]		NORMAL1/2, IDLE1/2 mode		SLOW1/2 SLEEP1/2 mode
			DV7CK = 0	DV7CK = 1	
		000	$fc/2^{11}$	$fs/2^3$	$fs/2^3$
		001	$fc/2^7$	$fc/2^7$	–
		010	$fc/2^5$	$fc/2^5$	–
		011	$fc/2^3$	$fc/2^3$	–
		100	fs	fs	fs
		101	fc/2	fc/2	–
		110	fc	fc	–
		111	TC4 pin input		
					R/W
TC4S	TC4 start control	0: Operation stop and counter clear 1: Operation start			R/W
TC4M	TC4M operating mode select	000: 8-bit timer/event counter mode 001: 8-bit programmable divider output (PDO) mode 010: 8-bit pulse width modulation (PWM) output mode 011: Reserved 100: 16-bit timer/event counter mode 101: Warm-up counter mode 110: 16-bit pulse width modulation (PWM) output mode 111: 16-bit PPG mode			R/W

Note 1: fc: High-frequency clock [Hz] fs: Low-frequency clock [Hz]

Note 2: Do not change the TC4M, TC4CK and TFF4 settings while the timer is running.

Note 3: To stop the timer operation (TC4S= 1 → 0), do not change the TC4M, TC4CK and TFF4 settings.
To start the timer operation (TC4S= 0 → 1), TC4M, TC4CK and TFF4 can be programmed.

Note 4: When TC4M= 1** (upper byte in the 16-bit mode), the source clock becomes the TC3 overflow signal regardless of the TC4CK setting.

Note 5: To use the TimerCounter in the 16-bit mode, select the operating mode by programming TC4M, where TC3CR<TC3M> must be set to 011.

Note 6: To the TimerCounter in the 16-bit mode, select the source clock by programming TC3CR<TC3CK>. Set the timer start control and timer F/F control by programming TC4S and TFF4, respectively.

Note 7: The operating clock settings are limited depending on the timer operating mode. For the detailed descriptions, see Table 10-1 and Table 10-2.

Note 8: The timer register settings are limited depending on the timer operating mode. For the detailed descriptions, see Table 10-3.

Table 10-1 Operating Mode and Selectable Source Clock (NORMAL1/2 and IDLE1/2 Modes)

Operating mode	$fc/2^{11}$ or $fs/2^3$	$fc/2^7$	$fc/2^5$	$fc/2^3$	fs	fc/2	fc	TC3 pin input	TC4 pin input
8-bit timer	O	O	O	O	–	–	–	–	–
8-bit event counter	–	–	–	–	–	–	–	O	O
8-bit PDO	O	O	O	O	–	–	–	–	–
8-bit PWM	O	O	O	O	O	O	O	–	–
16-bit timer	O	O	O	O	–	–	–	–	–
16-bit event counter	–	–	–	–	–	–	–	O	–
Warm-up counter	–	–	–	–	O	–	–	–	–
16-bit PWM	O	O	O	O	O	O	O	O	–
16-bit PPG	O	O	O	O	–	–	–	O	–

Note 1: For 16-bit operations (16-bit timer/event counter, warm-up counter, 16-bit PWM and 16-bit PPG), set its source clock on lower bit (TC3CK).

Note 2: O : Available source clock

Table 10-2 Operating Mode and Selectable Source Clock (SLOW1/2 and SLEEP1/2 Modes)

Operating mode	$fc/2^{11}$ or $fs/2^3$	$fc/2^7$	$fc/2^5$	$fc/2^3$	fs	fc/2	fc	TC3 pin input	TC4 pin input
8-bit timer	O	–	–	–	–	–	–	–	–
8-bit event counter	–	–	–	–	–	–	–	O	O
8-bit PDO	O	–	–	–	–	–	–	–	–
8-bit PWM	O	–	–	–	O	–	–	–	–
16-bit timer	O	–	–	–	–	–	–	–	–
16-bit event counter	–	–	–	–	–	–	–	O	–
Warm-up counter	–	–	–	–	–	–	O	–	–
16-bit PWM	O	–	–	–	O	–	–	O	–
16-bit PPG	O	–	–	–	–	–	–	O	–

Note1: For 16-bit operations (16-bit timer/event counter, warm-up counter, 16-bit PWM and 16-bit PPG), set its source clock on lower bit (TC3CK).

Note2: O : Available source clock

Table 10-3 Constraints on Register Values Being Compared

Operating mode	Register Value
8-bit timer/event counter	1≤ (TTREGn) ≤255
8-bit PDO	1≤ (TTREGn) ≤255
8-bit PWM	2≤ (PWREGn) ≤254
16-bit timer/event counter	1≤ (TTREG4, 3) ≤65535
Warm-up counter	256≤ (TTREG4, 3) ≤65535
16-bit PWM	2≤ (PWREG4, 3) ≤65534
16-bit PPG	1≤ (PWREG4, 3) < (TTREG4, 3) ≤65535 and (PWREG4, 3) + 1 < (TTREG4, 3)

Note: n = 3 to 4

10.3 Function

The TimerCounter 3 and 4 have the 8-bit timer, 8-bit event counter, 8-bit programmable divider output (PDO), 8-bit pulse width modulation (PWM) output modes. The TimerCounter 3 and 4 (TC3, 4) are cascadable to form a 16-bit timer. The 16-bit timer has the operating modes such as the 16-bit timer, 16-bit event counter, warm-up counter, 16-bit pulse width modulation (PWM) output and 16-bit programmable pulse generation (PPG) modes.

10.3.1 8-Bit Timer Mode (TC3 and 4)

In the timer mode, the up-counter counts up using the internal clock. When a match between the up-counter and the timer register j (TTREGj) value is detected, an INTTCj interrupt is generated and the up-counter is cleared. After being cleared, the up-counter restarts counting.

Note 1: In the timer mode, fix TCjCR<TFFj> to 0. If not fixed, the $\overline{\text{PDOj}}$, $\overline{\text{PWMj}}$ and $\overline{\text{PPGj}}$ pins may output pulses.

Note 2: In the timer mode, do not change the TTREGj setting while the timer is running. Since TTREGj is not in the shift register configuration in the timer mode, the new value programmed in TTREGj is in effect immediately after the programming. Therefore, if TTREGi is changed while the timer is running, an expected operation may not be obtained.

Note 3: j = 3, 4

Table 10-4 Source Clock for TimerCounter 3, 4 (Internal Clock)

Source Clock			Resolution		Maximum Time Setting	
NORMAL1/2, IDLE1/2 mode		SLOW1/2, SLEEP1/2 mode	fc = 16 MHz	fs = 32.768 kHz	fc = 16 MHz	fs = 32.768 kHz
DV7CK = 0	DV7CK = 1					
$fc/2^{11}$ [Hz]	$fs/2^3$ [Hz]	$fs/2^3$ [Hz]	128 μs	244.14 μs	32.6 ms	62.3 ms
$fc/2^7$	$fc/2^7$	–	8 μs	–	2.0 ms	–
$fc/2^5$	$fc/2^5$	–	2 μs	–	510 μs	–
$fc/2^3$	$fc/2^3$	–	500 ns	–	127.5 μs	–

Example :Setting the timer mode with source clock $fc/2^7$ Hz and generating an interrupt 80 μs later (TimerCounter4, fc = 16.0 MHz)

```
LD      (TTREG4), 0AH          : Sets the timer register (80 μs÷2^7/fc = 0AH).
DI
SET     (EIRH). 1              : Enables INTTC4 interrupt.
EI
LD      (TC4CR), 00010000B     : Sets the operating clock to fc/2^7, and 8-bit timer mode.
LD      (TC4CR), 00011000B     : Starts TC4.
```

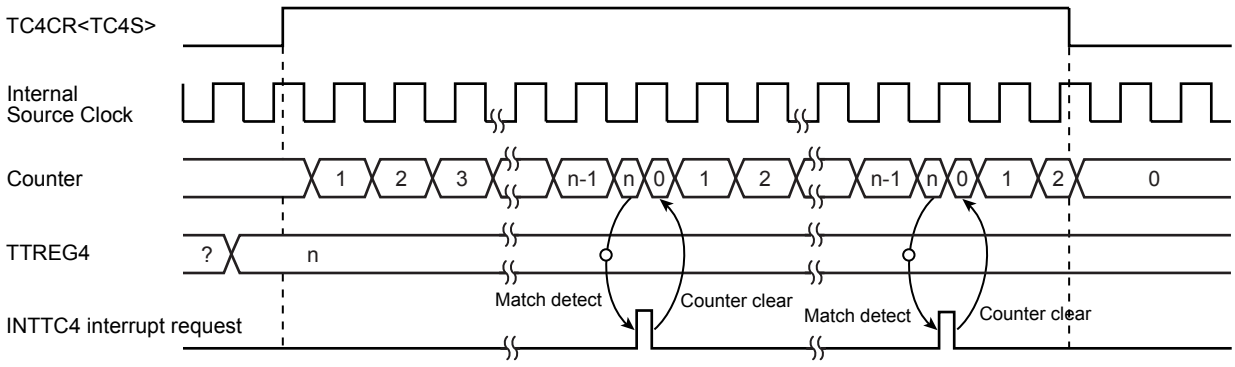


Figure 10-2 8-Bit Timer Mode Timing Chart (TC4)

10.3.2 8-Bit Event Counter Mode (TC3, 4)

In the 8-bit event counter mode, the up-counter counts up at the falling edge of the input pulse to the TCj pin. When a match between the up-counter and the TTREGj value is detected, an INTTCj interrupt is generated and the up-counter is cleared. After being cleared, the up-counter restarts counting at the falling edge of the input pulse to the TCj pin. Two machine cycles are required for the low- or high-level pulse input to the TCj pin. Therefore, a maximum frequency to be supplied is $fc/2^4$ Hz in the NORMAL1/2 or IDLE1/2 mode, and $fs/2^4$ Hz in the SLOW1/2 or SLEEP1/2 mode.

Note 1: In the event counter mode, fix TCjCR<TFFj> to 0. If not fixed, the $\overline{\text{PDOj, PWMj}}$ and $\overline{\text{PPGj}}$ pins may output pulses.

Note 2: In the event counter mode, do not change the TTREGj setting while the timer is running. Since TTREGj is not in the shift register configuration in the event counter mode, the new value programmed in TTREGj is in effect immediately after the programming. Therefore, if TTREGi is changed while the timer is running, an expected operation may not be obtained.

Note 3: j = 3, 4

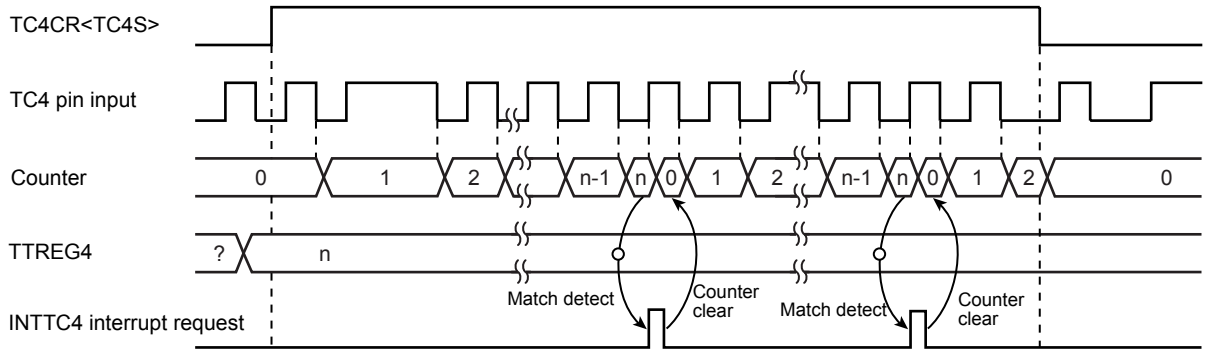


Figure 10-3 8-Bit Event Counter Mode Timing Chart (TC4)

10.3.3 8-Bit Programmable Divider Output (PDO) Mode (TC3, 4)

This mode is used to generate a pulse with a 50% duty cycle from the $\overline{\text{PDOj}}$ pin.

In the PDO mode, the up-counter counts up using the internal clock. When a match between the up-counter and the TTREGj value is detected, the logic level output from the $\overline{\text{PDOj}}$ pin is switched to the opposite state and the up-counter is cleared. The INTTCj interrupt request is generated at the time. The logic state opposite to the timer F/Fj logic level is output from the $\overline{\text{PDOj}}$ pin. An arbitrary value can be set to the timer F/Fj by TCjCR<TFFj>. Upon reset, the timer F/Fj value is initialized to 0.

To use the programmable divider output, set the output latch of the I/O port to 1.

Example :Generating 1024 Hz pulse using TC4 (fc = 16.0 MHz)

```
                Setting port
LD      (TTREG4),  3DH          : 1/1024÷2^7/fc÷2 = 3DH
LD      (TC4CR),   00010001B    : Sets the operating clock to fc/2^7, and 8-bit PDO mode.
LD      (TC4CR),  00011001B     : Starts TC4.
```

Note 1: In the programmable divider output mode, do not change the TTREGj setting while the timer is running. Since TTREGj is not in the shift register configuration in the programmable divider output mode, the new value programmed in TTREGj is in effect immediately after programming. Therefore, if TTREGi is changed while the timer is running, an expected operation may not be obtained.

Note 2: When the timer is stopped during PDO output, the $\overline{\text{PDOj}}$ pin holds the output status when the timer is stopped. To change the output status, program TCjCR<TFFj> after the timer is stopped. Do not change the TCjCR<TFFj> setting upon stopping of the timer.
Example: Fixing the $\overline{\text{PDOj}}$ pin to the high level when the TimerCounter is stopped
CLR (TCjCR).3: Stops the timer.
CLR (TCjCR).7: Sets the $\overline{\text{PDOj}}$ pin to the high level.

Note 3: j = 3, 4

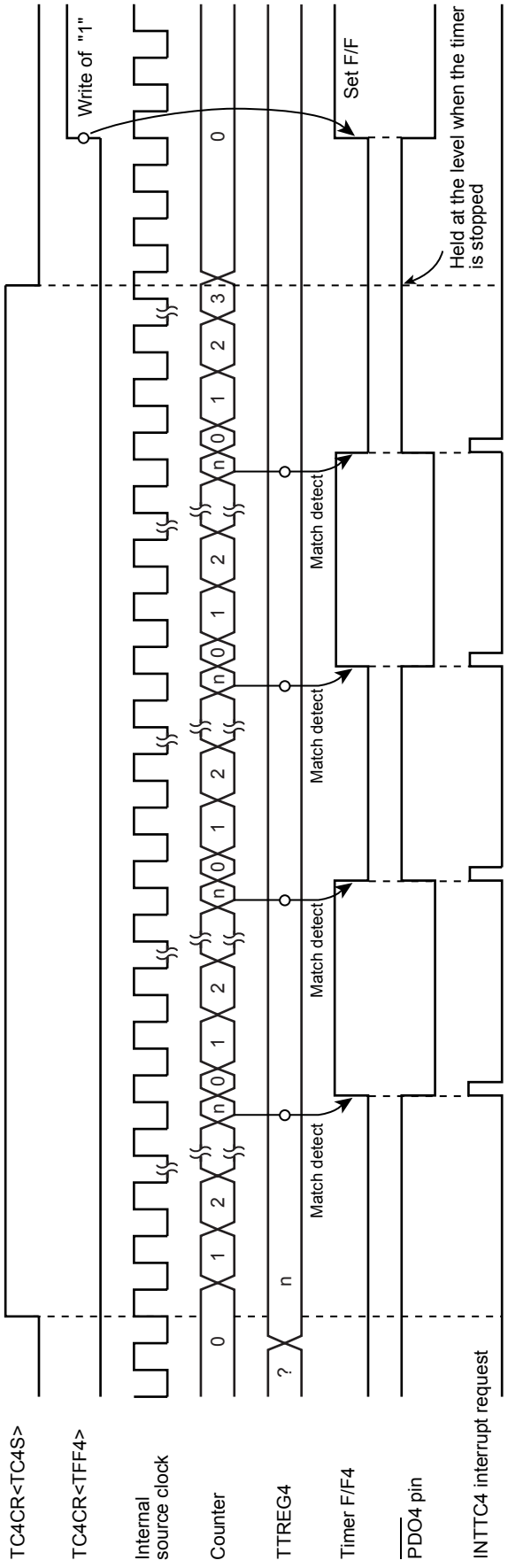


Figure 10-4 8-Bit PDO Mode Timing Chart (TC4)

10.3.4 8-Bit Pulse Width Modulation (PWM) Output Mode (TC3, 4)

This mode is used to generate a pulse-width modulated (PWM) signals with up to 8 bits of resolution. The up-counter counts up using the internal clock.

When a match between the up-counter and the PWREGj value is detected, the logic level output from the timer F/Fj is switched to the opposite state. The counter continues counting. The logic level output from the timer F/Fj is switched to the opposite state again by the up-counter overflow, and the counter is cleared. The INTTCj interrupt request is generated at this time.

Since the initial value can be set to the timer F/Fj by TCjCR<TFFj>, positive and negative pulses can be generated. Upon reset, the timer F/Fj is cleared to 0.

(The logic level output from the $\overline{\text{PWMj}}$ pin is the opposite to the timer F/Fj logic level.)

Since PWREGj in the PWM mode is serially connected to the shift register, the value set to PWREGj can be changed while the timer is running. The value set to PWREGj during a run of the timer is shifted by the INTTCj interrupt request and loaded into PWREGj. While the timer is stopped, the value is shifted immediately after the programming of PWREGj. If executing the read instruction to PWREGj during PWM output, the value in the shift register is read, but not the value set in PWREGj. Therefore, after writing to PWREGj, the reading data of PWREGj is previous value until INTTCj is generated.

For the pin used for PWM output, the output latch of the I/O port must be set to 1.

Note 1: In the PWM mode, program the timer register PWREGj immediately after the INTTCj interrupt request is generated (normally in the INTTCj interrupt service routine.) If the programming of PWREGj and the interrupt request occur at the same time, an unstable value is shifted, that may result in generation of the pulse different from the programmed value until the next INTTCj interrupt request is generated.

Note 2: When the timer is stopped during PWM output, the $\overline{\text{PWMj}}$ pin holds the output status when the timer is stopped. To change the output status, program TCjCR<TFFj> after the timer is stopped. Do not change the TCjCR<TFFj> upon stopping of the timer.
Example: Fixing the $\overline{\text{PWMj}}$ pin to the high level when the TimerCounter is stopped
CLR (TCjCR).3: Stops the timer.
CLR (TCjCR).7: Sets the $\overline{\text{PWMj}}$ pin to the high level.

Note 3: To enter the STOP mode during PWM output, stop the timer and then enter the STOP mode. If the STOP mode is entered without stopping the timer when fc, fc/2 or fs is selected as the source clock, a pulse is output from the $\overline{\text{PWMj}}$ pin during the warm-up period time after exiting the STOP mode.

Note 4: j = 3, 4

Table 10-5 PWM Output Mode

Source Clock			Resolution		Repeated Cycle	
NORMAL1/2, IDLE1/2 mode		SLOW1/2, SLEEP1/2 mode	fc = 16 MHz	fs = 32.768 kHz	fc = 16 MHz	fs = 32.768 kHz
DV7CK = 0	DV7CK = 1					
$fc/2^{11}$ [Hz]	$fs/2^3$ [Hz]	$fs/2^3$ [Hz]	128 μs	244.14 μs	32.8 ms	62.5 ms
$fc/2^7$	$fc/2^7$	–	8 μs	–	2.05 ms	–
$fc/2^5$	$fc/2^5$	–	2 μs	–	512 μs	–
$fc/2^3$	$fc/2^3$	–	500 ns	–	128 μs	–
fs	fs	fs	30.5 μs	30.5 μs	7.81 ms	7.81 ms
fc/2	fc/2	–	125 ns	–	32 μs	–
fc	fc	–	62.5 ns	–	16 μs	–

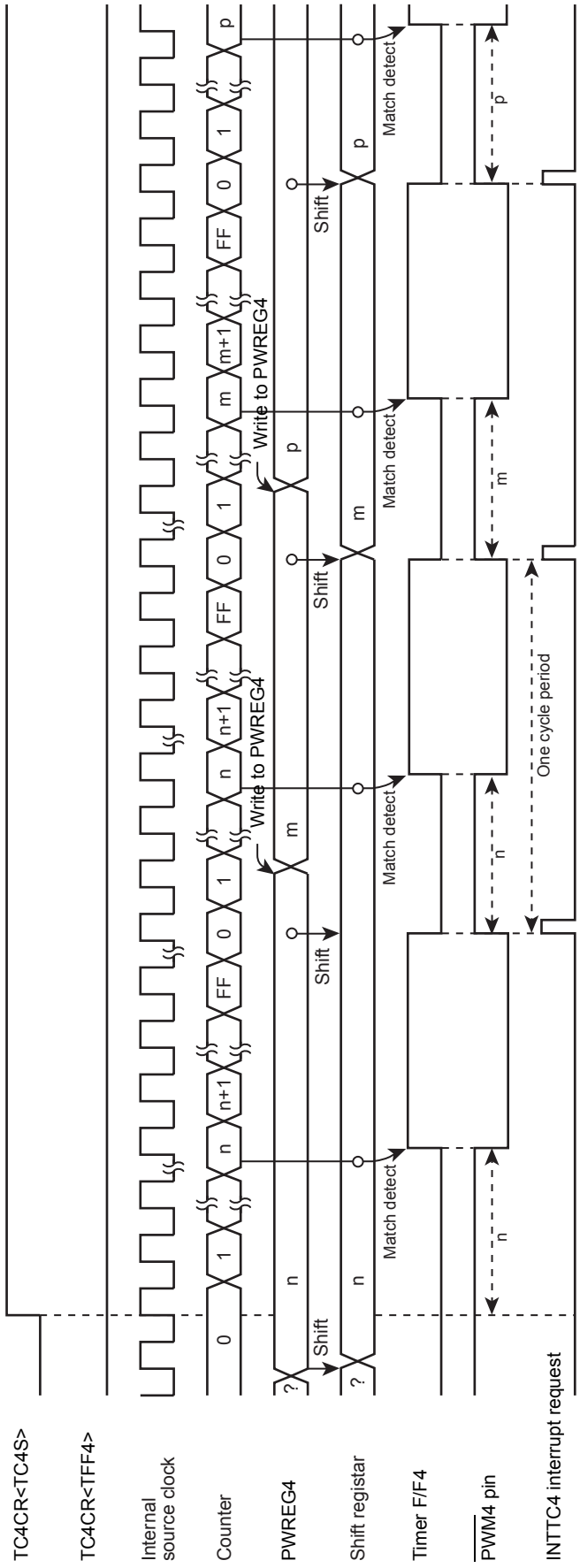


Figure 10-5 8-Bit PWM Mode Timing Chart (TC4)

10.3.5 16-Bit Timer Mode (TC3 and 4)

In the timer mode, the up-counter counts up using the internal clock. The TimerCounter 3 and 4 are cascadable to form a 16-bit timer.

When a match between the up-counter and the timer register (TTREG3, TTREG4) value is detected after the timer is started by setting TC4CR<TC4S> to 1, an INTTC4 interrupt is generated and the up-counter is cleared. After being cleared, the up-counter continues counting. Program the lower byte and upper byte in this order in the timer register. (Programming only the upper or lower byte should not be attempted.)

Note 1: In the timer mode, fix TCjCR<TFFj> to 0. If not fixed, the $\overline{PDOj}$, $\overline{PWMj}$, and $\overline{PPGj}$ pins may output a pulse.

Note 2: In the timer mode, do not change the TTREGj setting while the timer is running. Since TTREGj is not in the shift register configuration in the timer mode, the new value programmed in TTREGj is in effect immediately after programming of TTREGj. Therefore, if TTREGj is changed while the timer is running, an expected operation may not be obtained.

Note 3: j = 3, 4

Table 10-6 Source Clock for 16-Bit Timer Mode

Source Clock			Resolution		Maximum Time Setting	
NORMAL1/2, IDLE1/2 mode		SLOW1/2, SLEEP1/2 mode	fc = 16 MHz	fs = 32.768 kHz	fc = 16 MHz	fs = 32.768 kHz
DV7CK = 0	DV7CK = 1					
$fc/2^{11}$	$fs/2^3$	$fs/2^3$	128 μs	244.14 μs	8.39 s	16 s
$fc/2^7$	$fc/2^7$	–	8 μs	–	524.3 ms	–
$fc/2^5$	$fc/2^5$	–	2 μs	–	131.1 ms	–
$fc/2^3$	$fc/2^3$	–	500 ns	–	32.8 ms	–

Example :Setting the timer mode with source clock $fc/2^7$ Hz, and generating an interrupt 300 ms later (fc = 16.0 MHz)

```
LDW     (TTREG3), 927CH     : Sets the timer register (300 ms÷2^7/fc = 927CH).
DI
SET     (EIRH). 1           : Enables INTTC4 interrupt.
EI
LD      (TC3CR), 13H        :Sets the operating clock to fc/2^7, and 16-bit timer mode
                             (lower byte).
LD      (TC4CR), 04H        : Sets the 16-bit timer mode (upper byte).
LD      (TC4CR), 0CH        : Starts the timer.
```

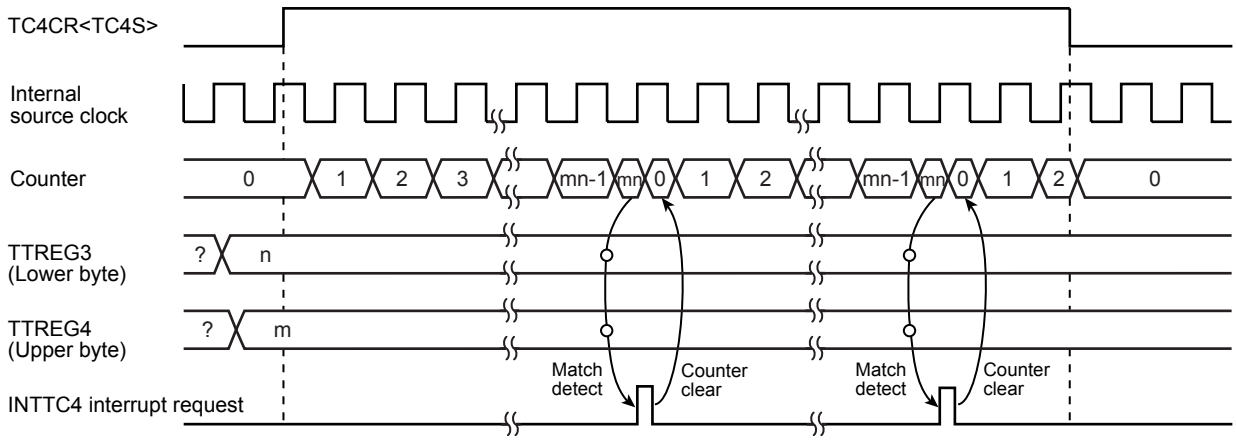


Figure 10-6 16-Bit Timer Mode Timing Chart (TC3 and TC4)

10.3.6 16-Bit Event Counter Mode (TC3 and 4)

In the event counter mode, the up-counter counts up at the falling edge to the TC3 pin. The TimerCounter 3 and 4 are cascadable to form a 16-bit event counter.

When a match between the up-counter and the timer register (TTREG3, TTREG4) value is detected after the timer is started by setting TC4CR<TC4S> to 1, an INTTC4 interrupt is generated and the up-counter is cleared.

After being cleared, the up-counter restarts counting at the falling edge of the input pulse to the TC3 pin. Two machine cycles are required for the low- or high-level pulse input to the TC3 pin.

Therefore, a maximum frequency to be supplied is $fc/2^4$ Hz in the NORMAL1/2 or IDLE1/2 mode, and $fs/2^4$ in the SLOW1/2 or SLEEP1/2 mode. Program the lower byte (TTREG3), and upper byte (TTREG4) in this order in the timer register. (Programming only the upper or lower byte should not be attempted.)

Note 1: In the event counter mode, fix TCjCR<TFFj> to 0. If not fixed, the $\overline{\text{PDOj}}$, $\overline{\text{PWMj}}$ and $\overline{\text{PPGj}}$ pins may output pulses.
Note 2: In the event counter mode, do not change the TTREGj setting while the timer is running. Since TTREGj is not in the shift register configuration in the event counter mode, the new value programmed in TTREGj is in effect immediately after the programming. Therefore, if TTREGj is changed while the timer is running, an expected operation may not be obtained.
Note 3: j = 3, 4

10.3.7 16-Bit Pulse Width Modulation (PWM) Output Mode (TC3 and 4)

This mode is used to generate a pulse-width modulated (PWM) signals with up to 16 bits of resolution. The TimerCounter 3 and 4 are cascadable to form the 16-bit PWM signal generator.

The counter counts up using the internal clock or external clock.

When a match between the up-counter and the timer register (PWREG3, PWREG4) value is detected, the logic level output from the timer F/F4 is switched to the opposite state. The counter continues counting. The logic level output from the timer F/F4 is switched to the opposite state again by the counter overflow, and the counter is cleared. The INTTC4 interrupt is generated at this time.

Two machine cycles are required for the high- or low-level pulse input to the TC3 pin. Therefore, a maximum frequency to be supplied is $fc/2^4$ Hz in the NORMAL1/2 or IDLE1/2 mode, and $fs/2^4$ to in the SLOW1/2 or SLEEP1/2 mode.

Since the initial value can be set to the timer F/F4 by TC4CR<TFF4>, positive and negative pulses can be generated. Upon reset, the timer F/F4 is cleared to 0.

(The logic level output from the $\overline{\text{PWM}}$4 pin is the opposite to the timer F/F4 logic level.)

Since PWREG4 and 3 in the PWM mode are serially connected to the shift register, the values set to PWREG4 and 3 can be changed while the timer is running. The values set to PWREG4 and 3 during a run of the timer are shifted by the INTTCj interrupt request and loaded into PWREG4 and 3. While the timer is stopped, the values are shifted immediately after the programming of PWREG4 and 3. Set the lower byte (PWREG3) and upper byte (PWREG4) in this order to program PWREG4 and 3. (Programming only the lower or upper byte of the register should not be attempted.)

If executing the read instruction to PWREG4 and 3 during PWM output, the values set in the shift register is read, but not the values set in PWREG4 and 3. Therefore, after writing to the PWREG4 and 3, reading data of PWREG4 and 3 is previous value until INTTC4 is generated.

For the pin used for PWM output, the output latch of the I/O port must be set to 1.

Note 1: In the PWM mode, program the timer register PWREG4 and 3 immediately after the INTTC4 interrupt request is generated (normally in the INTTC4 interrupt service routine.) If the programming of PWREGj and the interrupt request occur at the same time, an unstable value is shifted, that may result in generation of pulse different from the programmed value until the next INTTC4 interrupt request is generated.
Note 2: When the timer is stopped during PWM output, the $\overline{\text{PWM}}$4 pin holds the output status when the timer is stopped. To change the output status, program TC4CR<TFF4> after the timer is stopped. Do not program TC4CR<TFF4> upon stopping of the timer.
Example: Fixing the $\overline{\text{PWM}}$4 pin to the high level when the TimerCounter is stopped

CLR (TC4CR).3: Stops the timer.
CLR (TC4CR).7 : Sets the $\overline{PWM4}$ pin to the high level.

Note 3: To enter the STOP mode, stop the timer and then enter the STOP mode. If the STOP mode is entered without stopping of the timer when fc, fc/2 or fs is selected as the source clock, a pulse is output from the $\overline{PWM4}$ pin during the warm-up period time after exiting the STOP mode.

Table 10-7 16-Bit PWM Output Mode

Source Clock			Resolution		Repeated Cycle	
NORMAL1/2, IDLE1/2 mode		SLOW1/2, SLEEP1/2 mode	fc = 16 MHz	fs = 32.768 kHz	fc = 16 MHz	fs = 32.768 kHz
DV7CK = 0	DV7CK = 1					
$fc/2^{11}$	$fs/2^3$ [Hz]	$fs/2^3$ [Hz]	128 μs	244.14 μs	8.39 s	16 s
$fc/2^7$	$fc/2^7$	–	8 μs	–	524.3 ms	–
$fc/2^5$	$fc/2^5$	–	2 μs	–	131.1 ms	–
$fc/2^3$	$fc/2^3$	–	500 ns	–	32.8 ms	–
fs	fs	fs	30.5 μs	30.5 μs	2 s	2 s
fc/2	fc/2	–	125 ns	–	8.2 ms	–
fc	fc	–	62.5 ns	–	4.1 ms	–

Example :Generating a pulse with 1-ms high-level width and a period of 32.768 ms (fc = 16.0 MHz)

```
        Setting ports
LDW     (PWREG3), 07D0H     : Sets the pulse width.
LD      (TC3CR), 33H        : Sets the operating clock to fc/2^3, and 16-bit PWM output
                              mode (lower byte).
LD      (TC4CR), 056H       : Sets TFF4 to the initial value 0, and 16-bit PWM signal
                              generation mode (upper byte).
LD      (TC4CR), 05EH       : Starts the timer.
```

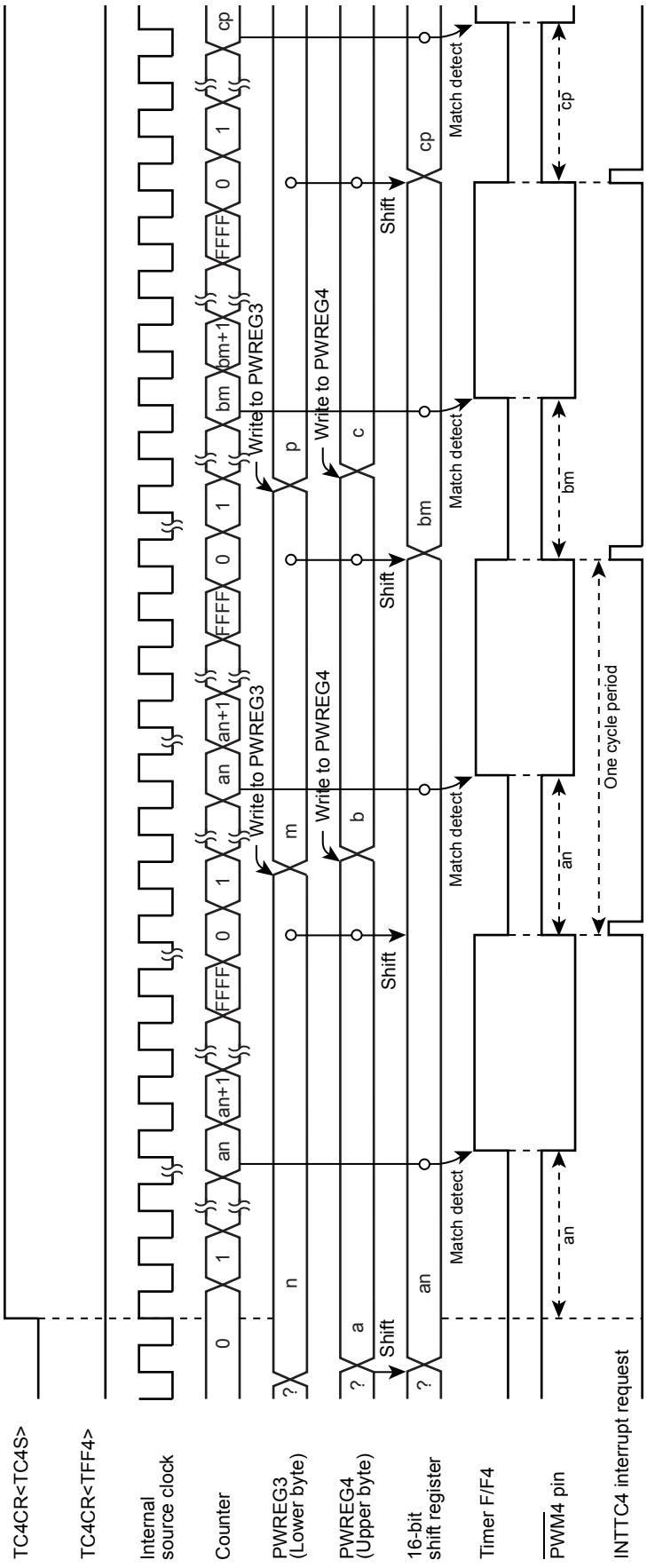


Figure 10-7 16-Bit PWM Mode Timing Chart (TC3 and TC4)

10.3.8 16-Bit Programmable Pulse Generate (PPG) Output Mode (TC3 and 4)

This mode is used to generate pulses with up to 16-bits of resolution. The timer counter 3 and 4 are cascadable to enter the 16-bit PPG mode.

The counter counts up using the internal clock or external clock. When a match between the up-counter and the timer register (PWREG3, PWREG4) value is detected, the logic level output from the timer F/F4 is switched to the opposite state. The counter continues counting. The logic level output from the timer F/F4 is switched to the opposite state again when a match between the up-counter and the timer register (TTREG3, TTREG4) value is detected, and the counter is cleared. The INTTC4 interrupt is generated at this time.

Two machine cycles are required for the high- or low-level pulse input to the TC3 pin. Therefore, a maximum frequency to be supplied is $fc/2^4$ Hz in the NORMAL1/2 or IDLE1/2 mode, and $fs/2^4$ to in the SLOW1/2 or SLEEP1/2 mode.

Since the initial value can be set to the timer F/F4 by TC4CR<TFF4>, positive and negative pulses can be generated. Upon reset, the timer F/F4 is cleared to 0.

(The logic level output from the $\overline{PPG}4$ pin is the opposite to the timer F/F4.)

Set the lower byte and upper byte in this order to program the timer register. (TTREG3 → TTREG4, PWREG3 → PWREG4) (Programming only the upper or lower byte should not be attempted.)

For PPG output, set the output latch of the I/O port to 1.

Example :Generating a pulse with 1-ms high-level width and a period of 16.385 ms (fc = 16.0 MHz)

```
        Setting ports
LDW     (PWREG3), 07D0H     : Sets the pulse width.
LDW     (TTREG3), 8002H     : Sets the cycle period.
LD      (TC3CR), 33H        : Sets the operating clock to fc/2^3, and16-bit PPG mode
                              (lower byte).
LD      (TC4CR), 057H       : Sets TFF4 to the initial value 0, and 16-bit
                              PPG mode (upper byte).
LD      (TC4CR), 05FH       : Starts the timer.
```

Note 1: In the PPG mode, do not change the PWREGi and TTREGi settings while the timer is running. Since PWREGi and TTREGi are not in the shift register configuration in the PPG mode, the new values programmed in PWREGi and TTREGi are in effect immediately after programming PWREGi and TTREGi. Therefore, if PWREGi and TTREGi are changed while the timer is running, an expected operation may not be obtained.

Note 2: When the timer is stopped during PPG output, the $\overline{PPG}4$ pin holds the output status when the timer is stopped. To change the output status, program TC4CR<TFF4> after the timer is stopped. Do not change TC4CR<TFF4> upon stopping of the timer.
Example: Fixing the $\overline{PPG}4$ pin to the high level when the TimerCounter is stopped
CLR (TC4CR).3: Stops the timer
CLR (TC4CR).7: Sets the $\overline{PPG}4$ pin to the high level

Note 3: i = 3, 4

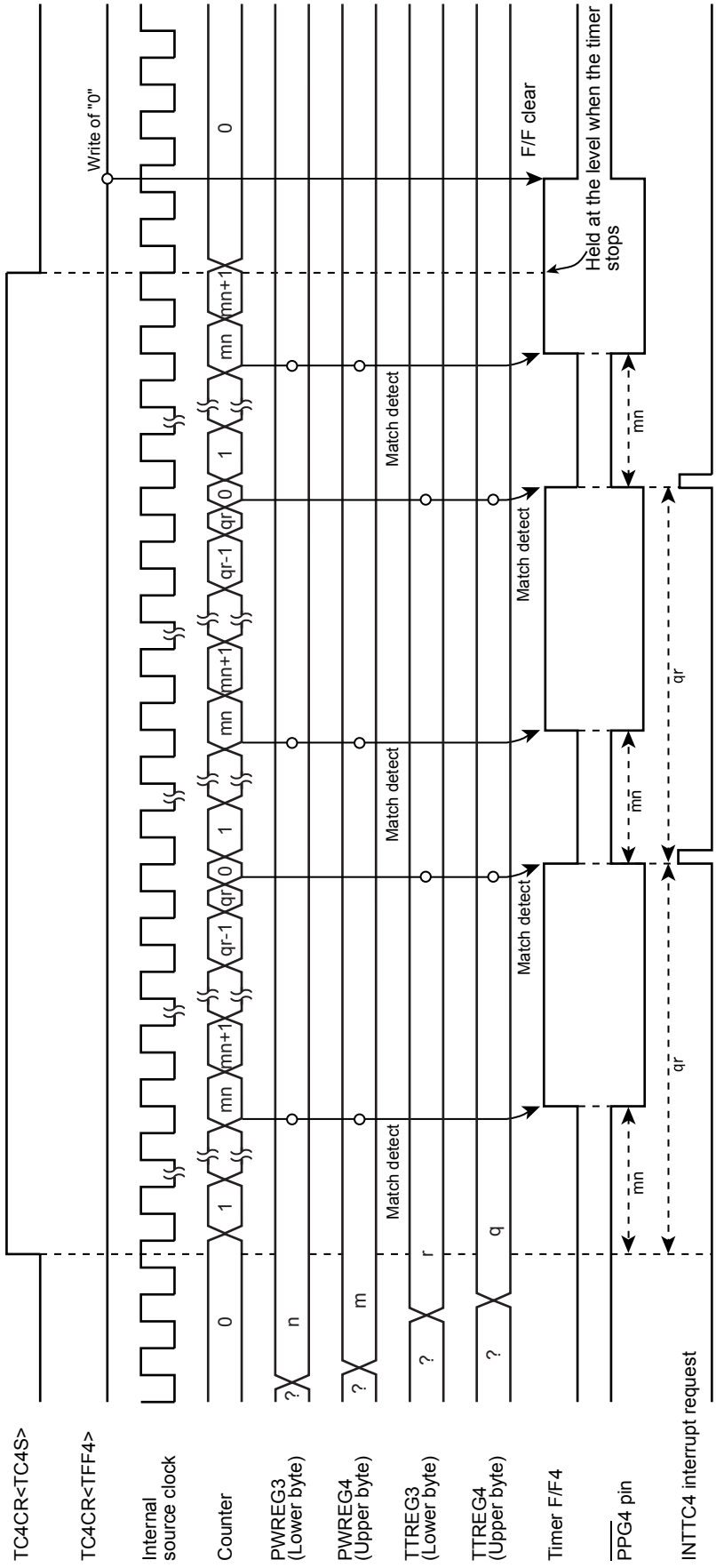


Figure 10-8 16-Bit PPG Mode Timing Chart (TC3 and TC4)

10.3.9 Warm-Up Counter Mode

In this mode, the warm-up period time is obtained to assure oscillation stability when the system clocking is switched between the high-frequency and low-frequency. The timer counter 3 and 4 are cascadable to form a 16-bit TimerCounter. The warm-up counter mode has two types of mode; switching from the high-frequency to low-frequency, and vice-versa.

Note 1: In the warm-up counter mode, fix TCiCR<TFFi> to 0. If not fixed, the $\overline{\text{PDOi}}$, $\overline{\text{PWMi}}$ and $\overline{\text{PPGi}}$ pins may output pulses.

Note 2: In the warm-up counter mode, only upper 8 bits of the timer register TTREG4 and 3 are used for match detection and lower 8 bits are not used.

Note 3: i = 3, 4

10.3.9.1 Low-Frequency Warm-up Counter Mode (NORMAL1 → NORMAL2 → SLOW2 → SLOW1)

In this mode, the warm-up period time from a stop of the low-frequency clock fs to oscillation stability is obtained. Before starting the timer, set SYSCR2<XTEN> to 1 to oscillate the low-frequency clock. When a match between the up-counter and the timer register (TTREG4, 3) value is detected after the timer is started by setting TC4CR<TC4S> to 1, the counter is cleared by generating the INTTC4 interrupt request. After stopping the timer in the INTTC4 interrupt service routine, set SYSCR2<SYSCK> to 1 to switch the system clock from the high-frequency to low-frequency, and then clear of SYSCR2<XEN> to 0 to stop the high-frequency clock.

Table 10-8 Setting Time of Low-Frequency Warm-Up Counter Mode (fs = 32.768 kHz)

Minimum Time Setting (TTREG4, 3 = 0100H)	Maximum Time Setting (TTREG4, 3 = FF00H)
7.81 ms	1.99 s

Example :After checking low-frequency clock oscillation stability with TC4 and 3, switching to the SLOW1 mode

```
                SET     (SYSCR2).6      : SYSCR2<XTEN> ← 1
                LD      (TC3CR), 43H    : Sets TFF3=0, source clock fs, and 16-bit mode.
                LD      (TC4CR), 05H    : Sets TFF4=0, and warm-up counter mode.
                LD      (TTREG3), 8000H : Sets the warm-up time.
                                          (The warm-up time depends on the oscillator characteristic.)
                DI                      : IMF ← 0
                SET     (EIRH). 1       : Enables the INTTC4.
                EI                      : IMF ← 1
                SET     (TC4CR).3       : Starts TC4 and 3.
                  :           :
PINTTC4:        CLR     (TC4CR).3       : Stops TC4 and 3.
                SET     (SYSCR2).5      : SYSCR2<SYSCK> ← 1
                                          (Switches the system clock to the low-frequency clock.)
                CLR     (SYSCR2).7      : SYSCR2<XEN> ← 0 (Stops the high-frequency clock.)
                RETI
                  :           :
VINTTC4:        DW      PINTTC4         : INTTC4 vector table
```

10.3.9.2 High-Frequency Warm-Up Counter Mode (SLOW1 → SLOW2 → NORMAL2 → NORMAL1)

In this mode, the warm-up period time from a stop of the high-frequency clock fc to the oscillation stability is obtained. Before starting the timer, set SYSCR2<XEN> to 1 to oscillate the high-frequency clock. When a match between the up-counter and the timer register (TTREG4, 3) value is detected after the timer is started by setting TC4CR<TC4S> to 1, the counter is cleared by generating the INTTC4 interrupt request. After stopping the timer in the INTTC4 interrupt service routine, clear SYSCR2<SYSCK> to 0 to switch the system clock from the low-frequency to high-frequency, and then SYSCR2<XTEN> to 0 to stop the low-frequency clock.

Table 10-9 Setting Time in High-Frequency Warm-Up Counter Mode

Minimum time Setting (TTREG4, 3 = 0100H)	Maximum time Setting (TTREG4, 3 = FF00H)
16 μs	4.08 ms

Example :After checking high-frequency clock oscillation stability with TC4 and 3, switching to the NORMAL1 mode

```
                SET     (SYSCR2).7          : SYSCR2<XEN> ← 1
                LD      (TC3CR), 63H        : Sets TFF3=0, source clock fc, and 16-bit mode.
                LD      (TC4CR), 05H        : Sets TFF4=0, and warm-up counter mode.
                LD      (TTREG3), 0F800H    : Sets the warm-up time.
                                              (The warm-up time depends on the oscillator characteristic.)
                DI                          : IMF ← 0
                SET     (EIRH). 1           : Enables the INTTC4.
                EI                          : IMF ← 1
                SET     (TC4CR).3           : Starts the TC4 and 3.
                 :          :
PINTTC4:        CLR     (TC4CR).3           : Stops the TC4 and 3.
                CLR     (SYSCR2).5          : SYSCR2<SYSCK> ← 0
                                              (Switches the system clock to the high-frequency clock.)
                CLR     (SYSCR2).6          : SYSCR2<XTEN> ← 0
                                              (Stops the low-frequency clock.)
                RETI
                 :          :
VINTTC4:        DW      PINTTC4             : INTTC4 vector table
```

11. 8-Bit TimerCounter (TC5, TC6)

11.1 Configuration

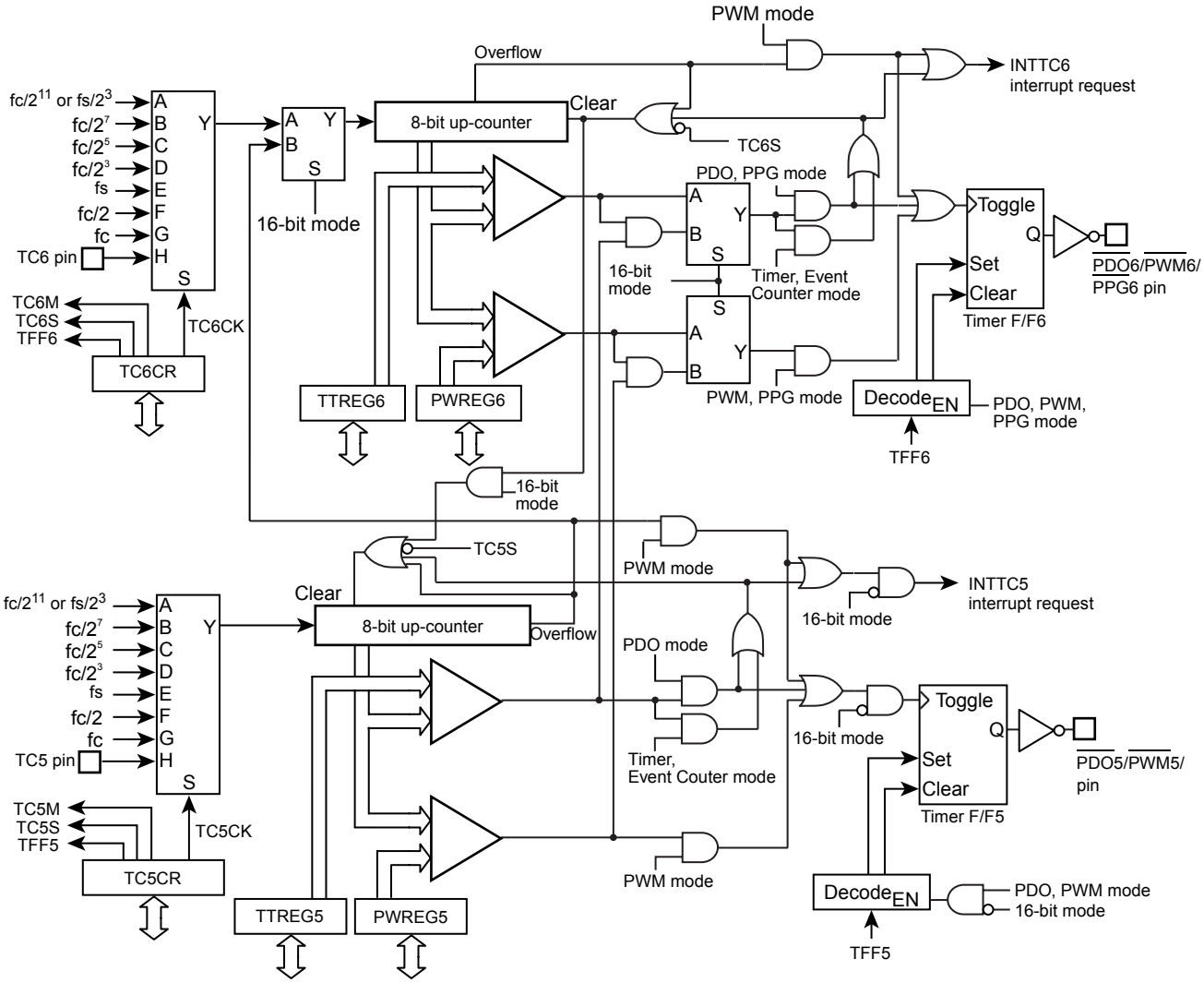


Figure 11-1 8-Bit TimerCounter 5, 6

11.2 TimerCounter Control

The TimerCounter 5 is controlled by the TimerCounter 5 control register (TC5CR) and two 8-bit timer registers (TTREG5, PWREG5).

TimerCounter 5 Timer Register

	7	6	5	4	3	2	1	0	
TTREG5 (0016H) R/W									(Initial value: 1111 1111)
PWREG5 (001AH) R/W									(Initial value: 1111 1111)

Note 1: Do not change the timer register (TTREG5) setting while the timer is running.

Note 2: Do not change the timer register (PWREG5) setting in the operating mode except the 8-bit and 16-bit PWM modes while the timer is running.

TimerCounter 5 Control Register

TC5CR (0029H)	7	6	5	4	3	2	1	0	
	TFF5	TC5CK			TC5S	TC5M			(Initial value: 0000 0000)

TFF5	Time F/F5 control	0: Clear 1: Set			R/W
TC5CK	Operating clock selection [Hz]		NORMAL1/2, IDLE1/2 mode	SLOW1/2 SLEEP1/2 mode	R/W
			DV7CK = 0	DV7CK = 1	
		000	$fc/2^{11}$	$fs/2^3$	$fs/2^3$
		001	$fc/2^7$	$fc/2^7$	–
		010	$fc/2^5$	$fc/2^5$	–
		011	$fc/2^3$	$fc/2^3$	–
		100	fs	fs	fs
		101	fc/2	fc/2	–
		110	fc	fc	fc (Note 8)
		111	TC5 pin input		
TC5S	TC5 start control	0: Operation stop and counter clear 1: Operation start			R/W
TC5M	TC5M operating mode select	000: 8-bit timer/event counter mode 001: 8-bit programmable divider output (PDO) mode 010: 8-bit pulse width modulation (PWM) output mode 011: 16-bit mode (Each mode is selectable with TC6M.) 1**: Reserved			R/W

Note 1: fc: High-frequency clock [Hz] fs: Low-frequency clock[Hz]

Note 2: Do not change the TC5M, TC5CK and TFF5 settings while the timer is running.

Note 3: To stop the timer operation (TC5S= 1 → 0), do not change the TC5M, TC5CK and TFF5 settings. To start the timer operation (TC5S= 0 → 1), TC5M, TC5CK and TFF5 can be programmed.

Note 4: To use the TimerCounter in the 16-bit mode, set the operating mode by programming TC6CR<TC6M>, where TC5M must be fixed to 011.

Note 5: To use the TimerCounter in the 16-bit mode, select the source clock by programming TC5CK. Set the timer start control and timer F/F control by programming TC6CR<TC6S> and TC6CR<TFF6>, respectively.

Note 6: The operating clock settings are limited depending on the timer operating mode. For the detailed descriptions, see Table 11-1 and Table 11-2.

Note 7: The timer register settings are limited depending on the timer operating mode. For the detailed descriptions, see Table 11-3.

Note 8: The operating clock fc in the SLOW or SLEEP mode can be used only as the high-frequency warm-up mode.

The TimerCounter 6 is controlled by the TimerCounter 6 control register (TC6CR) and two 8-bit timer registers (TTREG6 and PWREG6).

TimerCounter 6 Timer Register

TTREG6 (0017H) R/W

7	6	5	4	3	2	1	0

(Initial value: 1111 1111)

PWREG6 (001BH) R/W

7	6	5	4	3	2	1	0

(Initial value: 1111 1111)

Note 1: Do not change the timer register (TTREG6) setting while the timer is running.

Note 2: Do not change the timer register (PWREG6) setting in the operating mode except the 8-bit and 16-bit PWM modes while the timer is running.

TimerCounter 6 Control Register

TC6CR (002AH)

7	6	5	4	3	2	1	0
TFF6	TC6CK			TC6S	TC6M		

(Initial value: 0000 0000)

TFF6	Timer F/F6 control	0: Clear 1: Set			R/W
TC6CK	Operating clock selection [Hz]		NORMAL1/2, IDLE1/2 mode	SLOW1/2 SLEEP1/2 mode	R/W
			DV7CK = 0	DV7CK = 1	
		000	$fc/2^{11}$	$fs/2^3$	$fs/2^3$
		001	$fc/2^7$	$fc/2^7$	–
		010	$fc/2^5$	$fc/2^5$	–
		011	$fc/2^3$	$fc/2^3$	–
		100	fs	fs	fs
		101	fc/2	fc/2	–
		110	fc	fc	–
		111	TC6 pin input		
TC6S	TC6 start control	0: Operation stop and counter clear 1: Operation start			R/W
TC6M	TC6M operating mode select	000: 8-bit timer/event counter mode 001: 8-bit programmable divider output (PDO) mode 010: 8-bit pulse width modulation (PWM) output mode 011: Reserved 100: 16-bit timer/event counter mode 101: Warm-up counter mode 110: 16-bit pulse width modulation (PWM) output mode 111: 16-bit PPG mode			R/W

Note 1: fc: High-frequency clock [Hz] fs: Low-frequency clock [Hz]

Note 2: Do not change the TC6M, TC6CK and TFF6 settings while the timer is running.

Note 3: To stop the timer operation (TC6S= 1 → 0), do not change the TC6M, TC6CK and TFF6 settings.
To start the timer operation (TC6S= 0 → 1), TC6M, TC6CK and TFF6 can be programmed.

Note 4: When TC6M= 1** (upper byte in the 16-bit mode), the source clock becomes the TC5 overflow signal regardless of the TC6CK setting.

Note 5: To use the TimerCounter in the 16-bit mode, select the operating mode by programming TC6M, where TC5CR<TC5M> must be set to 011.

Note 6: To the TimerCounter in the 16-bit mode, select the source clock by programming TC5CR<TC5CK>. Set the timer start control and timer F/F control by programming TC6S and TFF6, respectively.

Note 7: The operating clock settings are limited depending on the timer operating mode. For the detailed descriptions, see Table 11-1 and Table 11-2.

Note 8: The timer register settings are limited depending on the timer operating mode. For the detailed descriptions, see Table 11-3.

Table 11-1 Operating Mode and Selectable Source Clock (NORMAL1/2 and IDLE1/2 Modes)

Operating mode	$fc/2^{11}$ or $fs/2^3$	$fc/2^7$	$fc/2^5$	$fc/2^3$	fs	fc/2	fc	TC5 pin input	TC6 pin input
8-bit timer	O	O	O	O	–	–	–	–	–
8-bit event counter	–	–	–	–	–	–	–	O	O
8-bit PDO	O	O	O	O	–	–	–	–	–
8-bit PWM	O	O	O	O	O	O	O	–	–
16-bit timer	O	O	O	O	–	–	–	–	–
16-bit event counter	–	–	–	–	–	–	–	O	–
Warm-up counter	–	–	–	–	O	–	–	–	–
16-bit PWM	O	O	O	O	O	O	O	O	–
16-bit PPG	O	O	O	O	–	–	–	O	–

Note 1: For 16-bit operations (16-bit timer/event counter, warm-up counter, 16-bit PWM and 16-bit PPG), set its source clock on lower bit (TC5CK).

Note 2: O : Available source clock

Table 11-2 Operating Mode and Selectable Source Clock (SLOW1/2 and SLEEP1/2 Modes)

Operating mode	$fc/2^{11}$ or $fs/2^3$	$fc/2^7$	$fc/2^5$	$fc/2^3$	fs	fc/2	fc	TC5 pin input	TC6 pin input
8-bit timer	O	–	–	–	–	–	–	–	–
8-bit event counter	–	–	–	–	–	–	–	O	O
8-bit PDO	O	–	–	–	–	–	–	–	–
8-bit PWM	O	–	–	–	O	–	–	–	–
16-bit timer	O	–	–	–	–	–	–	–	–
16-bit event counter	–	–	–	–	–	–	–	O	–
Warm-up counter	–	–	–	–	–	–	O	–	–
16-bit PWM	O	–	–	–	O	–	–	O	–
16-bit PPG	O	–	–	–	–	–	–	O	–

Note1: For 16-bit operations (16-bit timer/event counter, warm-up counter, 16-bit PWM and 16-bit PPG), set its source clock on lower bit (TC5CK).

Note2: O : Available source clock

Table 11-3 Constraints on Register Values Being Compared

Operating mode	Register Value
8-bit timer/event counter	1≤ (TTREGn) ≤255
8-bit PDO	1≤ (TTREGn) ≤255
8-bit PWM	2≤ (PWREGn) ≤254
16-bit timer/event counter	1≤ (TTREG6, 5) ≤65535
Warm-up counter	256≤ (TTREG6, 5) ≤65535
16-bit PWM	2≤ (PWREG6, 5) ≤65534
16-bit PPG	1≤ (PWREG6, 5) < (TTREG6, 5) ≤65535 and (PWREG6, 5) + 1 < (TTREG6, 5)

Note: n = 5 to 6

11.3 Function

The TimerCounter 5 and 6 have the 8-bit timer, 8-bit event counter, 8-bit programmable divider output (PDO), 8-bit pulse width modulation (PWM) output modes. The TimerCounter 5 and 6 (TC5, 6) are cascadable to form a 16-bit timer. The 16-bit timer has the operating modes such as the 16-bit timer, 16-bit event counter, warm-up counter, 16-bit pulse width modulation (PWM) output and 16-bit programmable pulse generation (PPG) modes.

11.3.1 8-Bit Timer Mode (TC5 and 6)

In the timer mode, the up-counter counts up using the internal clock. When a match between the up-counter and the timer register j (TTREGj) value is detected, an INTTCj interrupt is generated and the up-counter is cleared. After being cleared, the up-counter restarts counting.

Note 1: In the timer mode, fix TCjCR<TFFj> to 0. If not fixed, the $\overline{\text{PDOj}}$, $\overline{\text{PWMj}}$ and $\overline{\text{PPGj}}$ pins may output pulses.

Note 2: In the timer mode, do not change the TTREGj setting while the timer is running. Since TTREGj is not in the shift register configuration in the timer mode, the new value programmed in TTREGj is in effect immediately after the programming. Therefore, if TTREGi is changed while the timer is running, an expected operation may not be obtained.

Note 3: j = 5, 6

Table 11-4 Source Clock for TimerCounter 5, 6 (Internal Clock)

Source Clock			Resolution		Maximum Time Setting	
NORMAL1/2, IDLE1/2 mode		SLOW1/2, SLEEP1/2 mode	fc = 16 MHz	fs = 32.768 kHz	fc = 16 MHz	fs = 32.768 kHz
DV7CK = 0	DV7CK = 1					
$fc/2^{11}$ [Hz]	$fs/2^3$ [Hz]	$fs/2^3$ [Hz]	128 μs	244.14 μs	32.6 ms	62.3 ms
$fc/2^7$	$fc/2^7$	–	8 μs	–	2.0 ms	–
$fc/2^5$	$fc/2^5$	–	2 μs	–	510 μs	–
$fc/2^3$	$fc/2^3$	–	500 ns	–	127.5 μs	–

Example :Setting the timer mode with source clock $fc/2^7$ Hz and generating an interrupt 80 μs later (TimerCounter6, fc = 16.0 MHz)

```
LD      (TTREG6), 0AH          : Sets the timer register (80 μs÷2^7/fc = 0AH).
DI
SET     (EIRE). 2              : Enables INTTC6 interrupt.
EI
LD      (TC6CR), 00010000B     : Sets the operating clock to fc/2^7, and 8-bit timer mode.
LD      (TC6CR), 00011000B     : Starts TC6.
```

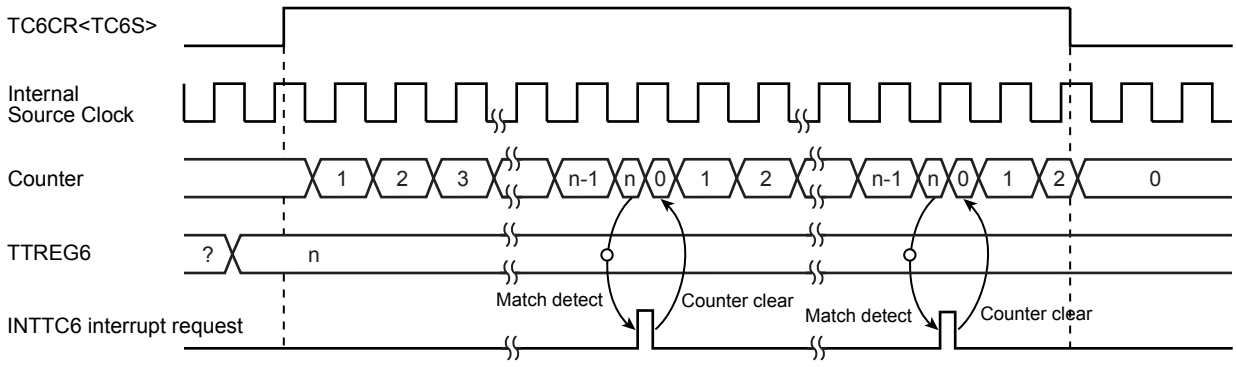


Figure 11-2 8-Bit Timer Mode Timing Chart (TC6)

11.3.2 8-Bit Event Counter Mode (TC5, 6)

In the 8-bit event counter mode, the up-counter counts up at the falling edge of the input pulse to the TCj pin. When a match between the up-counter and the TTREGj value is detected, an INTTCj interrupt is generated and the up-counter is cleared. After being cleared, the up-counter restarts counting at the falling edge of the input pulse to the TCj pin. Two machine cycles are required for the low- or high-level pulse input to the TCj pin. Therefore, a maximum frequency to be supplied is $fc/2^4$ Hz in the NORMAL1/2 or IDLE1/2 mode, and $fs/2^4$ Hz in the SLOW1/2 or SLEEP1/2 mode.

Note 1: In the event counter mode, fix TCjCR<TFFj> to 0. If not fixed, the $\overline{\text{PDOj, PWMj}}$ and $\overline{\text{PPGj}}$ pins may output pulses.

Note 2: In the event counter mode, do not change the TTREGj setting while the timer is running. Since TTREGj is not in the shift register configuration in the event counter mode, the new value programmed in TTREGj is in effect immediately after the programming. Therefore, if TTREGi is changed while the timer is running, an expected operation may not be obtained.

Note 3: j = 5, 6

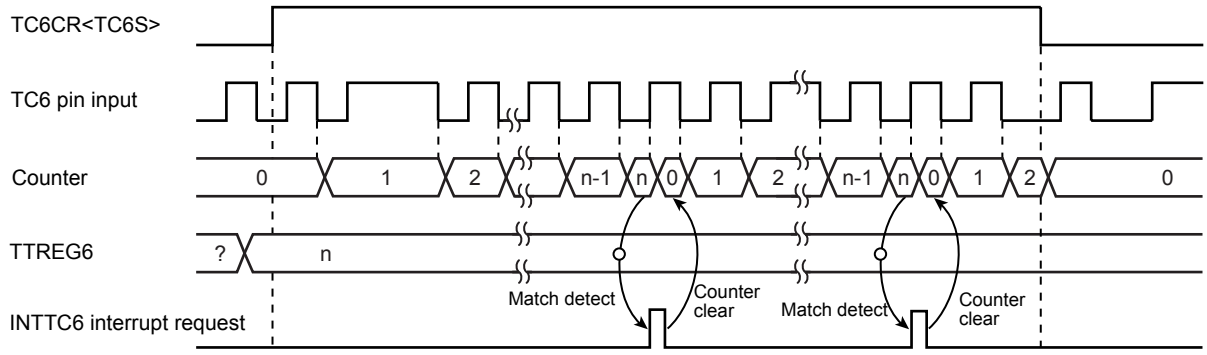


Figure 11-3 8-Bit Event Counter Mode Timing Chart (TC6)

11.3.3 8-Bit Programmable Divider Output (PDO) Mode (TC5, 6)

This mode is used to generate a pulse with a 50% duty cycle from the $\overline{\text{PDOj}}$ pin.

In the PDO mode, the up-counter counts up using the internal clock. When a match between the up-counter and the TTREGj value is detected, the logic level output from the $\overline{\text{PDOj}}$ pin is switched to the opposite state and the up-counter is cleared. The INTTCj interrupt request is generated at the time. The logic state opposite to the timer F/Fj logic level is output from the $\overline{\text{PDOj}}$ pin. An arbitrary value can be set to the timer F/Fj by TCjCR<TFFj>. Upon reset, the timer F/Fj value is initialized to 0.

To use the programmable divider output, set the output latch of the I/O port to 1.

Example :Generating 1024 Hz pulse using TC6 (fc = 16.0 MHz)

```
                Setting port
LD      (TTREG6),  3DH          : 1/1024÷2^7/fc÷2 = 3DH
LD      (TC6CR),   00010001B    : Sets the operating clock to fc/2^7, and 8-bit PDO mode.
LD      (TC6CR),  00011001B     : Starts TC6.
```

Note 1: In the programmable divider output mode, do not change the TTREGj setting while the timer is running. Since TTREGj is not in the shift register configuration in the programmable divider output mode, the new value programmed in TTREGj is in effect immediately after programming. Therefore, if TTREGi is changed while the timer is running, an expected operation may not be obtained.

Note 2: When the timer is stopped during PDO output, the $\overline{\text{PDOj}}$ pin holds the output status when the timer is stopped. To change the output status, program TCjCR<TFFj> after the timer is stopped. Do not change the TCjCR<TFFj> setting upon stopping of the timer.
Example: Fixing the $\overline{\text{PDOj}}$ pin to the high level when the TimerCounter is stopped
CLR (TCjCR).3: Stops the timer.
CLR (TCjCR).7: Sets the $\overline{\text{PDOj}}$ pin to the high level.

Note 3: j = 5, 6

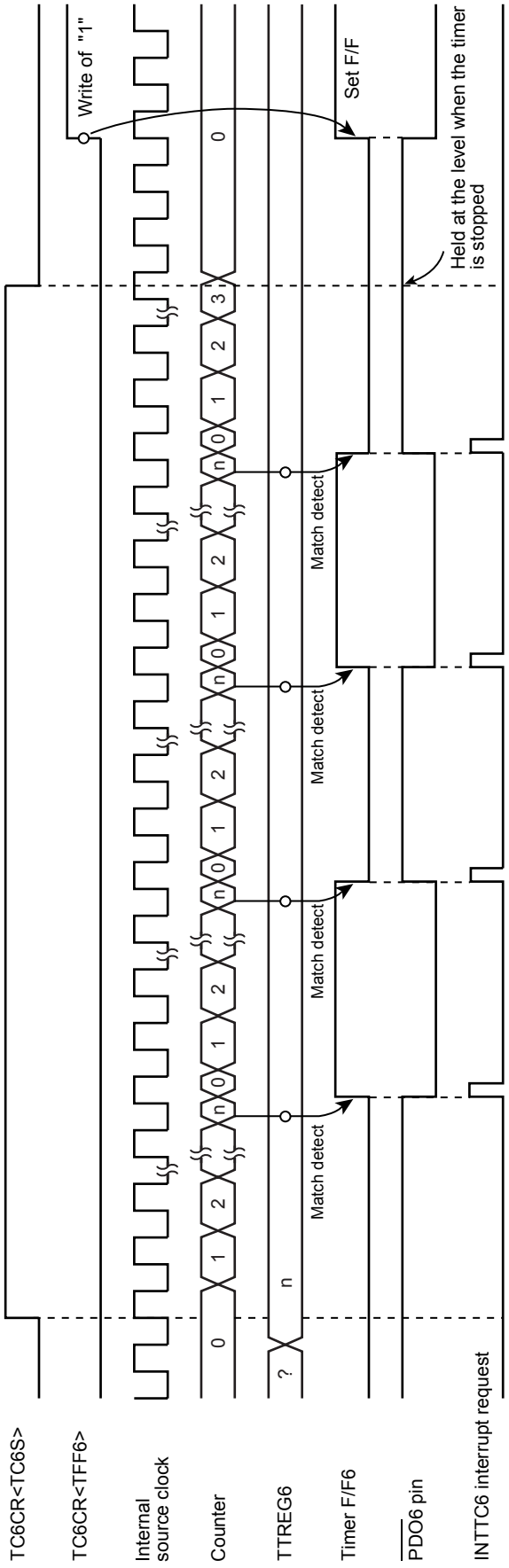


Figure 11-4 8-Bit PDO Mode Timing Chart (TC6)

11.3.4 8-Bit Pulse Width Modulation (PWM) Output Mode (TC5, 6)

This mode is used to generate a pulse-width modulated (PWM) signals with up to 8 bits of resolution. The up-counter counts up using the internal clock.

When a match between the up-counter and the PWREGj value is detected, the logic level output from the timer F/Fj is switched to the opposite state. The counter continues counting. The logic level output from the timer F/Fj is switched to the opposite state again by the up-counter overflow, and the counter is cleared. The INTTCj interrupt request is generated at this time.

Since the initial value can be set to the timer F/Fj by TCjCR<TFFj>, positive and negative pulses can be generated. Upon reset, the timer F/Fj is cleared to 0.

(The logic level output from the $\overline{\text{PWMj}}$ pin is the opposite to the timer F/Fj logic level.)

Since PWREGj in the PWM mode is serially connected to the shift register, the value set to PWREGj can be changed while the timer is running. The value set to PWREGj during a run of the timer is shifted by the INTTCj interrupt request and loaded into PWREGj. While the timer is stopped, the value is shifted immediately after the programming of PWREGj. If executing the read instruction to PWREGj during PWM output, the value in the shift register is read, but not the value set in PWREGj. Therefore, after writing to PWREGj, the reading data of PWREGj is previous value until INTTCj is generated.

For the pin used for PWM output, the output latch of the I/O port must be set to 1.

Note 1: In the PWM mode, program the timer register PWREGj immediately after the INTTCj interrupt request is generated (normally in the INTTCj interrupt service routine.) If the programming of PWREGj and the interrupt request occur at the same time, an unstable value is shifted, that may result in generation of the pulse different from the programmed value until the next INTTCj interrupt request is generated.

Note 2: When the timer is stopped during PWM output, the $\overline{\text{PWMj}}$ pin holds the output status when the timer is stopped. To change the output status, program TCjCR<TFFj> after the timer is stopped. Do not change the TCjCR<TFFj> upon stopping of the timer.
Example: Fixing the $\overline{\text{PWMj}}$ pin to the high level when the TimerCounter is stopped
CLR (TCjCR).3: Stops the timer.
CLR (TCjCR).7: Sets the $\overline{\text{PWMj}}$ pin to the high level.

Note 3: To enter the STOP mode during PWM output, stop the timer and then enter the STOP mode. If the STOP mode is entered without stopping the timer when fc, fc/2 or fs is selected as the source clock, a pulse is output from the $\overline{\text{PWMj}}$ pin during the warm-up period time after exiting the STOP mode.

Note 4: j = 5, 6

Table 11-5 PWM Output Mode

Source Clock			Resolution		Repeated Cycle	
NORMAL1/2, IDLE1/2 mode		SLOW1/2, SLEEP1/2 mode	fc = 16 MHz	fs = 32.768 kHz	fc = 16 MHz	fs = 32.768 kHz
DV7CK = 0	DV7CK = 1					
$fc/2^{11}$ [Hz]	$fs/2^3$ [Hz]	$fs/2^3$ [Hz]	128 μs	244.14 μs	32.8 ms	62.5 ms
$fc/2^7$	$fc/2^7$	–	8 μs	–	2.05 ms	–
$fc/2^5$	$fc/2^5$	–	2 μs	–	512 μs	–
$fc/2^3$	$fc/2^3$	–	500 ns	–	128 μs	–
fs	fs	fs	30.5 μs	30.5 μs	7.81 ms	7.81 ms
fc/2	fc/2	–	125 ns	–	32 μs	–
fc	fc	–	62.5 ns	–	16 μs	–

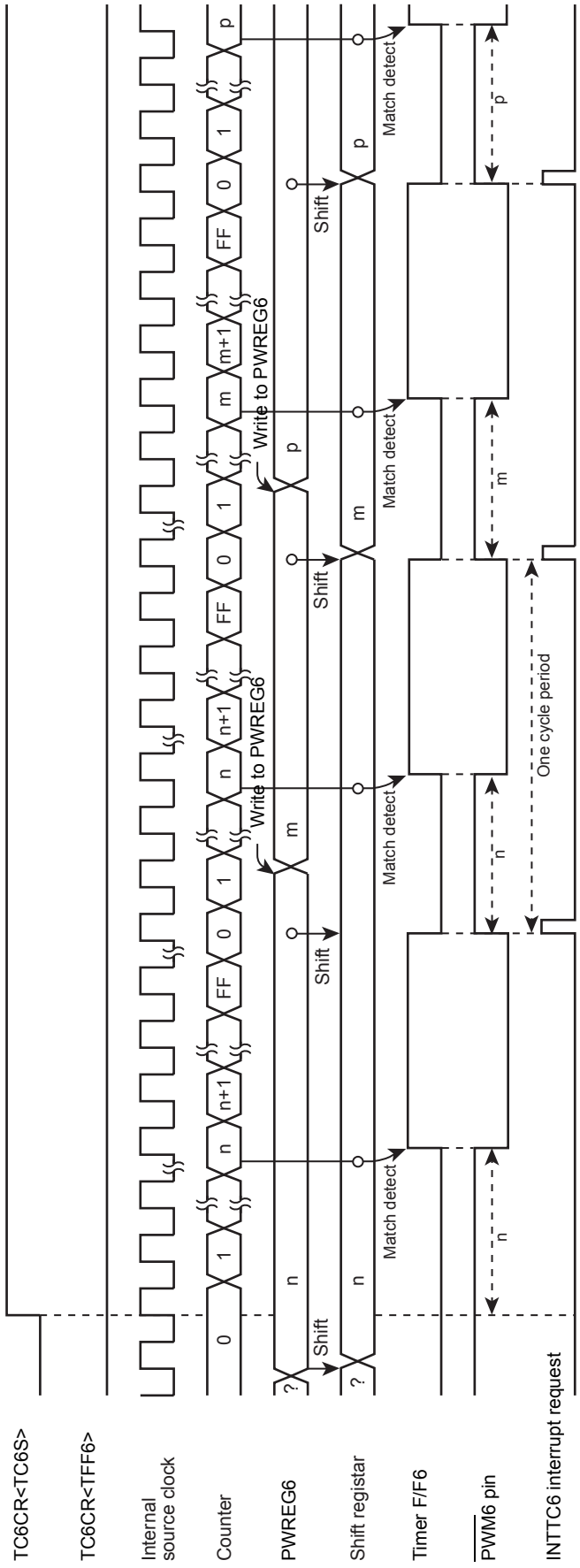


Figure 11-5 8-Bit PWM Mode Timing Chart (TC6)

11.3.5 16-Bit Timer Mode (TC5 and 6)

In the timer mode, the up-counter counts up using the internal clock. The TimerCounter 5 and 6 are cascadable to form a 16-bit timer.

When a match between the up-counter and the timer register (TTREG5, TTREG6) value is detected after the timer is started by setting TC6CR<TC6S> to 1, an INTTC6 interrupt is generated and the up-counter is cleared. After being cleared, the up-counter continues counting. Program the lower byte and upper byte in this order in the timer register. (Programming only the upper or lower byte should not be attempted.)

Note 1: In the timer mode, fix TCjCR<TFFj> to 0. If not fixed, the $\overline{PDOj}$, $\overline{PWMj}$, and $\overline{PPGj}$ pins may output a pulse.

Note 2: In the timer mode, do not change the TTREGj setting while the timer is running. Since TTREGj is not in the shift register configuration in the timer mode, the new value programmed in TTREGj is in effect immediately after programming of TTREGj. Therefore, if TTREGj is changed while the timer is running, an expected operation may not be obtained.

Note 3: j = 5, 6

Table 11-6 Source Clock for 16-Bit Timer Mode

Source Clock			Resolution		Maximum Time Setting	
NORMAL1/2, IDLE1/2 mode		SLOW1/2, SLEEP1/2 mode	fc = 16 MHz	fs = 32.768 kHz	fc = 16 MHz	fs = 32.768 kHz
DV7CK = 0	DV7CK = 1					
$fc/2^{11}$	$fs/2^3$	$fs/2^3$	128 μs	244.14 μs	8.39 s	16 s
$fc/2^7$	$fc/2^7$	–	8 μs	–	524.3 ms	–
$fc/2^5$	$fc/2^5$	–	2 μs	–	131.1 ms	–
$fc/2^3$	$fc/2^3$	–	500 ns	–	32.8 ms	–

Example :Setting the timer mode with source clock $fc/2^7$ Hz, and generating an interrupt 300 ms later (fc = 16.0 MHz)

```
LDW     (TTREG5), 927CH     : Sets the timer register (300 ms÷2^7/fc = 927CH).
DI
SET     (EIRE). 2           : Enables INTTC6 interrupt.
EI
LD      (TC5CR), 13H        :Sets the operating clock to fc/2^7, and 16-bit timer mode
                             (lower byte).
LD      (TC6CR), 04H        : Sets the 16-bit timer mode (upper byte).
LD      (TC6CR), 0CH        : Starts the timer.
```

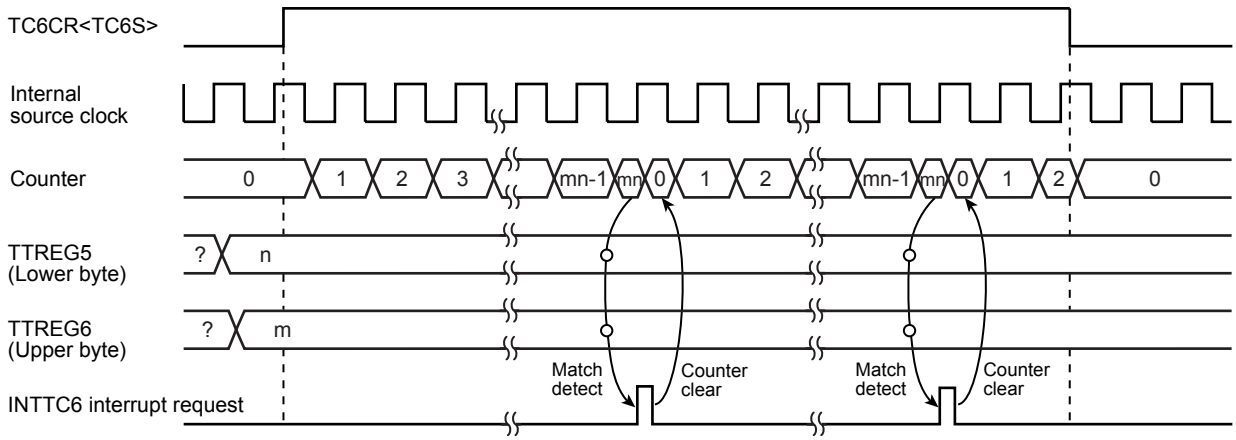


Figure 11-6 16-Bit Timer Mode Timing Chart (TC5 and TC6)

11.3.6 16-Bit Event Counter Mode (TC5 and 6)

In the event counter mode, the up-counter counts up at the falling edge to the TC5 pin. The TimerCounter 5 and 6 are cascadable to form a 16-bit event counter.

When a match between the up-counter and the timer register (TTREG5, TTREG6) value is detected after the timer is started by setting TC6CR<TC6S> to 1, an INTTC6 interrupt is generated and the up-counter is cleared.

After being cleared, the up-counter restarts counting at the falling edge of the input pulse to the TC5 pin. Two machine cycles are required for the low- or high-level pulse input to the TC5 pin.

Therefore, a maximum frequency to be supplied is $fc/2^4$ Hz in the NORMAL1/2 or IDLE1/2 mode, and $fs/2^4$ in the SLOW1/2 or SLEEP1/2 mode. Program the lower byte (TTREG5), and upper byte (TTREG6) in this order in the timer register. (Programming only the upper or lower byte should not be attempted.)

Note 1: In the event counter mode, fix TCjCR<TFFj> to 0. If not fixed, the $\overline{\text{PDOj}}$, $\overline{\text{PWMj}}$ and $\overline{\text{PPGj}}$ pins may output pulses.
Note 2: In the event counter mode, do not change the TTREGj setting while the timer is running. Since TTREGj is not in the shift register configuration in the event counter mode, the new value programmed in TTREGj is in effect immediately after the programming. Therefore, if TTREGj is changed while the timer is running, an expected operation may not be obtained.
Note 3: j = 5, 6

11.3.7 16-Bit Pulse Width Modulation (PWM) Output Mode (TC5 and 6)

This mode is used to generate a pulse-width modulated (PWM) signals with up to 16 bits of resolution. The TimerCounter 5 and 6 are cascadable to form the 16-bit PWM signal generator.

The counter counts up using the internal clock or external clock.

When a match between the up-counter and the timer register (PWREG5, PWREG6) value is detected, the logic level output from the timer F/F6 is switched to the opposite state. The counter continues counting. The logic level output from the timer F/F6 is switched to the opposite state again by the counter overflow, and the counter is cleared. The INTTC6 interrupt is generated at this time.

Two machine cycles are required for the high- or low-level pulse input to the TC5 pin. Therefore, a maximum frequency to be supplied is $fc/2^4$ Hz in the NORMAL1/2 or IDLE1/2 mode, and $fs/2^4$ to in the SLOW1/2 or SLEEP1/2 mode.

Since the initial value can be set to the timer F/F6 by TC6CR<TFF6>, positive and negative pulses can be generated. Upon reset, the timer F/F6 is cleared to 0.

(The logic level output from the $\overline{\text{PWM}}$6 pin is the opposite to the timer F/F6 logic level.)

Since PWREG6 and 5 in the PWM mode are serially connected to the shift register, the values set to PWREG6 and 5 can be changed while the timer is running. The values set to PWREG6 and 5 during a run of the timer are shifted by the INTTCj interrupt request and loaded into PWREG6 and 5. While the timer is stopped, the values are shifted immediately after the programming of PWREG6 and 5. Set the lower byte (PWREG5) and upper byte (PWREG6) in this order to program PWREG6 and 5. (Programming only the lower or upper byte of the register should not be attempted.)

If executing the read instruction to PWREG6 and 5 during PWM output, the values set in the shift register is read, but not the values set in PWREG6 and 5. Therefore, after writing to the PWREG6 and 5, reading data of PWREG6 and 5 is previous value until INTTC6 is generated.

For the pin used for PWM output, the output latch of the I/O port must be set to 1.

Note 1: In the PWM mode, program the timer register PWREG6 and 5 immediately after the INTTC6 interrupt request is generated (normally in the INTTC6 interrupt service routine.) If the programming of PWREGj and the interrupt request occur at the same time, an unstable value is shifted, that may result in generation of pulse different from the programmed value until the next INTTC6 interrupt request is generated.
Note 2: When the timer is stopped during PWM output, the $\overline{\text{PWM}}$6 pin holds the output status when the timer is stopped. To change the output status, program TC6CR<TFF6> after the timer is stopped. Do not program TC6CR<TFF6> upon stopping of the timer.
Example: Fixing the $\overline{\text{PWM}}$6 pin to the high level when the TimerCounter is stopped

CLR (TC6CR).3: Stops the timer.
CLR (TC6CR).7 : Sets the $\overline{PWM6}$ pin to the high level.

Note 3: To enter the STOP mode, stop the timer and then enter the STOP mode. If the STOP mode is entered without stopping of the timer when fc, fc/2 or fs is selected as the source clock, a pulse is output from the $\overline{PWM6}$ pin during the warm-up period time after exiting the STOP mode.

Table 11-7 16-Bit PWM Output Mode

Source Clock			Resolution		Repeated Cycle	
NORMAL1/2, IDLE1/2 mode		SLOW1/2, SLEEP1/2 mode	fc = 16 MHz	fs = 32.768 kHz	fc = 16 MHz	fs = 32.768 kHz
DV7CK = 0	DV7CK = 1					
$fc/2^{11}$	$fs/2^3$ [Hz]	$fs/2^3$ [Hz]	128 μs	244.14 μs	8.39 s	16 s
$fc/2^7$	$fc/2^7$	–	8 μs	–	524.3 ms	–
$fc/2^5$	$fc/2^5$	–	2 μs	–	131.1 ms	–
$fc/2^3$	$fc/2^3$	–	500 ns	–	32.8 ms	–
fs	fs	fs	30.5 μs	30.5 μs	2 s	2 s
fc/2	fc/2	–	125 ns	–	8.2 ms	–
fc	fc	–	62.5 ns	–	4.1 ms	–

Example :Generating a pulse with 1-ms high-level width and a period of 32.768 ms (fc = 16.0 MHz)

```
        Setting ports
LDW     (PWREG5), 07D0H     : Sets the pulse width.
LD      (TC5CR), 33H        : Sets the operating clock to fc/2^3, and 16-bit PWM output
                              mode (lower byte).
LD      (TC6CR), 056H       : Sets TFF6 to the initial value 0, and 16-bit PWM signal
                              generation mode (upper byte).
LD      (TC6CR), 05EH       : Starts the timer.
```

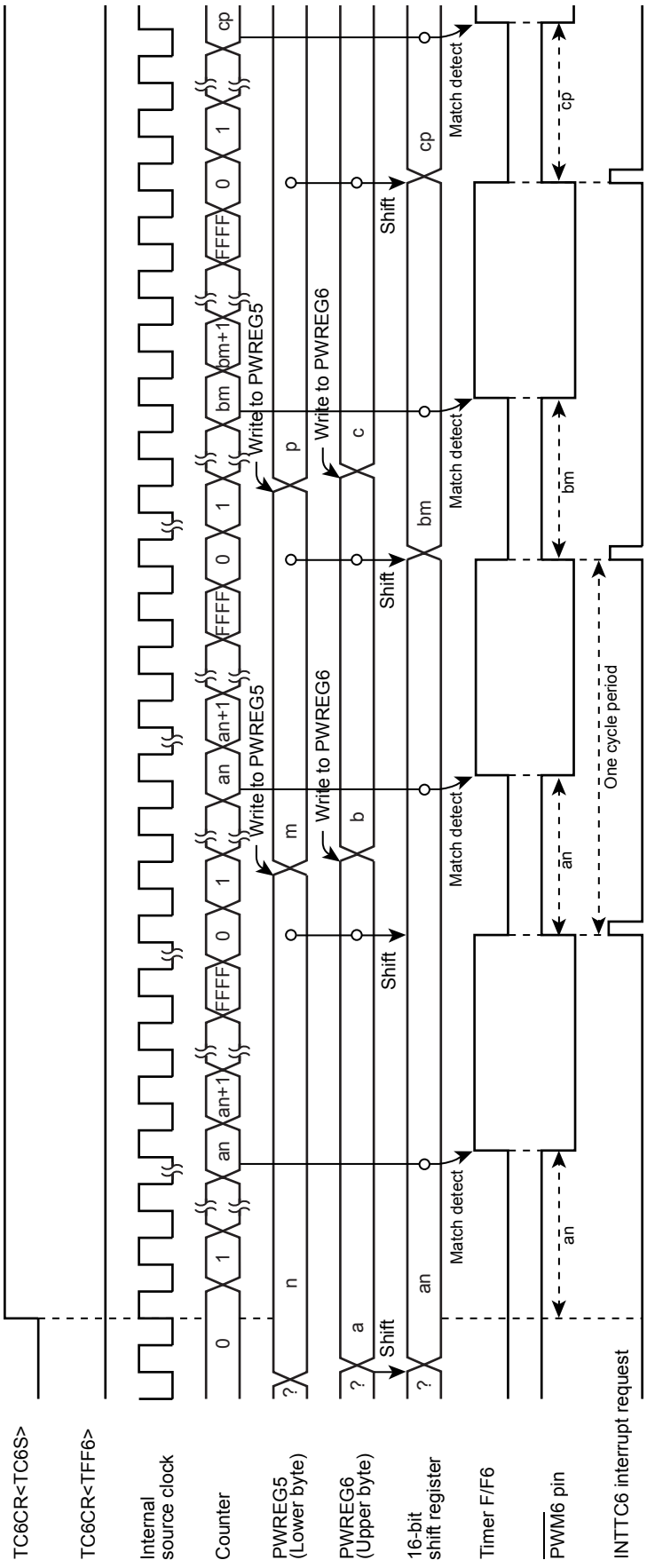


Figure 11-7 16-Bit PWM Mode Timing Chart (TC5 and TC6)

11.3.8 16-Bit Programmable Pulse Generate (PPG) Output Mode (TC5 and 6)

This mode is used to generate pulses with up to 16-bits of resolution. The timer counter 5 and 6 are cascadable to enter the 16-bit PPG mode.

The counter counts up using the internal clock or external clock. When a match between the up-counter and the timer register (PWREG5, PWREG6) value is detected, the logic level output from the timer F/F6 is switched to the opposite state. The counter continues counting. The logic level output from the timer F/F6 is switched to the opposite state again when a match between the up-counter and the timer register (TTREG5, TTREG6) value is detected, and the counter is cleared. The INTTC6 interrupt is generated at this time.

Two machine cycles are required for the high- or low-level pulse input to the TC5 pin. Therefore, a maximum frequency to be supplied is $fc/2^4$ Hz in the NORMAL1/2 or IDLE1/2 mode, and $fs/2^4$ to in the SLOW1/2 or SLEEP1/2 mode.

Since the initial value can be set to the timer F/F6 by TC6CR<TFF6>, positive and negative pulses can be generated. Upon reset, the timer F/F6 is cleared to 0.

(The logic level output from the $\overline{PPG}$6 pin is the opposite to the timer F/F6.)

Set the lower byte and upper byte in this order to program the timer register. (TTREG5 → TTREG6, PWREG5 → PWREG6) (Programming only the upper or lower byte should not be attempted.)

For PPG output, set the output latch of the I/O port to 1.

Example :Generating a pulse with 1-ms high-level width and a period of 16.385 ms (fc = 16.0 MHz)

```
        Setting ports
LDW     (PWREG5), 07D0H     : Sets the pulse width.
LDW     (TTREG5), 8002H     : Sets the cycle period.
LD      (TC5CR), 33H        : Sets the operating clock to fc/2^3, and16-bit PPG mode
                              (lower byte).
LD      (TC6CR), 057H       : Sets TFF6 to the initial value 0, and 16-bit
                              PPG mode (upper byte).
LD      (TC6CR), 05FH       : Starts the timer.
```

Note 1: In the PPG mode, do not change the PWREGi and TTREGi settings while the timer is running. Since PWREGi and TTREGi are not in the shift register configuration in the PPG mode, the new values programmed in PWREGi and TTREGi are in effect immediately after programming PWREGi and TTREGi. Therefore, if PWREGi and TTREGi are changed while the timer is running, an expected operation may not be obtained.

Note 2: When the timer is stopped during PPG output, the $\overline{PPG}$6 pin holds the output status when the timer is stopped. To change the output status, program TC6CR<TFF6> after the timer is stopped. Do not change TC6CR<TFF6> upon stopping of the timer.
Example: Fixing the $\overline{PPG}$6 pin to the high level when the TimerCounter is stopped
CLR (TC6CR).3: Stops the timer
CLR (TC6CR).7: Sets the $\overline{PPG}$6 pin to the high level

Note 3: i = 5, 6

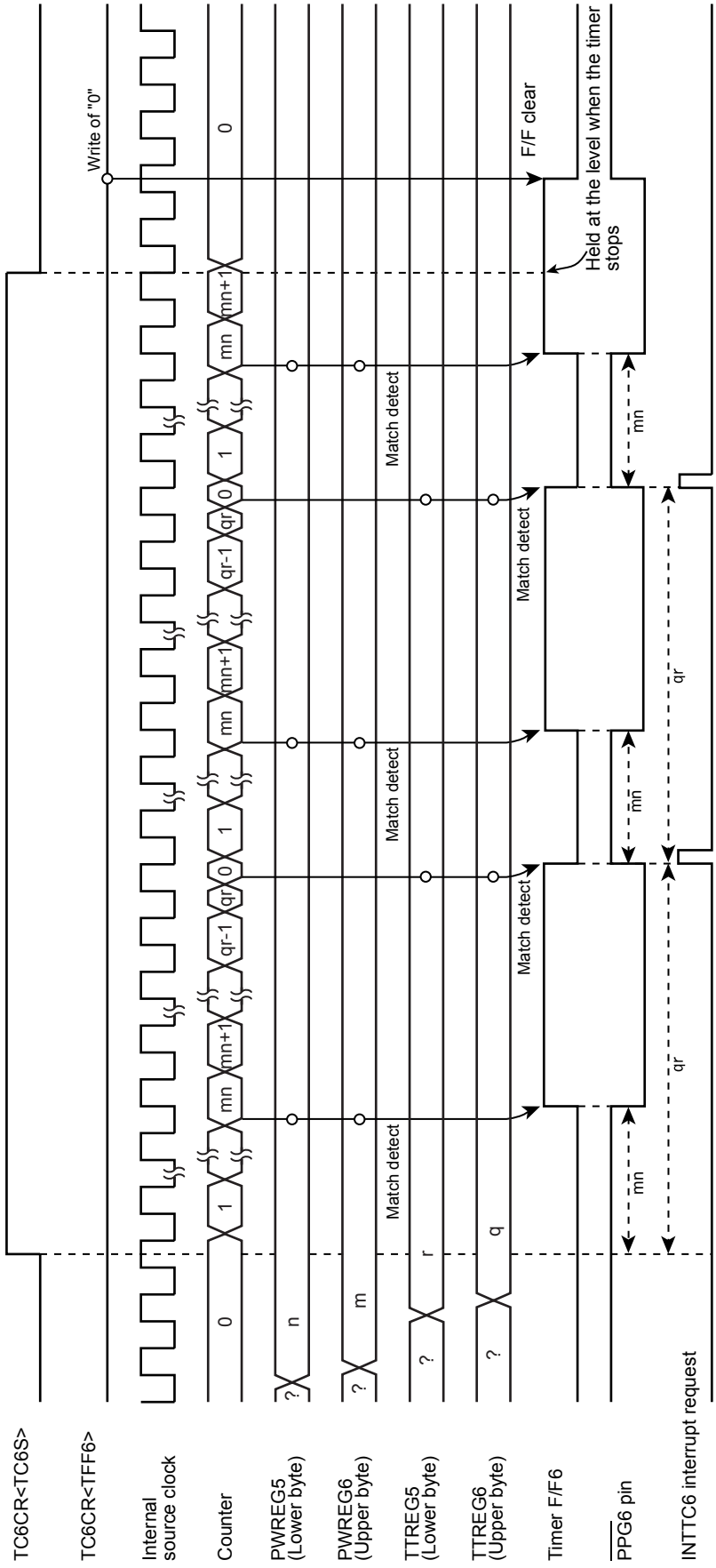


Figure 11-8 16-Bit PPG Mode Timing Chart (TC5 and TC6)

11.3.9 Warm-Up Counter Mode

In this mode, the warm-up period time is obtained to assure oscillation stability when the system clocking is switched between the high-frequency and low-frequency. The timer counter 5 and 6 are cascadable to form a 16-bit TimerCounter. The warm-up counter mode has two types of mode; switching from the high-frequency to low-frequency, and vice-versa.

Note 1: In the warm-up counter mode, fix TCiCR<TFFi> to 0. If not fixed, the $\overline{\text{PDOi}}$, $\overline{\text{PWMi}}$ and $\overline{\text{PPGi}}$ pins may output pulses.

Note 2: In the warm-up counter mode, only upper 8 bits of the timer register TTREG6 and 5 are used for match detection and lower 8 bits are not used.

Note 3: i = 5, 6

11.3.9.1 Low-Frequency Warm-up Counter Mode (NORMAL1 → NORMAL2 → SLOW2 → SLOW1)

In this mode, the warm-up period time from a stop of the low-frequency clock fs to oscillation stability is obtained. Before starting the timer, set SYSCR2<XTEN> to 1 to oscillate the low-frequency clock. When a match between the up-counter and the timer register (TTREG6, 5) value is detected after the timer is started by setting TC6CR<TC6S> to 1, the counter is cleared by generating the INTTC6 interrupt request. After stopping the timer in the INTTC6 interrupt service routine, set SYSCR2<SYSCK> to 1 to switch the system clock from the high-frequency to low-frequency, and then clear of SYSCR2<XEN> to 0 to stop the high-frequency clock.

Table 11-8 Setting Time of Low-Frequency Warm-Up Counter Mode (fs = 32.768 kHz)

Minimum Time Setting (TTREG6, 5 = 0100H)	Maximum Time Setting (TTREG6, 5 = FF00H)
7.81 ms	1.99 s

Example :After checking low-frequency clock oscillation stability with TC6 and 5, switching to the SLOW1 mode

```
                SET     (SYSCR2).6      : SYSCR2<XTEN> ← 1
                LD      (TC5CR), 43H    : Sets TFF5=0, source clock fs, and 16-bit mode.
                LD      (TC6CR), 05H    : Sets TFF6=0, and warm-up counter mode.
                LD      (TTREG5), 8000H : Sets the warm-up time.
                                          (The warm-up time depends on the oscillator characteristic.)
                DI                      : IMF ← 0
                SET     (EIRE). 2       : Enables the INTTC6.
                EI                      : IMF ← 1
                SET     (TC6CR).3       : Starts TC6 and 5.
                  :       :
PINTTC6:        CLR     (TC6CR).3       : Stops TC6 and 5.
                SET     (SYSCR2).5      : SYSCR2<SYSCK> ← 1
                                          (Switches the system clock to the low-frequency clock.)
                CLR     (SYSCR2).7      : SYSCR2<XEN> ← 0 (Stops the high-frequency clock.)
                RETI
                  :       :
VINTTC6:        DW      PINTTC6         : INTTC6 vector table
```

11.3.9.2 High-Frequency Warm-Up Counter Mode (SLOW1 → SLOW2 → NORMAL2 → NORMAL1)

In this mode, the warm-up period time from a stop of the high-frequency clock fc to the oscillation stability is obtained. Before starting the timer, set SYSCR2<XEN> to 1 to oscillate the high-frequency clock. When a match between the up-counter and the timer register (TTREG6, 5) value is detected after the timer is started by setting TC6CR<TC6S> to 1, the counter is cleared by generating the INTTC6 interrupt request. After stopping the timer in the INTTC6 interrupt service routine, clear SYSCR2<SYSCK> to 0 to switch the system clock from the low-frequency to high-frequency, and then SYSCR2<XTEN> to 0 to stop the low-frequency clock.

Table 11-9 Setting Time in High-Frequency Warm-Up Counter Mode

Minimum time Setting (TTREG6, 5 = 0100H)	Maximum time Setting (TTREG6, 5 = FF00H)
16 μs	4.08 ms

Example :After checking high-frequency clock oscillation stability with TC6 and 5, switching to the NORMAL1 mode

```
                SET     (SYSCR2).7          : SYSCR2<XEN> ← 1
                LD      (TC5CR), 63H        : Sets TFF5=0, source clock fc, and 16-bit mode.
                LD      (TC6CR), 05H        : Sets TFF6=0, and warm-up counter mode.
                LD      (TTREG5), 0F800H    : Sets the warm-up time.
                                              (The warm-up time depends on the oscillator characteristic.)
                DI                          : IMF ← 0
                SET     (EIRE). 2           : Enables the INTTC6.
                EI                          : IMF ← 1
                SET     (TC6CR).3           : Starts the TC6 and 5.
                 :          :
PINTTC6:        CLR     (TC6CR).3           : Stops the TC6 and 5.
                CLR     (SYSCR2).5          : SYSCR2<SYSCK> ← 0
                                              (Switches the system clock to the high-frequency clock.)
                CLR     (SYSCR2).6          : SYSCR2<XTEN> ← 0
                                              (Stops the low-frequency clock.)
                RETI
                 :          :
VINTTC6:        DW      PINTTC6             : INTTC6 vector table
```

12. Asynchronous Serial interface (UART1)

12.1 Configuration

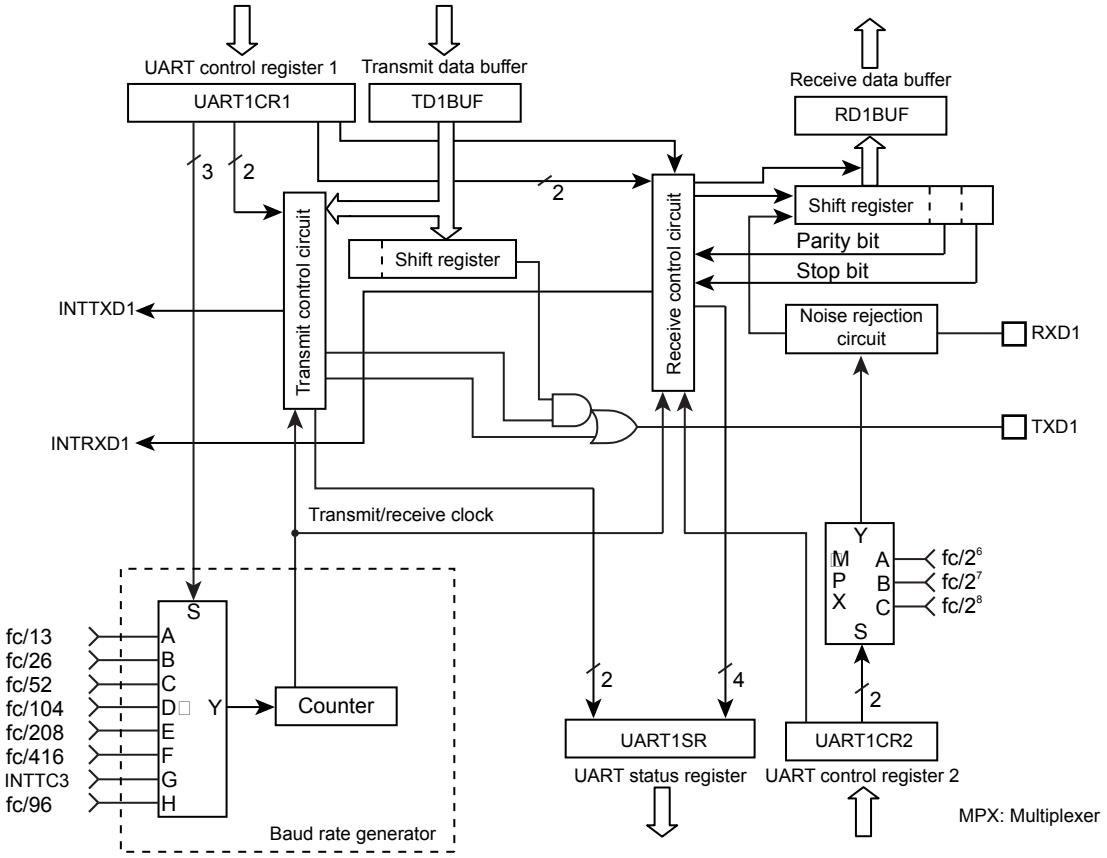


Figure 12-1 UART1 (Asynchronous Serial Interface)

12.2 Control

UART1 is controlled by the UART1 Control Registers (UART1CR1, UART1CR2). The operating status can be monitored using the UART status register (UART1SR).

UART1 Control Register1

UART1CR1 (0F95H)

7	6	5	4	3	2	1	0
TXE	RXE	STBT	EVEN	PE	BRG		

(Initial value: 0000 0000)

TXE	Transfer operation	0: Disable 1: Enable	Write only
RXE	Receive operation	0: Disable 1: Enable	
STBT	Transmit stop bit length	0: 1 bit 1: 2 bits	
EVEN	Even-numbered parity	0: Odd-numbered parity 1: Even-numbered parity	
PE	Parity addition	0: No parity 1: Parity	
BRG	Transmit clock select	000: fc/13 [Hz] 001: fc/26 010: fc/52 011: fc/104 100: fc/208 101: fc/416 110: TC3 (Input INTTC3) 111: fc/96	

Note 1: When operations are disabled by setting TXE and RXE bit to “0”, the setting becomes valid when data transmit or receive complete. When the transmit data is stored in the transmit data buffer, the data are not transmitted. Even if data transmit is enabled, until new data are written to the transmit data buffer, the current data are not transmitted.

Note 2: The transmit clock and the parity are common to transmit and receive.

Note 3: UART1CR1<RXE> and UART1CR1<TXE> should be set to “0” before UART1CR1<BRG> is changed.

UART1 Control Register2

UART1CR2 (0F96H)

7	6	5	4	3	2	1	0
					RXDNC	STOPBR	

(Initial value: **** *000)

RXDNC	Selection of RXD input noise rejection time	00: No noise rejection (Hysteresis input) 01: Rejects pulses shorter than 31/fc [s] as noise 10: Rejects pulses shorter than 63/fc [s] as noise 11: Rejects pulses shorter than 127/fc [s] as noise	Write only
STOPBR	Receive stop bit length	0: 1 bit 1: 2 bits	

Note: When UART1CR2<RXDNC> = “01”, pulses longer than 96/fc [s] are always regarded as signals; when UART1CR2<RXDNC> = “10”, longer than 192/fc [s]; and when UART1CR2<RXDNC> = “11”, longer than 384/fc [s].

UART1 Status Register

UART1SR (0F95H)

7	6	5	4	3	2	1	0
PERR	FERR	OERR	RBFL	TEND	TBEP		

(Initial value: 0000 11**)

PERR	Parity error flag	0: No parity error 1: Parity error	Read only
FERR	Framing error flag	0: No framing error 1: Framing error	
OERR	Overrun error flag	0: No overrun error 1: Overrun error	
RBFL	Receive data buffer full flag	0: Receive data buffer empty 1: Receive data buffer full	
TEND	Transmit end flag	0: On transmitting 1: Transmit end	
TBEP	Transmit data buffer empty flag	0: Transmit data buffer full (Transmit data writing is finished) 1: Transmit data buffer empty	

Note: When an INTTXD is generated, TBEP flag is set to "1" automatically.

UART1 Receive Data Buffer

RD1BUF (0F97H)

7	6	5	4	3	2	1	0

Read only

(Initial value: 0000 0000)

UART1 Transmit Data Buffer

TD1BUF (0F97H)

7	6	5	4	3	2	1	0

Write only

(Initial value: 0000 0000)

12.3 Transfer Data Format

In UART1, an one-bit start bit (Low level), stop bit (Bit length selectable at high level, by UART1CR1<STBT>), and parity (Select parity in UART1CR1<PE>; even- or odd-numbered parity by UART1CR1<EVEN>) are added to the transfer data. The transfer data formats are shown as follows.

PE	STBT	Frame Length: 1 2 3 ... 8 9 10 11 12
0	0	Start Bit 0 Bit 1 - - - - Bit 6 Bit 7 Stop 1
0	1	Start Bit 0 Bit 1 - - - - Bit 6 Bit 7 Stop 1 Stop 2
1	0	Start Bit 0 Bit 1 - - - - Bit 6 Bit 7 Parity Stop 1
1	1	Start Bit 0 Bit 1 - - - - Bit 6 Bit 7 Parity Stop 1 Stop 2

Figure 12-2 Transfer Data Format

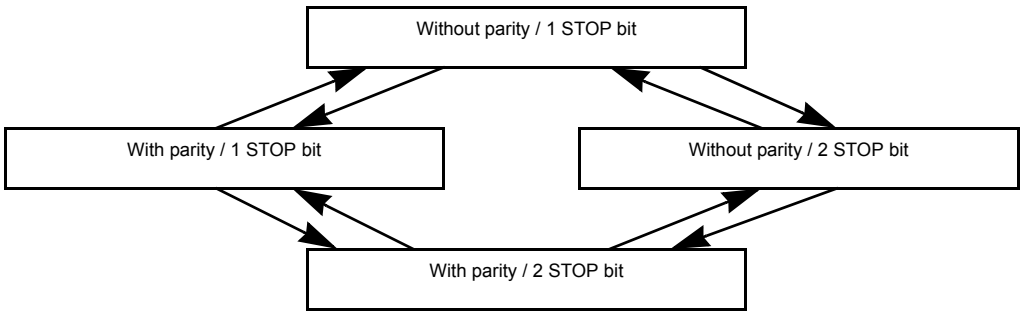


Figure 12-3 Caution on Changing Transfer Data Format

Note: In order to switch the transfer data format, perform transmit operations in the above Figure 12-3 sequence except for the initial setting.

12.4 Transfer Rate

The baud rate of UART1 is set of UART1CR1<BRG>. The example of the baud rate are shown as follows.

Table 12-1 Transfer Rate (Example)

BRG	Source Clock		
	16 MHz	8 MHz	4 MHz
000	76800 [baud]	38400 [baud]	19200 [baud]
001	38400	19200	9600
010	19200	9600	4800
011	9600	4800	2400
100	4800	2400	1200
101	2400	1200	600

When TC3 is used as the UART1 transfer rate (when UART1CR1<BRG> = “110”), the transfer clock and transfer rate are determined as follows:

Transfer clock [Hz] = TC3 source clock [Hz] / TTREG3 setting value

Transfer Rate [baud] = Transfer clock [Hz] / 16

12.5 Data Sampling Method

The UART1 receiver keeps sampling input using the clock selected by UART1CR1<BRG> until a start bit is detected in RXD1 pin input. RT clock starts detecting “L” level of the RXD1 pin. Once a start bit is detected, the start bit, data bits, stop bit(s), and parity bit are sampled at three times of RT7, RT8, and RT9 during one receiver clock interval (RT clock). (RT0 is the position where the bit supposedly starts.) Bit is determined according to majority rule (The data are the same twice or more out of three samplings).

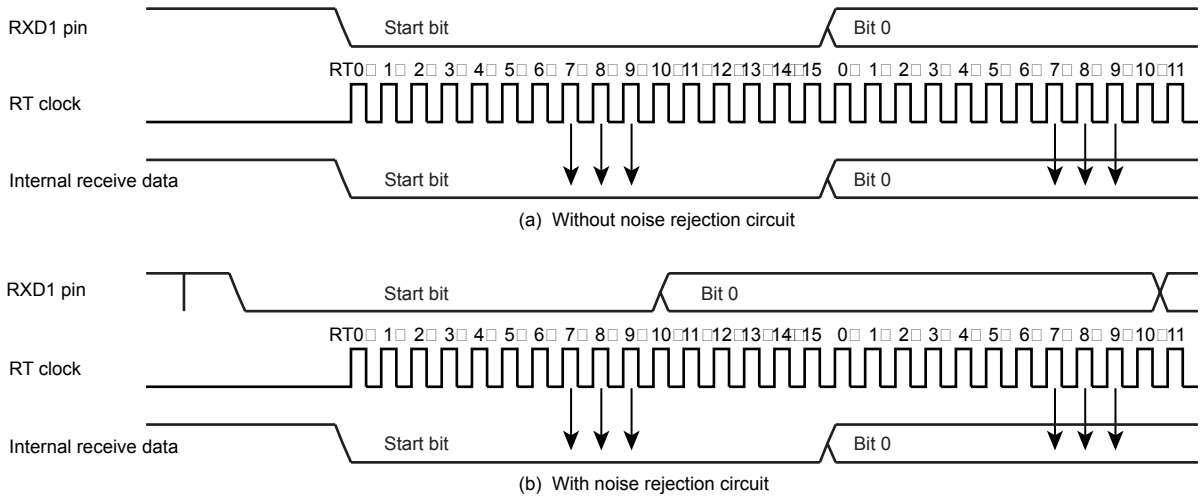

RXD1 pin
Start bit
Bit 0
RT0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11
RT clock
Internal receive data
Start bit
Bit 0
(a) Without noise rejection circuit
RXD1 pin
Start bit
Bit 0
RT0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11
RT clock
Internal receive data
Start bit
Bit 0
(b) With noise rejection circuit

Figure 12-4 Data Sampling Method

12.6 STOP Bit Length

Select a transmit stop bit length (1 bit or 2 bits) by UART1CR1<STBT>.

12.7 Parity

Set parity / no parity by UART1CR1<PE> and set parity type (Odd- or Even-numbered) by UART1CR1<EVEN>.

12.8 Transmit/Receive Operation

12.8.1 Data Transmit Operation

Set UART1CR1<TXE> to "1". Read UART1SR to check UART1SR<TBEP> = "1", then write data in TD1BUF (Transmit data buffer). Writing data in TD1BUF zero-clears UART1SR<TBEP>, transfers the data to the transmit shift register and the data are sequentially output from the TXD1 pin. The data output include a one-bit start bit, stop bits whose number is specified in UART1CR1<STBT> and a parity bit if parity addition is specified. Select the data transfer baud rate using UART1CR1<BRG>. When data transmit starts, transmit buffer empty flag UART1SR<TBEP> is set to "1" and an INTTXD1 interrupt is generated.

While UART1CR1<TXE> = "0" and from when "1" is written to UART1CR1<TXE> to when send data are written to TD1BUF, the TXD1 pin is fixed at high level.
When transmitting data, first read UART1SR, then write data in TD1BUF. Otherwise, UART1SR<TBEP> is not zero-cleared and transmit does not start.

12.8.2 Data Receive Operation

Set UART1CR1<RXE> to "1". When data are received via the RXD1 pin, the receive data are transferred to RD1BUF (Receive data buffer). At this time, the data transmitted includes a start bit and stop bit(s) and a parity bit if parity addition is specified. When stop bit(s) are received, data only are extracted and transferred to RD1BUF (Receive data buffer). Then the receive buffer full flag UART1SR<RBFL> is set and an INTRXD1 interrupt is generated. Select the data transfer baud rate using UART1CR1<BRG>.

If an overrun error (OERR) occurs when data are received, the data are not transferred to RD1BUF (Receive data buffer) but discarded; data in the RD1BUF are not affected.

Note: When a receive operation is disabled by setting UART1CR1<RXE> bit to "0", the setting becomes valid when data receive is completed. However, if a framing error occurs in data receive, the receive-disabling setting may not become valid. If a framing error occurs, be sure to perform a re-receive operation.

12.9 Status Flag

12.9.1 Parity Error

When parity determined using the receive data bits differs from the received parity bit, the parity error flag UART1SR<PERR> is set to “1”. The UART1SR<PERR> is cleared to “0” when the RD1BUF is read after reading the UART1SR.

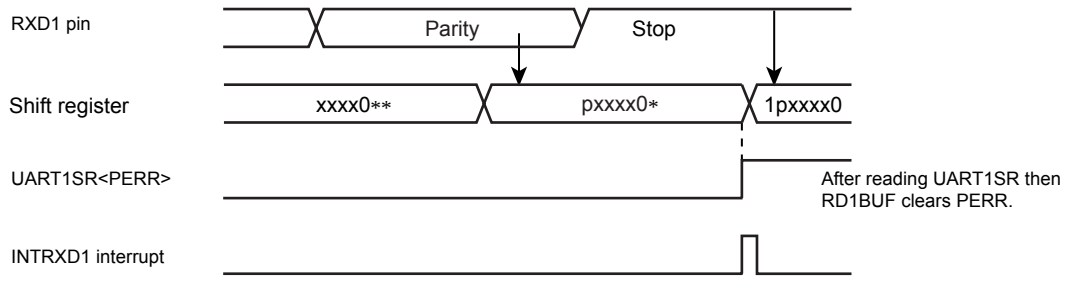


Figure 12-5 Generation of Parity Error

12.9.2 Framing Error

When “0” is sampled as the stop bit in the receive data, framing error flag UART1SR<FERR> is set to “1”. The UART1SR<FERR> is cleared to “0” when the RD1BUF is read after reading the UART1SR.

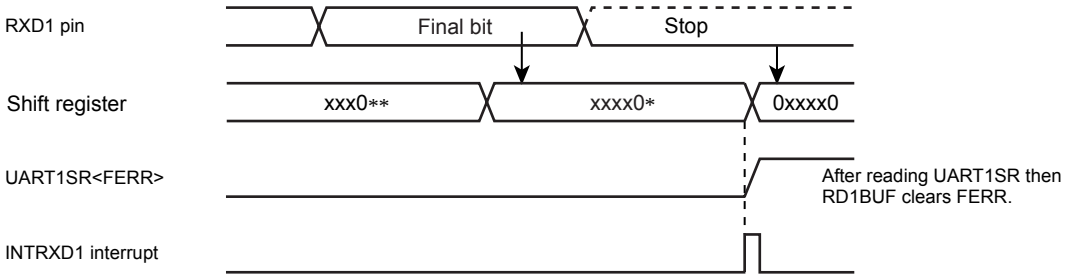


Figure 12-6 Generation of Framing Error

12.9.3 Overrun Error

When all bits in the next data are received while unread data are still in RD1BUF, overrun error flag UART1SR<OERR> is set to “1”. In this case, the receive data is discarded; data in RD1BUF are not affected. The UART1SR<OERR> is cleared to “0” when the RD1BUF is read after reading the UART1SR.

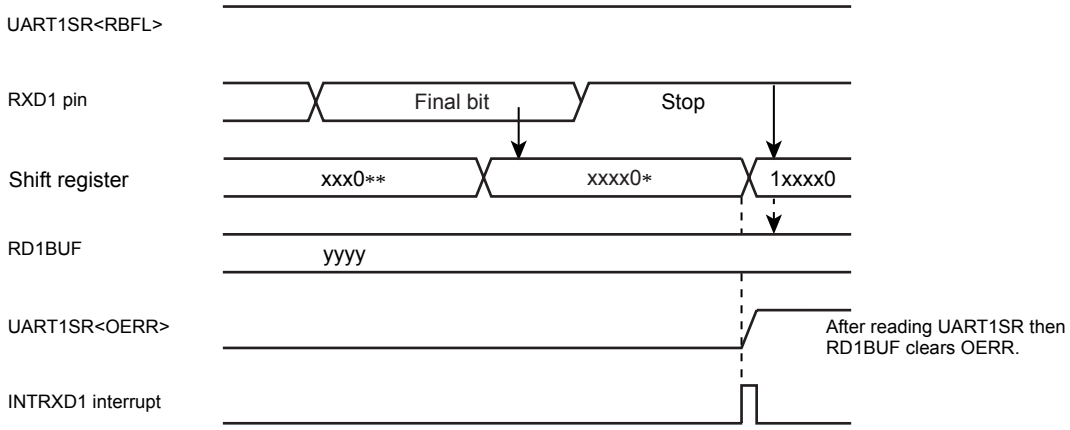


Figure 12-7 Generation of Overrun Error

Note: Receive operations are disabled until the overrun error flag UART1SR<OERR> is cleared.

12.9.4 Receive Data Buffer Full

Loading the received data in RD1BUF sets receive data buffer full flag UART1SR<RBFL> to "1". The UART1SR<RBFL> is cleared to “0” when the RD1BUF is read after reading the UART1SR.

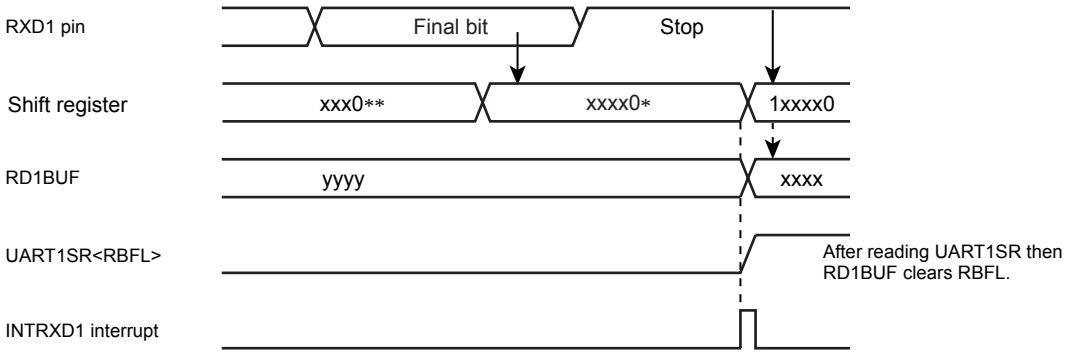


Figure 12-8 Generation of Receive Data Buffer Full

Note: If the overrun error flag UART1SR<OERR> is set during the period between reading the UART1SR and reading the RD1BUF, it cannot be cleared by only reading the RD1BUF. Therefore, after reading the RD1BUF, read the UART1SR again to check whether or not the overrun error flag which should have been cleared still remains set.

12.9.5 Transmit Data Buffer Empty

When no data is in the transmit buffer TD1BUF, that is, when data in TD1BUF are transferred to the transmit shift register and data transmit starts, transmit data buffer empty flag UART1SR<TBEP> is set to “1”. The UART1SR<TBEP> is cleared to “0” when the TD1BUF is written after reading the UART1SR.

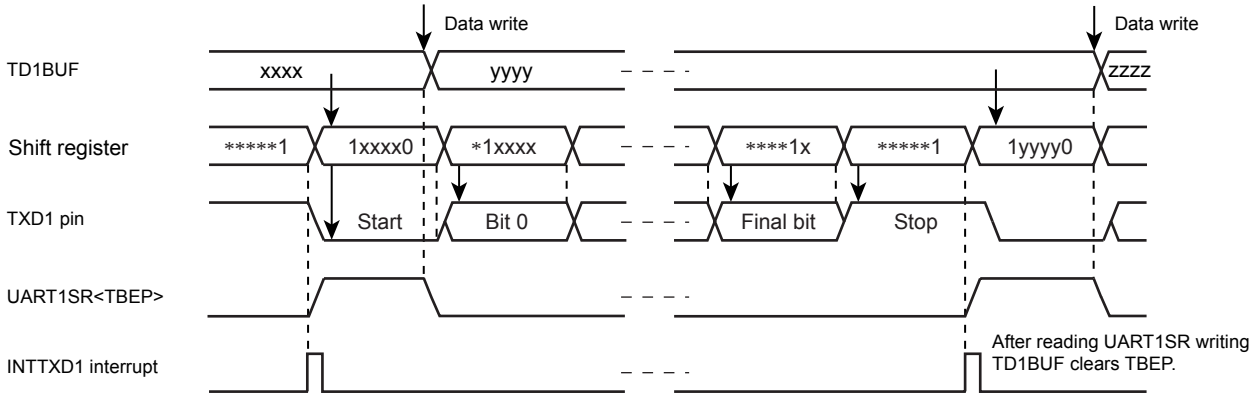


Figure 12-9 Generation of Transmit Data Buffer Empty

12.9.6 Transmit End Flag

When data are transmitted and no data is in TD1BUF (UART1SR<TBEP> = "1"), transmit end flag UART1SR<TEND> is set to "1". The UART1SR<TEND> is cleared to "0" when the data transmit is started after writing the TD1BUF.

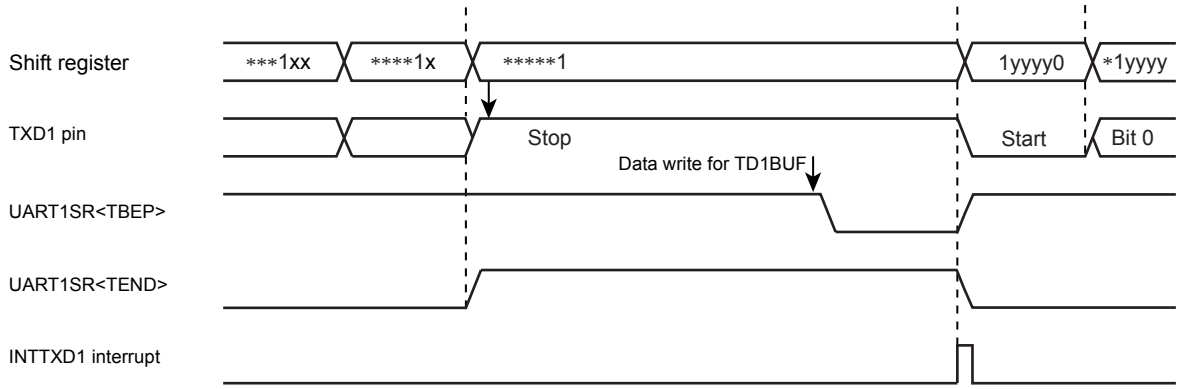


Figure 12-10 Generation of Transmit End Flag and Transmit Data Buffer Empty

13. Asynchronous Serial interface (UART2)

13.1 Configuration

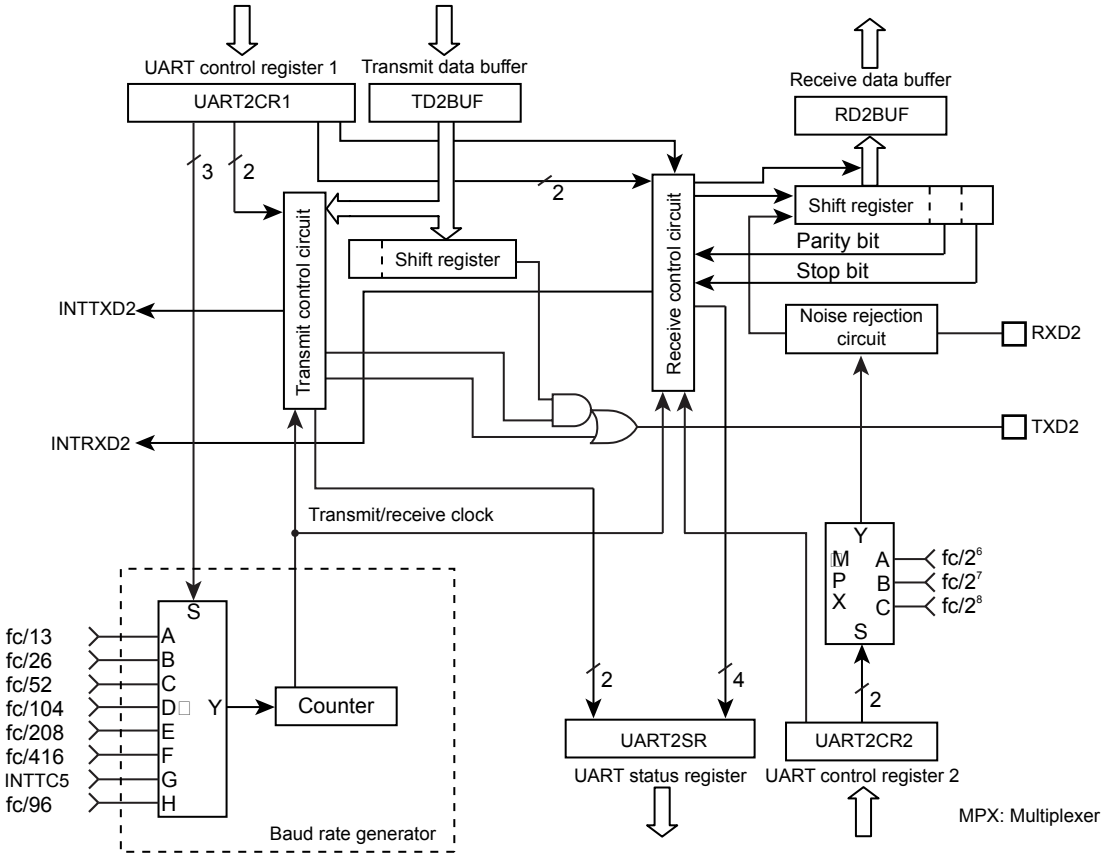


Figure 13-1 UART2 (Asynchronous Serial Interface)

13.2 Control

UART2 is controlled by the UART2 Control Registers (UART2CR1, UART2CR2). The operating status can be monitored using the UART status register (UART2SR).

UART2 Control Register1

UART2CR1 (0F98H)

7	6	5	4	3	2	1	0
TXE	RXE	STBT	EVEN	PE	BRG		

(Initial value: 0000 0000)

TXE	Transfer operation	0: Disable 1: Enable	Write only
RXE	Receive operation	0: Disable 1: Enable	
STBT	Transmit stop bit length	0: 1 bit 1: 2 bits	
EVEN	Even-numbered parity	0: Odd-numbered parity 1: Even-numbered parity	
PE	Parity addition	0: No parity 1: Parity	
BRG	Transmit clock select	000: fc/13 [Hz] 001: fc/26 010: fc/52 011: fc/104 100: fc/208 101: fc/416 110: TC5 (Input INTTC5) 111: fc/96	

Note 1: When operations are disabled by setting TXE and RXE bit to “0”, the setting becomes valid when data transmit or receive complete. When the transmit data is stored in the transmit data buffer, the data are not transmitted. Even if data transmit is enabled, until new data are written to the transmit data buffer, the current data are not transmitted.

Note 2: The transmit clock and the parity are common to transmit and receive.

Note 3: UART2CR1<RXE> and UART2CR1<TXE> should be set to “0” before UART2CR1<BRG> is changed.

UART2 Control Register2

UART2CR2 (0F99H)

7	6	5	4	3	2	1	0
					RXDNC	STOPBR	

(Initial value: **** *000)

RXDNC	Selection of RXD input noise rejection time	00: No noise rejection (Hysteresis input) 01: Rejects pulses shorter than 31/fc [s] as noise 10: Rejects pulses shorter than 63/fc [s] as noise 11: Rejects pulses shorter than 127/fc [s] as noise	Write only
STOPBR	Receive stop bit length	0: 1 bit 1: 2 bits	

Note: When UART2CR2<RXDNC> = “01”, pulses longer than 96/fc [s] are always regarded as signals; when UART2CR2<RXDNC> = “10”, longer than 192/fc [s]; and when UART2CR2<RXDNC> = “11”, longer than 384/fc [s].

UART2 Status Register

UART2SR (0F98H)

7	6	5	4	3	2	1	0
PERR	FERR	OERR	RBFL	TEND	TBEP		

(Initial value: 0000 11**)

PERR	Parity error flag	0: No parity error 1: Parity error	Read only
FERR	Framing error flag	0: No framing error 1: Framing error	
OERR	Overrun error flag	0: No overrun error 1: Overrun error	
RBFL	Receive data buffer full flag	0: Receive data buffer empty 1: Receive data buffer full	
TEND	Transmit end flag	0: On transmitting 1: Transmit end	
TBEP	Transmit data buffer empty flag	0: Transmit data buffer full (Transmit data writing is finished) 1: Transmit data buffer empty	

Note: When an INTTXD is generated, TBEP flag is set to "1" automatically.

UART2 Receive Data Buffer

RD2BUF (0F9AH)

7	6	5	4	3	2	1	0

Read only

(Initial value: 0000 0000)

UART2 Transmit Data Buffer

TD2BUF (0F9AH)

7	6	5	4	3	2	1	0

Write only

(Initial value: 0000 0000)

13.3 Transfer Data Format

In UART2, an one-bit start bit (Low level), stop bit (Bit length selectable at high level, by UART2CR1<STBT>), and parity (Select parity in UART2CR1<PE>; even- or odd-numbered parity by UART2CR1<EVEN>) are added to the transfer data. The transfer data formats are shown as follows.

PE	STBT	Frame Length: 1	2	3		8	9	10	11	12
0	0	Start	Bit 0	Bit 1	- - - -	Bit 6	Bit 7	Stop 1		
0	1	Start	Bit 0	Bit 1	- - - -	Bit 6	Bit 7	Stop 1	Stop 2	
1	0	Start	Bit 0	Bit 1	- - - -	Bit 6	Bit 7	Parity	Stop 1	
1	1	Start	Bit 0	Bit 1	- - - -	Bit 6	Bit 7	Parity	Stop 1	Stop 2

Figure 13-2 Transfer Data Format

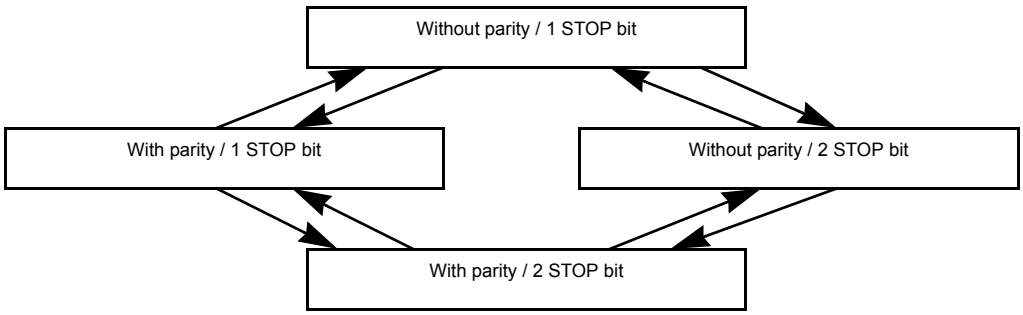


Figure 13-3 Caution on Changing Transfer Data Format

Note: In order to switch the transfer data format, perform transmit operations in the above Figure 13-3 sequence except for the initial setting.

13.4 Transfer Rate

The baud rate of UART2 is set of UART2CR1<BRG>. The example of the baud rate are shown as follows.

Table 13-1 Transfer Rate (Example)

BRG	Source Clock		
	16 MHz	8 MHz	4 MHz
000	76800 [baud]	38400 [baud]	19200 [baud]
001	38400	19200	9600
010	19200	9600	4800
011	9600	4800	2400
100	4800	2400	1200
101	2400	1200	600

When TC5 is used as the UART2 transfer rate (when UART2CR1<BRG> = “110”), the transfer clock and transfer rate are determined as follows:

Transfer clock [Hz] = TC5 source clock [Hz] / TTREG5 setting value

Transfer Rate [baud] = Transfer clock [Hz] / 16

13.5 Data Sampling Method

The UART2 receiver keeps sampling input using the clock selected by UART2CR1<BRG> until a start bit is detected in RXD2 pin input. RT clock starts detecting “L” level of the RXD2 pin. Once a start bit is detected, the start bit, data bits, stop bit(s), and parity bit are sampled at three times of RT7, RT8, and RT9 during one receiver clock interval (RT clock). (RT0 is the position where the bit supposedly starts.) Bit is determined according to majority rule (The data are the same twice or more out of three samplings).

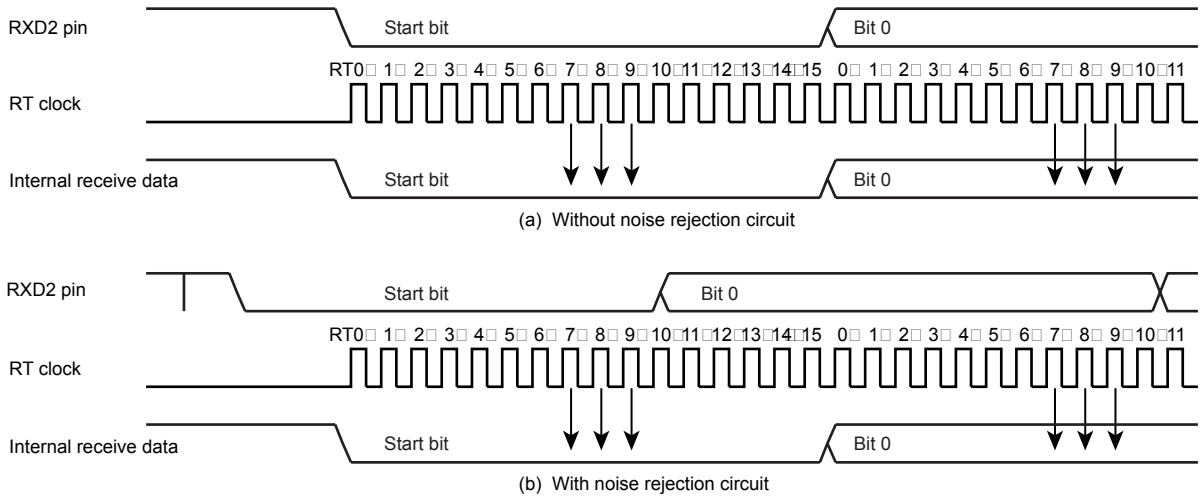

RXD2 pin
Start bit
Bit 0
RT0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11
RT clock
Internal receive data
Start bit
Bit 0
(a) Without noise rejection circuit
RXD2 pin
Start bit
Bit 0
RT0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11
RT clock
Internal receive data
Start bit
Bit 0
(b) With noise rejection circuit

Figure 13-4 Data Sampling Method

13.6 STOP Bit Length

Select a transmit stop bit length (1 bit or 2 bits) by UART2CR1<STBT>.

13.7 Parity

Set parity / no parity by UART2CR1<PE> and set parity type (Odd- or Even-numbered) by UART2CR1<EVEN>.

13.8 Transmit/Receive Operation

13.8.1 Data Transmit Operation

Set UART2CR1<TXE> to "1". Read UART2SR to check UART2SR<TBEP> = "1", then write data in TD2BUF (Transmit data buffer). Writing data in TD2BUF zero-clears UART2SR<TBEP>, transfers the data to the transmit shift register and the data are sequentially output from the TXD2 pin. The data output include a one-bit start bit, stop bits whose number is specified in UART2CR1<STBT> and a parity bit if parity addition is specified. Select the data transfer baud rate using UART2CR1<BRG>. When data transmit starts, transmit buffer empty flag UART2SR<TBEP> is set to "1" and an INTTXD2 interrupt is generated.

While UART2CR1<TXE> = "0" and from when "1" is written to UART2CR1<TXE> to when send data are written to TD2BUF, the TXD2 pin is fixed at high level.
When transmitting data, first read UART2SR, then write data in TD2BUF. Otherwise, UART2SR<TBEP> is not zero-cleared and transmit does not start.

13.8.2 Data Receive Operation

Set UART2CR1<RXE> to "1". When data are received via the RXD2 pin, the receive data are transferred to RD2BUF (Receive data buffer). At this time, the data transmitted includes a start bit and stop bit(s) and a parity bit if parity addition is specified. When stop bit(s) are received, data only are extracted and transferred to RD2BUF (Receive data buffer). Then the receive buffer full flag UART2SR<RBFL> is set and an INTRXD2 interrupt is generated. Select the data transfer baud rate using UART2CR1<BRG>.

If an overrun error (OERR) occurs when data are received, the data are not transferred to RD2BUF (Receive data buffer) but discarded; data in the RD2BUF are not affected.

Note: When a receive operation is disabled by setting UART2CR1<RXE> bit to "0", the setting becomes valid when data receive is completed. However, if a framing error occurs in data receive, the receive-disabling setting may not become valid. If a framing error occurs, be sure to perform a re-receive operation.

13.9 Status Flag

13.9.1 Parity Error

When parity determined using the receive data bits differs from the received parity bit, the parity error flag UART2SR<PERR> is set to “1”. The UART2SR<PERR> is cleared to “0” when the RD2BUF is read after reading the UART2SR.

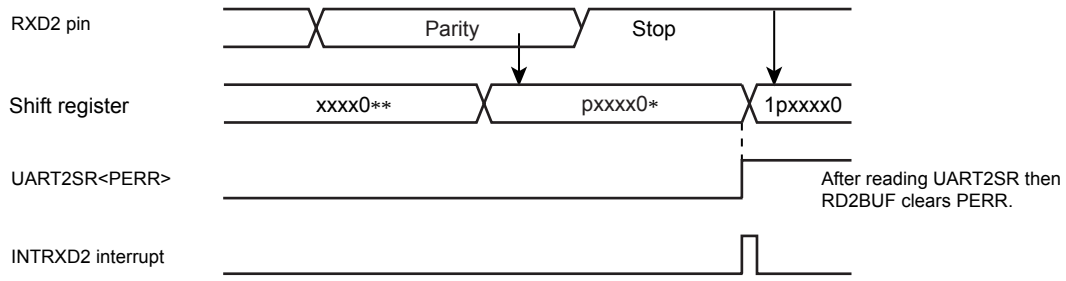


Figure 13-5 Generation of Parity Error

13.9.2 Framing Error

When “0” is sampled as the stop bit in the receive data, framing error flag UART2SR<FERR> is set to “1”. The UART2SR<FERR> is cleared to “0” when the RD2BUF is read after reading the UART2SR.

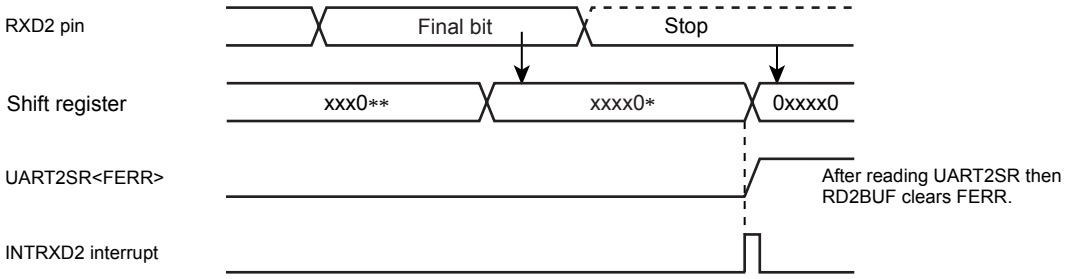


Figure 13-6 Generation of Framing Error

13.9.3 Overrun Error

When all bits in the next data are received while unread data are still in RD2BUF, overrun error flag UART2SR<OERR> is set to “1”. In this case, the receive data is discarded; data in RD2BUF are not affected. The UART2SR<OERR> is cleared to “0” when the RD2BUF is read after reading the UART2SR.

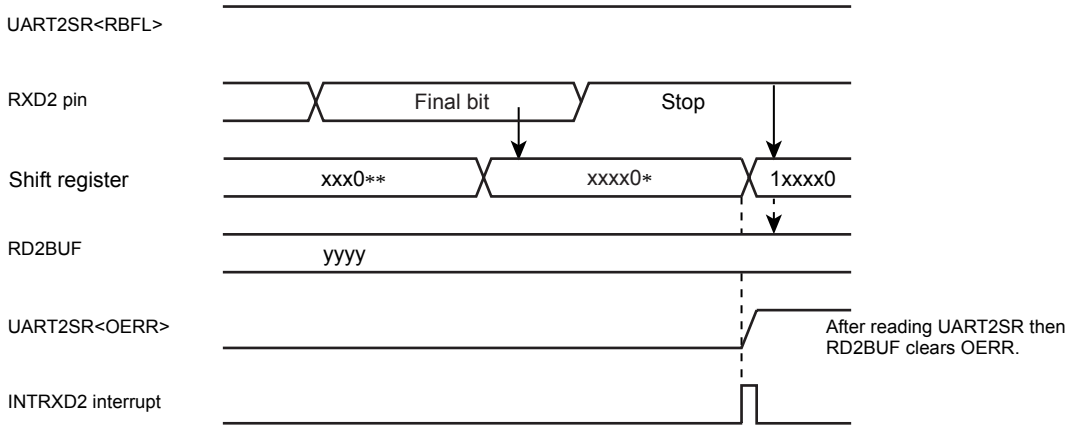


Figure 13-7 Generation of Overrun Error

Note: Receive operations are disabled until the overrun error flag UART2SR<OERR> is cleared.

13.9.4 Receive Data Buffer Full

Loading the received data in RD2BUF sets receive data buffer full flag UART2SR<RBFL> to "1". The UART2SR<RBFL> is cleared to “0” when the RD2BUF is read after reading the UART2SR.

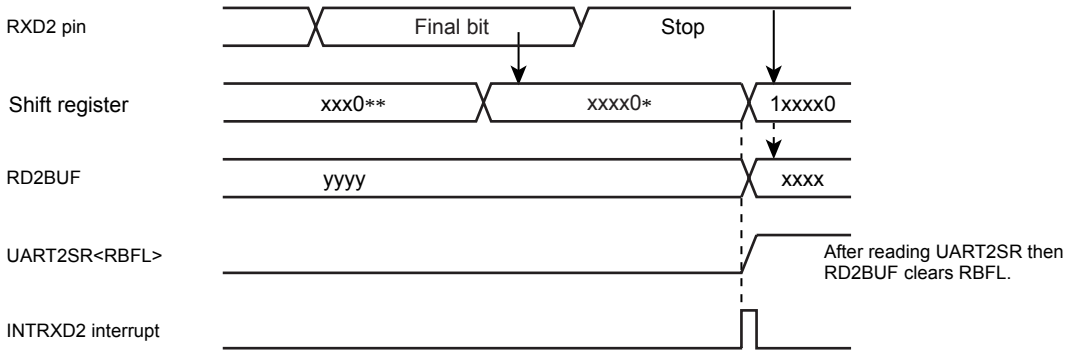


Figure 13-8 Generation of Receive Data Buffer Full

Note: If the overrun error flag UART2SR<OERR> is set during the period between reading the UART2SR and reading the RD2BUF, it cannot be cleared by only reading the RD2BUF. Therefore, after reading the RD2BUF, read the UART2SR again to check whether or not the overrun error flag which should have been cleared still remains set.

13.9.5 Transmit Data Buffer Empty

When no data is in the transmit buffer TD2BUF, that is, when data in TD2BUF are transferred to the transmit shift register and data transmit starts, transmit data buffer empty flag UART2SR<TBEP> is set to “1”. The UART2SR<TBEP> is cleared to “0” when the TD2BUF is written after reading the UART2SR.

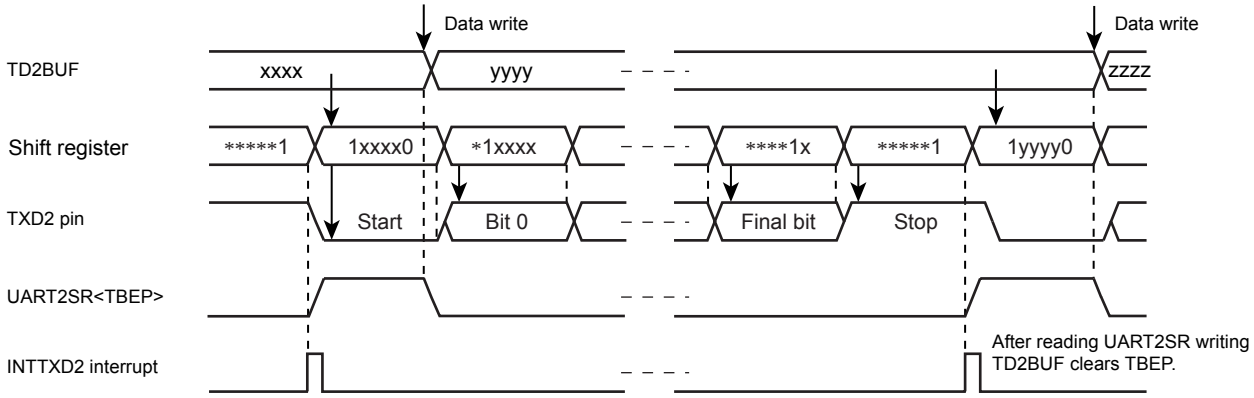


Figure 13-9 Generation of Transmit Data Buffer Empty

13.9.6 Transmit End Flag

When data are transmitted and no data is in TD2BUF (UART2SR<TBEP> = "1"), transmit end flag UART2SR<TEND> is set to "1". The UART2SR<TEND> is cleared to "0" when the data transmit is started after writing the TD2BUF.

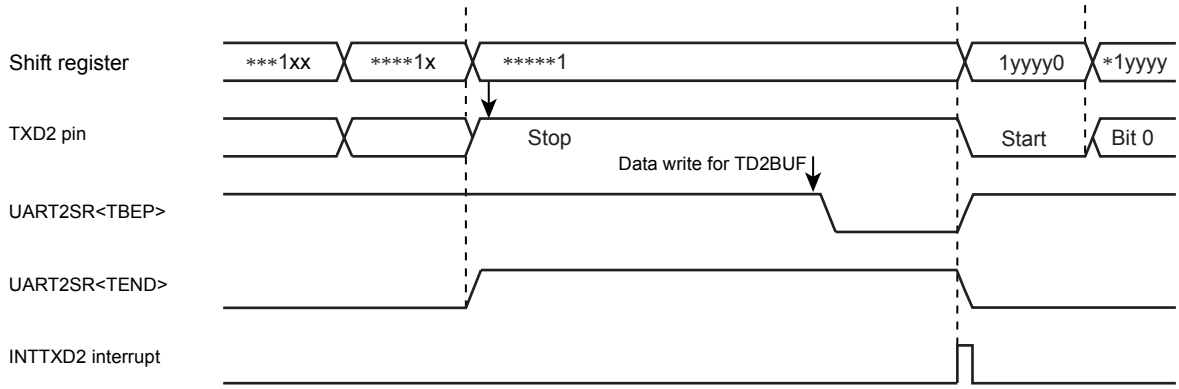


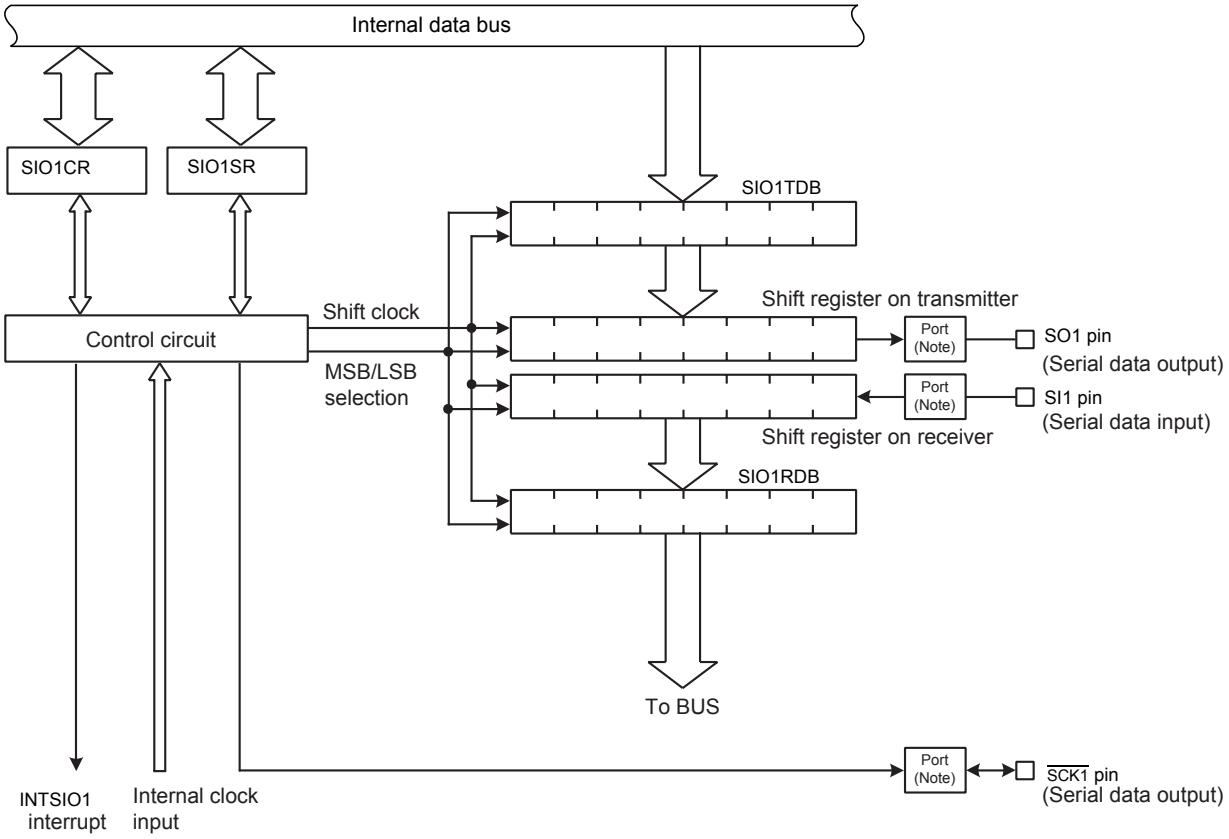
Figure 13-10 Generation of Transmit End Flag and Transmit Data Buffer Empty

14. Synchronous Serial Interface (SIO1)

The serial interfaces connect to an external device via SI1, SO1, and $\overline{SCK1}$ pins.

When these pins are used as serial interface, the output latches for each port should be set to "1".

14.1 Configuration



Note: Set the register of port correctly for the port assigned as serial interface pins.
For details, see the description of the input/output port control register.

Figure 14-1 Synchronous Serial Interface (SIO)

14.2 Control

The SIO is controlled using the serial interface control register (SIO1CR). The operating status of the serial interface can be inspected by reading the status register (SIO1CR).

Serial Interface Control Register

SIO1CR (0020H)

7	6	5	4	3	2	1	0
SIOS	SIOINH	SIOM		SIODIR	SCK		

(Initial value: 0000 0000)

SIOS	Specify start/stop of transfer	0: Stop 1: Start			R/W
SIOINH	Forcibly stops transfer (Note 1)	0: – 1: Forcibly stop (Automatically cleared to "0" after stopping)			
SIOM	Selects transfer mode	00: Transmit mode 01: Receive mode 10: Transmit/receive mode 11: Reserved			
SIODIR	Selects direction of transfer	0: MSB (Transfer beginning with bit7) 1: LSB (Transfer beginning with bit0)			
SCK	Selects serial clock		NORMAL1/2 or IDLE1/2 modes		SLOW/SLEEP mode
			TBTCR <DV7CK> = "0"	TBTCR <DV7CK> = "1"	
		000	$fc/2^{12}$	$fs/2^4$	$fs/2^4$
		001	$fc/2^8$	$fc/2^8$	Reserved
		010	$fc/2^7$	$fc/2^7$	Reserved
		011	$fc/2^6$	$fc/2^6$	Reserved
		100	$fc/2^5$	$fc/2^5$	Reserved
		101	$fc/2^4$	$fc/2^4$	Reserved
		110	$fc/2^3$	$fc/2^3$	Reserved
		111	External clock (Input from $\overline{SCK1}$ pin)		

Note 1: When SIO1CR<SIOINH> is set to “1”, SIO1CR<SIOS>, SIO1SR register, SIO1RDB register and SIO1TDB register are initialized.

Note 2: Transfer mode, direction of transfer and serial clock must be select during the transfer is stopping (when SIO1SR<SIOF> "0").

Note 3: fc: High-frequency clock [Hz], fs: Low-frequency clock [Hz], *: Don’t care

Serial Interface Status Register

SIO1SR (0021H)

7	6	5	4	3	2	1	0
SIOF	SEF	TXF	RXF	TXERR	RXERR		

(Initial value: 0010 00**)

SIOF	Serial transfer operation status monitor	0: Transfer finished 1: Transfer in progress	Read only
SEF	Number of clocks monitor	0: 8 clocks 1: 1 to 7 clocks	
TXF	Transmit buffer empty flag	0: Data exists in transmit buffer 1: No data exists in transmit buffer	
RXF	Receive buffer full flag	0: No data exists in receive buffer 1: Data exists in receive buffer	
TXERR	Transfer operation error flag	Read 0: – (No error exist) 1: Transmit buffer under run occurs in an external clock mode Write 0: Clear the flag 1: – (A write of "1" to this bit is ignored)	R/W
RXERR	Receive operation error flag	Read 0: – (No error exist) 1: Receive buffer over run occurs in an external clock mode Write 0: Clear the flag 1: – (A write of "1" to this bit is ignored)	

Note 1: The operation error flag (TXERR and RXERR) are not automatically cleared by stopping transfer with SIO1CR<SIOS> "0". Therefore, set these bits to "0" for clearing these error flag. Or set SIO1CR<SIOINH> to "1".

Note 2: *: Don't care

Receive buffer register

SIO1RDB (0022H)

7	6	5	4	3	2	1	0

Read only

(Initial value: 0000 0000)

Transmit buffer register

SIO1TDB (0022H)

7	6	5	4	3	2	1	0

Write only

(Initial value: **** ****)

Note 1: SIO1TDB is write only register. A bit manipulation should not be performed on the transmit buffer register using a read-modify-write instruction.

Note 2: The SIO1TDB should be written after checking SIO1SR<TXF> "1". When SIO1SR<TXF> is "0", the writing data can't be transferred to SIO1TDB even if write instruction is executed to SIO1TDB

Note 3: *: Don't care

14.3 Function

14.3.1 Serial clock

14.3.1.1 Clock source

The serial clock can be selected by using SIO1CR<SCK>. When the serial clock is changed, the writing instruction to SIO1CR<SCK> should be executed while the transfer is stopped (when SIO1SR<SIOF> "0")

(1) Internal clock

Setting the SIO1CR<SCK> to other than "111B" outputs the clock (shown in " Table 14-1 Serial Clock Rate (fc = 16 MHz, fs = 32.768kHz) ") as serial clock outputs from $\overline{SCK1}$ pin. At the before beginning or finishing of a transfer, $\overline{SCK1}$ pin is kept in high level.

When writing (in the transmit mode) or reading (in the receive mode) data can not follow the serial clock rate, an automatic-wait function is executed to stop the serial clock automatically and hold the next shift operation until reading or writing is completed (shown in " Figure 14-2 Automatic-wait Function (Example of transmit mode) "). The maximum time from releasing the automatic-wait function by reading or writing a data is 1 cycle of the selected serial clock until the serial clock comes out from $\overline{SCK1}$ pin.

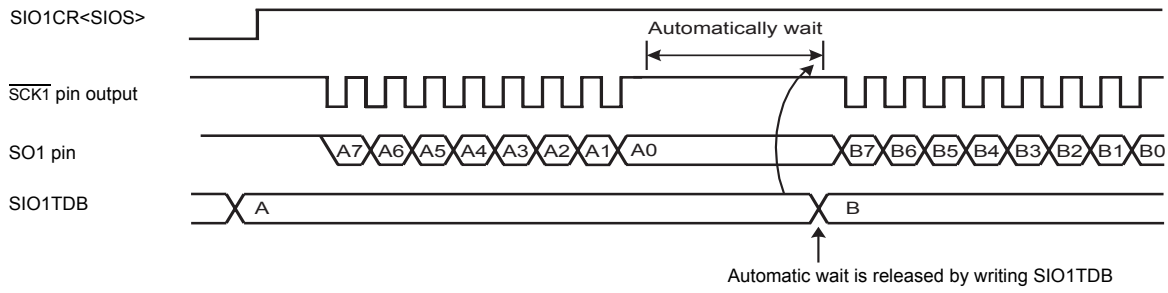


Figure 14-2 Automatic-wait Function (Example of transmit mode)

Table 14-1 Serial Clock Rate (fc = 16 MHz, fs = 32.768kHz)

	NORMAL1/2, IDLE1/2 Mode				SLOW1/2, SLEEP1/2 Mode	
	TBTCR<DV7CK> = "0"		TBTCR<DV7CK> = "1"		Serial Clock	Baud Rate
SCK	Serial Clock	Baud Rate	Serial Clock	Baud Rate		
000	$fc/2^{12}$	3.906 kbps	$fs/2^{4}$	2048 bps	$fs/2^{4}$	2048 bps
001	$fc/2^{8}$	62.5 kbps	$fc/2^{8}$	62.5 kbps	Reserved	–
010	$fc/2^{7}$	125 kbps	$fc/2^{7}$	125 kbps	Reserved	–
011	$fc/2^{6}$	250 kbps	$fc/2^{6}$	250 kbps	Reserved	–
100	$fc/2^{5}$	500 kbps	$fc/2^{5}$	500 kbps	Reserved	–
101	$fc/2^{4}$	1.00 Mbps	$fc/2^{4}$	1.00 Mbps	Reserved	–
110	$fc/2^{3}$	2.00 Mbps	$fc/2^{3}$	2.00 Mbps	Reserved	

(2) External clock

When an external clock is selected by setting SIO1CR<SCK> to "111B", the clock via the $\overline{SCK1}$ pin from an external source is used as the serial clock.

To ensure shift operation, the serial clock pulse width must be 4/fc or more for both "H" and "L" levels.

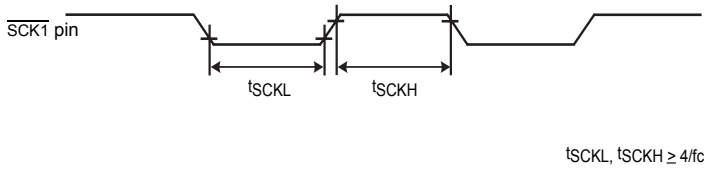


Figure 14-3 External Clock

14.3.1.2 Shift edge

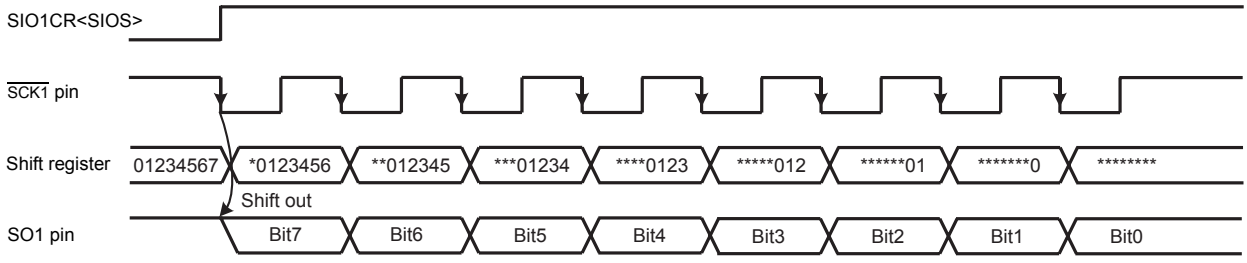
The leading edge is used to transmit data, and the trailing edge is used to receive data.

(1) Leading edge shift

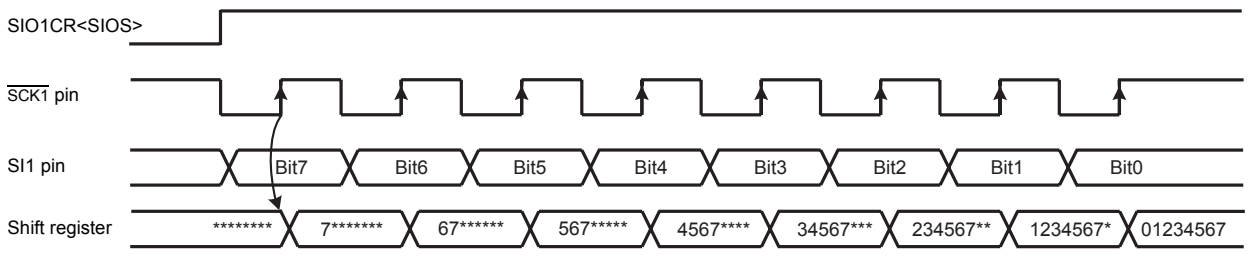
Data is shifted on the leading edge of the serial clock (falling edge of the $\overline{SCK1}$ pin input/output).

(2) Trailing edge shift

Data is shifted on the trailing edge of the serial clock (rising edge of the $\overline{SCK1}$ pin input/output).



(a) Leading edge shift (Example of MSB transfer)



(b) Trailing edge shift (Example of MSB transfer)

Figure 14-4 Shift Edge

14.3.2 Transfer bit direction

Transfer data direction can be selected by using SIO1CR<SIODIR>. The transfer data direction can't be set individually for transmit and receive operations.

When the data direction is changed, the writing instruction to SIO1CR<SIODIR> should be executed while the transfer is stopped (when SIO1CR<SIOF>= “0”)

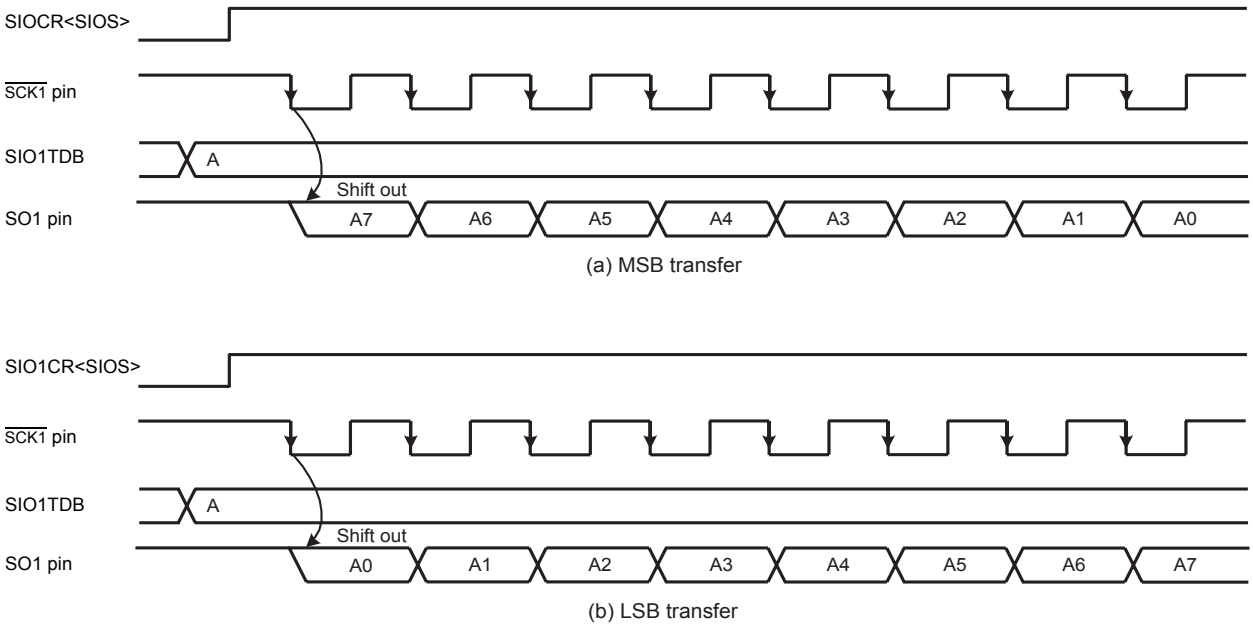


Figure 14-5 Transfer Bit Direction (Example of transmit mode)

14.3.2.1 Transmit mode

(1) MSB transmit mode

MSB transmit mode is selected by setting SIO1CR<SIODIR> to “0”, in which case the data is transferred sequentially beginning with the most significant bit (Bit7).

(2) LSB transmit mode

LSB transmit mode is selected by setting SIO1CR<SIODIR> to “1”, in which case the data is transferred sequentially beginning with the least significant bit (Bit0).

14.3.2.2 Receive mode

(1) MSB receive mode

MSB receive mode is selected by setting SIO1CR<SIODIR> to “0”, in which case the data is received sequentially beginning with the most significant bit (Bit7).

(2) LSB receive mode

LSB receive mode is selected by setting SIO1CR<SIODIR> to “1”, in which case the data is received sequentially beginning with the least significant bit (Bit0).

14.3.2.3 Transmit/receive mode

(1) MSB transmit/receive mode

MSB transmit/receive mode are selected by setting SIO1CR<SIODIR> to “0” in which case the data is transferred sequentially beginning with the most significant bit (Bit7) and the data is received sequentially beginning with the most significant (Bit7).

(2) LSB transmit/receive mode

LSB transmit/receive mode are selected by setting SIO1CR<SIODIR> to “1”, in which case the data is transferred sequentially beginning with the least significant bit (Bit0) and the data is received sequentially beginning with the least significant (Bit0).

14.3.3 Transfer modes

Transmit, receive and transmit/receive mode are selected by using SIO1CR<SIOM>.

14.3.3.1 Transmit mode

Transmit mode is selected by writing “00B” to SIO1CR<SIOM>.

(1) Starting the transmit operation

Transmit mode is selected by setting “00B” to SIO1CR<SIOM>. Serial clock is selected by using SIO1CR<SCK>. Transfer direction is selected by using SIO1CR<SIODIR>.

When a transmit data is written to the transmit buffer register (SIO1TDB), SIO1SR<TXF> is cleared to “0”.

After SIO1CR<SIOS> is set to “1”, SIO1SR<SIOF> is set synchronously to “1” the falling edge of $\overline{\text{SCK1}}$ pin.

The data is transferred sequentially starting from SO1 pin with the direction of the bit specified by SIO1CR<SIODIR>, synchronizing with the $\overline{\text{SCK1}}$ pin's falling edge.

SIO1SR<SEF> is kept in high level, between the first clock falling edge of $\overline{\text{SCK1}}$ pin and eighth clock falling edge.

SIO1SR<TXF> is set to “1” at the rising edge of pin after the data written to the SIO1TDB is transferred to shift register, then the INTSIO1 interrupt request is generated, synchronizing with the next falling edge on $\overline{\text{SCK1}}$ pin.

Note 1: In internal clock operation, when SIO1CR<SIOS> is set to "1", transfer mode does not start without writing a transmit data to the transmit buffer register (SIO1TDB).

Note 2: In internal clock operation, when the SIO1CR<SIOS> is set to "1", SIO1TDB is transferred to shift register after maximum 1-cycle of serial clock frequency, then a serial clock is output from $\overline{\text{SCK1}}$ pin.

Note 3: In external clock operation, when the falling edge is input from $\overline{\text{SCK1}}$ pin after SIO1CR<SIOS> is set to "1", SIO1TDB is transferred to shift register immediately.

(2) During the transmit operation

When data is written to SIO1TDB, SIO1SR<TXF> is cleared to “0”.

In internal clock operation, in case a next transmit data is not written to SIO1TDB, the serial clock stops to “H” level by an automatic-wait function when all of the bit set in the SIO1TDB has been transmitted. Automatic-wait function is released by writing a transmit data to SIO1TDB. Then, transmit operation is restarted after maximum 1-cycle of serial clock.

When the next data is written to the SIO1TDB before termination of previous 8-bit data with SIO1SR<TXF> “1”, the next data is continuously transferred after transmission of previous data.

In external clock operation, after SIO1SR<TXF> is set to “1”, the transmit data must be written to SIO1TDB before the shift operation of the next data begins.

If the transmit data is not written to SIO1TDB, transmit error occurs immediately after shift operation is started. Then, INTSIO1 interrupt request is generated after SIO1SR<TXERR> is set to “1”.

(3) Stopping the transmit operation

There are two ways for stopping transmits operation.

- The way of clearing SIO1CR<SIOS>.
  When SIO1CR<SIOS> is cleared to “0”, transmit operation is stopped after all transfer of the data is finished. When transmit operation is finished, SIO1SR<SIOF> is cleared to “0” and SO1 pin is kept in high level.
  In external clock operation, SIO1CR<SIOS> must be cleared to “0” before SIO1SR<SEF> is set to “1” by beginning next transfer.
- The way of setting SIO1CR<SIOINH>.
  Transmit operation is stopped immediately after SIO1CR<SIOINH> is set to “1”. In this case, SIO1CR<SIOS>, SIO1SR register, SIO1RDB register and SIO1TDB register are initialized.

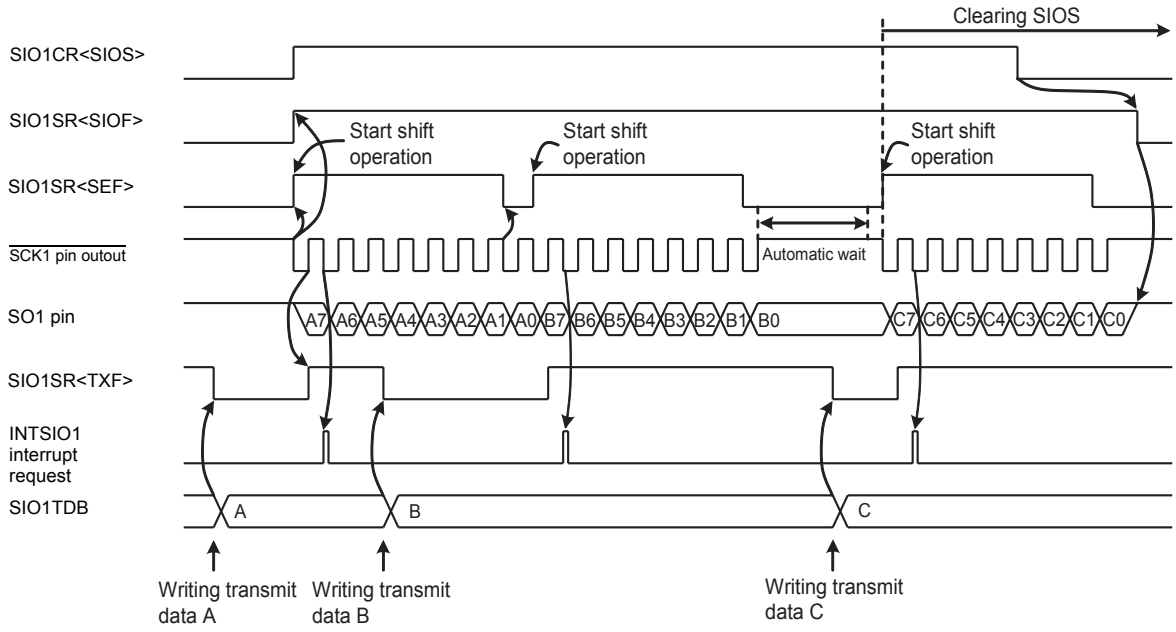


Figure 14-6 Example of Internal Clock and MSB Transmit Mode

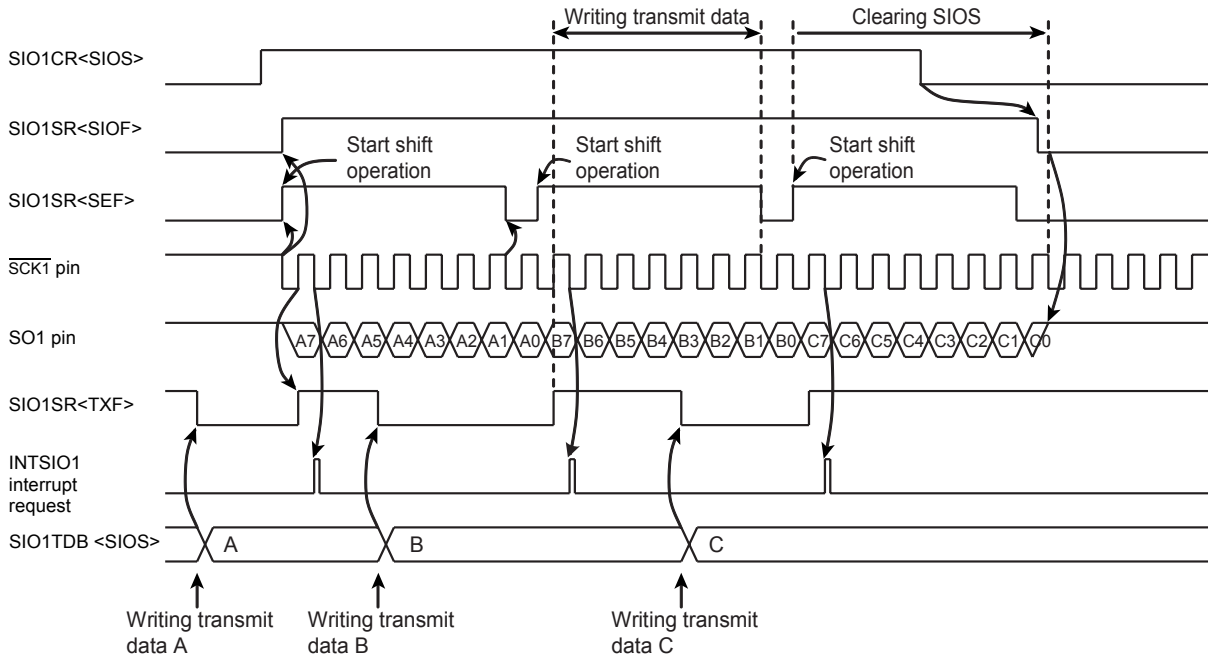


Figure 14-7 Exaple of External Clock and MSB Transmit Mode

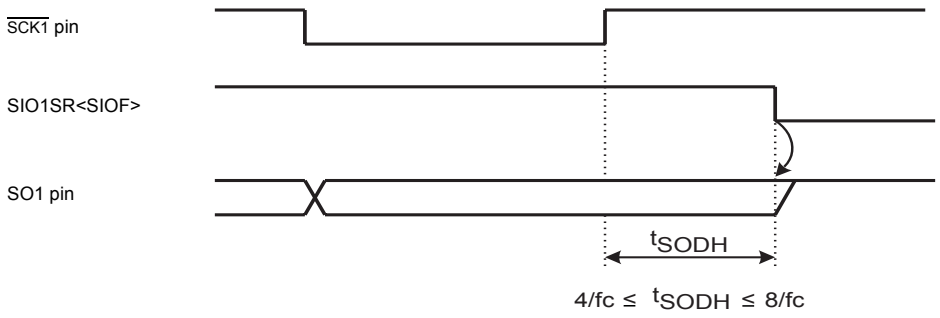


Figure 14-8 Hold Time of the End of Transmit Mode

(4) Transmit error processing

Transmit errors occur on the following situation.

- Shift operation starts before writing next transmit data to SIO1TDB in external clock operation.
  If transmit errors occur during transmit operation, SIO1SR<TXERR> is set to “1” immediately after starting shift operation. Synchronizing with the next serial clock falling edge, INTSIO1 interrupt request is generated.
  If shift operation starts before writing data to SIO1TDB after SIO1CR<SIOS> is set to “1”, SIO1SR<TXERR> is set to “1” immediately after shift operation is started and then INTSIO1 interrupt request is generated.
  SIO1 pin is kept in high level when SIO1SR<TXERR> is set to “1”. When transmit error occurs, transmit operation must be forcibly stop by writing SIO1CR<SIOINH> to “1”. In this case, SIO1CR<SIOS>, SIO1SR register, SIO1RDB register and SIO1TDB register are initialized.

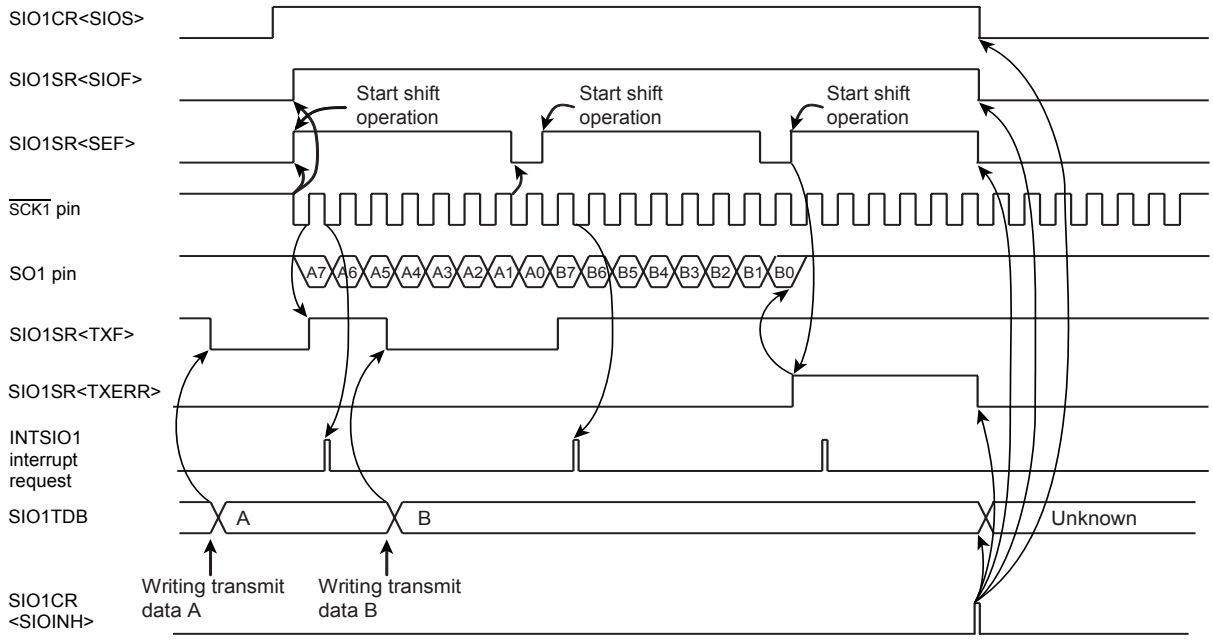


Figure 14-9 Example of Transmit Error Processingme

14.3.3.2 Receive mode

The receive mode is selected by writing “01B” to SIO1CR<SIOM>.

(1) Starting the receive operation

Receive mode is selected by setting “01” to SIO1CR<SIOM>. Serial clock is selected by using SIO1CR<SCK>. Transfer direction is selected by using SIO1CR<SIODIR>.

After SIO1CR<SIOS> is set to “1”, SIO1SR<SIOF> is set synchronously to “1” the falling edge of $\overline{\text{SCK1}}$ pin.

Synchronizing with the $\overline{\text{SCK1}}$ pin's rising edge, the data is received sequentially from SI1 pin with the direction of the bit specified by SBI1DIR<SIODIR>.

SIO1SR<SEF> is kept in high level, between the first clock falling edge of $\overline{\text{SCK1}}$ pin and eighth clock falling edge.

When 8-bit data is received, the data is transferred to SIO1RDB from shift register. INTSIO1 interrupt request is generated and SIO1SR<RXF> is set to “1”

Note: In internal clock operation, when the SIO1CR<SIOS> is set to "1", the serial clock is generated from $\overline{\text{SCK1}}$ pin after maximum 1-cycle of serial clock frequency.

(2) During the receive operation

The SIO1SR<RXF> is cleared to “0” by reading a data from SIO1RDB.

In the internal clock operation, the serial clock stops to “H” level by an automatic-wait function when the all of the 8-bit data has been received. Automatic-wait function is released by reading a received data from SIO1RDB. Then, receive operation is restarted after maximum 1-cycle of serial clock.

In external clock operation, after SIO1SR<RXF> is set to “1”, the received data must be read from SIO1RDB, before the next data shift-in operation is finished.

If received data is not read out from SIO1RDB receive error occurs immediately after shift operation is finished. Then INTSIO1 interrupt request is generated after SIO1SR<RXERR> is set to "1".

(3) Stopping the receive operation

There are two ways for stopping the receive operation.

- The way of clearing SIO1CR<SIOS>.
  When SIO1CR<SIOS> is cleared to "0", receive operation is stopped after all of the data is finished to receive. When receive operation is finished, SIO1SR<SIOF> is cleared to "0". In external clock operation, SIO1CR<SIOS> must be cleared to "0" before SIO1SR<SEF> is set to "1" by starting the next shift operation.
- The way of setting SIO1CR<SIOINH>.
  Receive operation is stopped immediately after SIO1CR<SIOINH> is set to "1". In this case, SIO1CR<SIOS>, SIO1SR register, SIO1RDB register and SIO1TDB register are initialized.

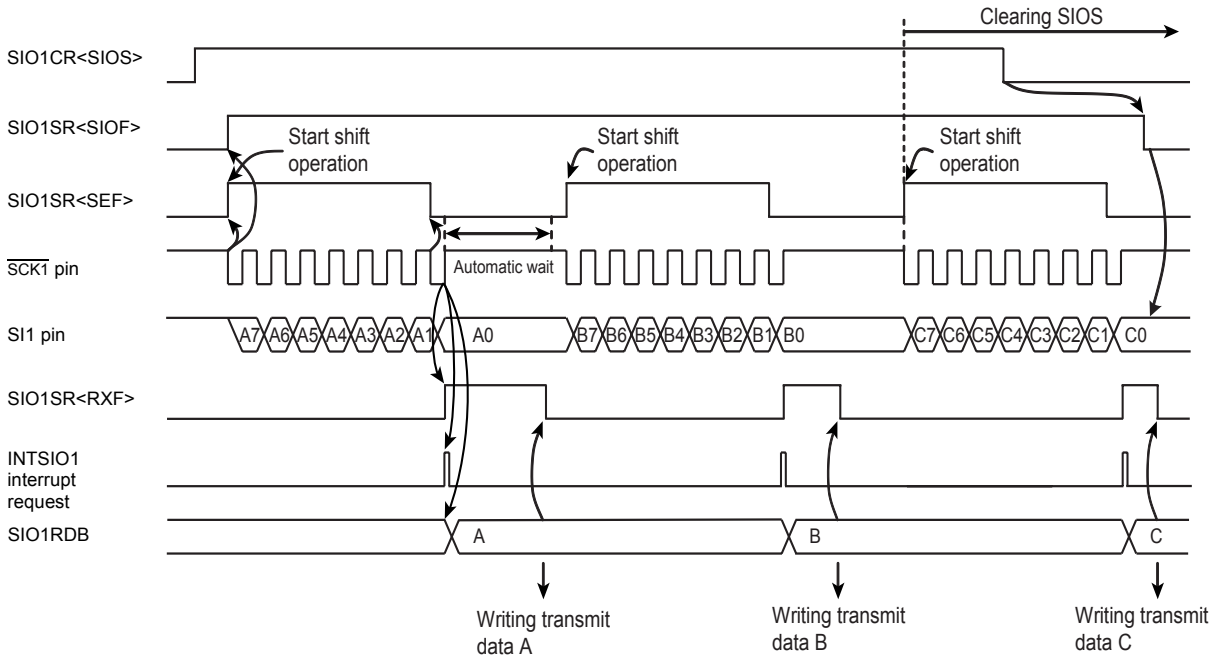


Figure 14-10 Example of Internal Clock and MSB Receive Mode

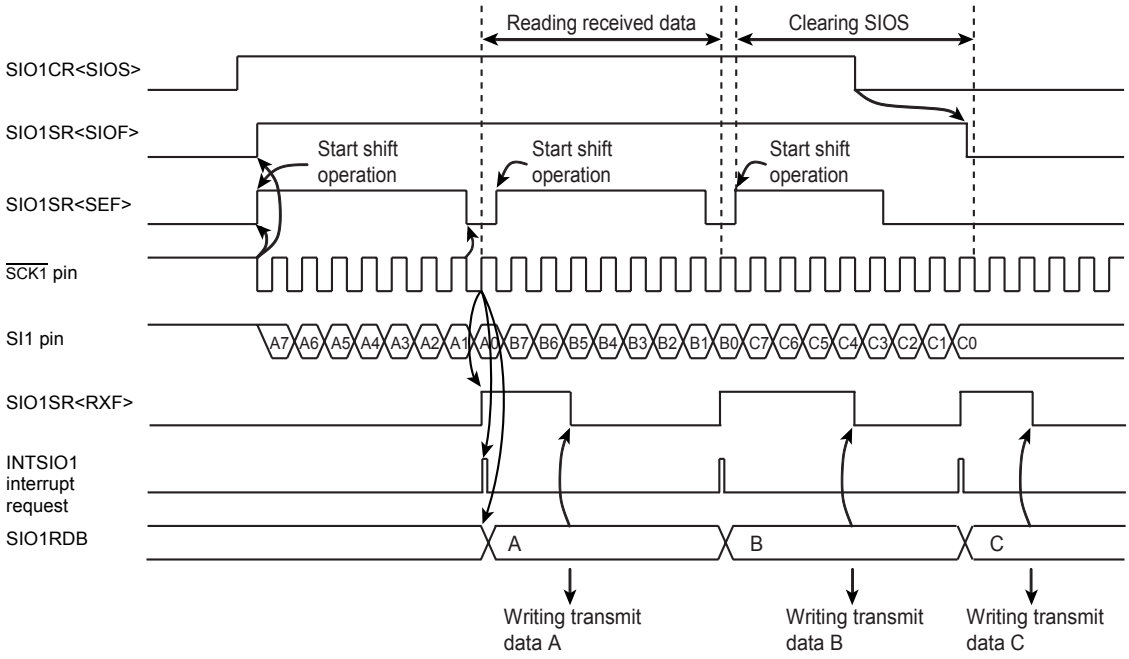


Figure 14-11 Example of External Clock and MSB Receive Mode

(4) Receive error processing

Receive errors occur on the following situation. To protect SIO1RDB and the shift register contents, the received data is ignored while the SIO1SR<RXERR> is "1".

- Shift operation is finished before reading out received data from SIO1RDB at SIO1SR<RXF> is "1" in an external clock operation.
  If receive error occurs, set the SIO1CR<SIOS> to "0" for reading the data that received immediately before error occurence. And read the data from SIO1RDB. Data in shift register (at errors occur) can be read by reading the SIO1RDB again.
  When SIO1SR<RXERR> is cleared to "0" after reading the received data, SIO1SR<RXF> is cleared to "0".
  After clearing SIO1CR<SIOS> to "0", when 8-bit serial clock is input to $\overline{\text{SCK1}}$ pin, receive operation is stopped. To restart the receive operation, confirm that SIO1SR<SIOF> is cleared to "0".
  If the receive error occurs, set the SIO1CR<SIOINH> to "1" for stopping the receive operation immediately. In this case, SIO1CR<SIOS>, SIO1SR register, SIO1RDB register and SIO1TDB register are initialized.

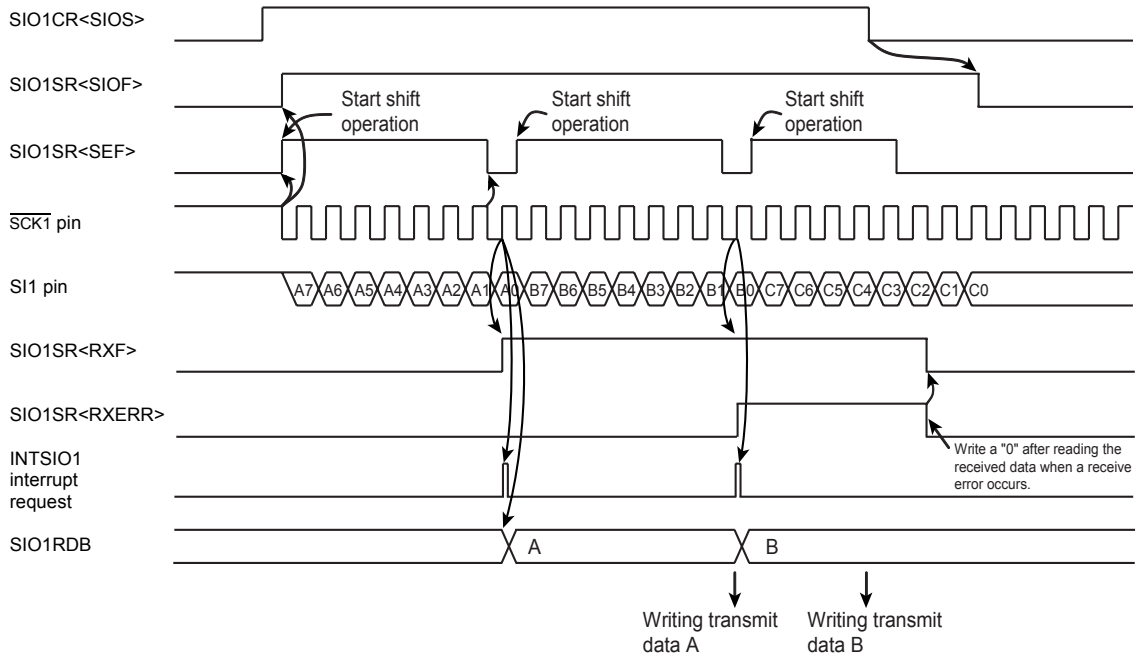


Figure 14-12 Example of Receive Error Processing

Note: If receive error is not corrected, an interrupt request does not generate after the error occurs.

14.3.3.3 Transmit/receive mode

The transmit/receive mode are selected by writing “10” to SIO1CR<SIOM>.

(1) Starting the transmit/receive operation

Transmit/receive mode is selected by writing “10B” to SIO1CR<SIOM>. Serial clock is selected by using SIO1CR<SCK>. Transfer direction is selected by using SIO1CR<SIODIR>.

When a transmit data is written to the transmit buffer register (SIO1TDB), SIO1SR<TXF> is cleared to “0”.

After SIO1CR<SIOS> is set to “1”, SIO1SR<SIOF> is set synchronously to the falling edge of $\overline{\text{SCK1}}$ pin.

The data is transferred sequentially starting from SO1 pin with the direction of the bit specified by SIO1CR<SIODIR>, synchronizing with the $\overline{\text{SCK1}}$ pin's falling edge. And receiving operation also starts with the direction of the bit specified by SIO1CR<SIODIR>, synchronizing with the $\overline{\text{SCK1}}$ pin's rising edge.

SIO1SR<SEF> is kept in high level between the first clock falling edge of $\overline{\text{SCK1}}$ pin and eighth clock falling edge.

SIO1SR<TXF> is set to “1” at the rising edge of $\overline{\text{SCK1}}$ pin after the data written to the SIO1TDB is transferred to shift register. When 8-bit data has been received, the received data is transferred to SIO1RDB from shift register, then the INTSIO1 interrupt request occurs, synchronizing with setting SIO1SR<RXF> to “1”.

Note 1: In internal clock operation, when the SIO1CR<SIOS> is set to "1", SIO1TDB is transferred to shift register after maximum 1-cycle of serial clock frequency, then a serial clock is output from $\overline{\text{SCK1}}$ pin.

Note 2: In external clock operation, when the falling edge is input from $\overline{\text{SCK1}}$ pin after SIO1CR<SIOS> is set to "1", SIO1TDB is transferred to shift register immediately. When the rising edge is input from $\overline{\text{SCK1}}$ pin, receive operation also starts.

(2) During the transmit/receive operation

When data is written to SIO1TDB, SIO1SR<TXF> is cleared to “0” and when a data is read from SIO1RDB, SIO1SR<RXF> is cleared to “0”.

In internal clock operation, in case of the condition described below, the serial clock stops to “H” level by an automatic-wait function when all of the bit set in the data has been transmitted.

- Next transmit data is not written to SIO1TDB after reading a received data from SIO1RDB.
- Received data is not read from SIO1RDB after writing a next transmit data to SIO1TDB.
- Neither SIO1TDB nor SIO1RDB is accessed after transmission.

The automatic wait function is released by writing the next transmit data to SIO1TDB after reading the received data from SIO1RDB, or reading the received data from SIO1RDB after writing the next data to SIO1TDB.
Then, transmit/receive operation is restarted after maximum 1 cycle of serial clock.
In external clock operation, reading the received data from SIO1RDB and writing the next data to SIO1TDB must be finished before the shift operation of the next data begins.
If the transmit data is not written to SIO1TDB after SIO1SR<TXF> is set to “1”, transmit error occurs immediately after shift operation is started. When the transmit error occurred, SIO1SR<TXERR> is set to “1”.
If received data is not read out from SIO1RDB before next shift operation starts after setting SIO1SR<RXF> to “1”, receive error occurs immediately after shift operation is finished. When the receive error has occurred, SIO1SR<RXERR> is set to “1”.

(3) Stopping the transmit/receive operation

There are two ways for stopping the transmit/receive operation.

- The way of clearing SIO1CR<SIOS>.
  When SIO1CR<SIOS> is cleared to “0”, transmit/receive operation is stopped after all transfer of the data is finished. When transmit/receive operation is finished, SIO1SR<SIOF> is cleared to “0” and SO1 pin is kept in high level.
  In external clock operation, SIO1CR<SIOS> must be cleared to “0” before SIO1SR<SEF> is set to “1” by beginning next transfer.
- The way of setting SIO1CR<SIOINH>.
  Transmit/receive operation is stopped immediately after SIO1CR<SIOINH> is set to “1”. In this case, SIO1CR<SIOS>, SIO1SR register, SIO1RDB register and SIO1TDB register are initialized.

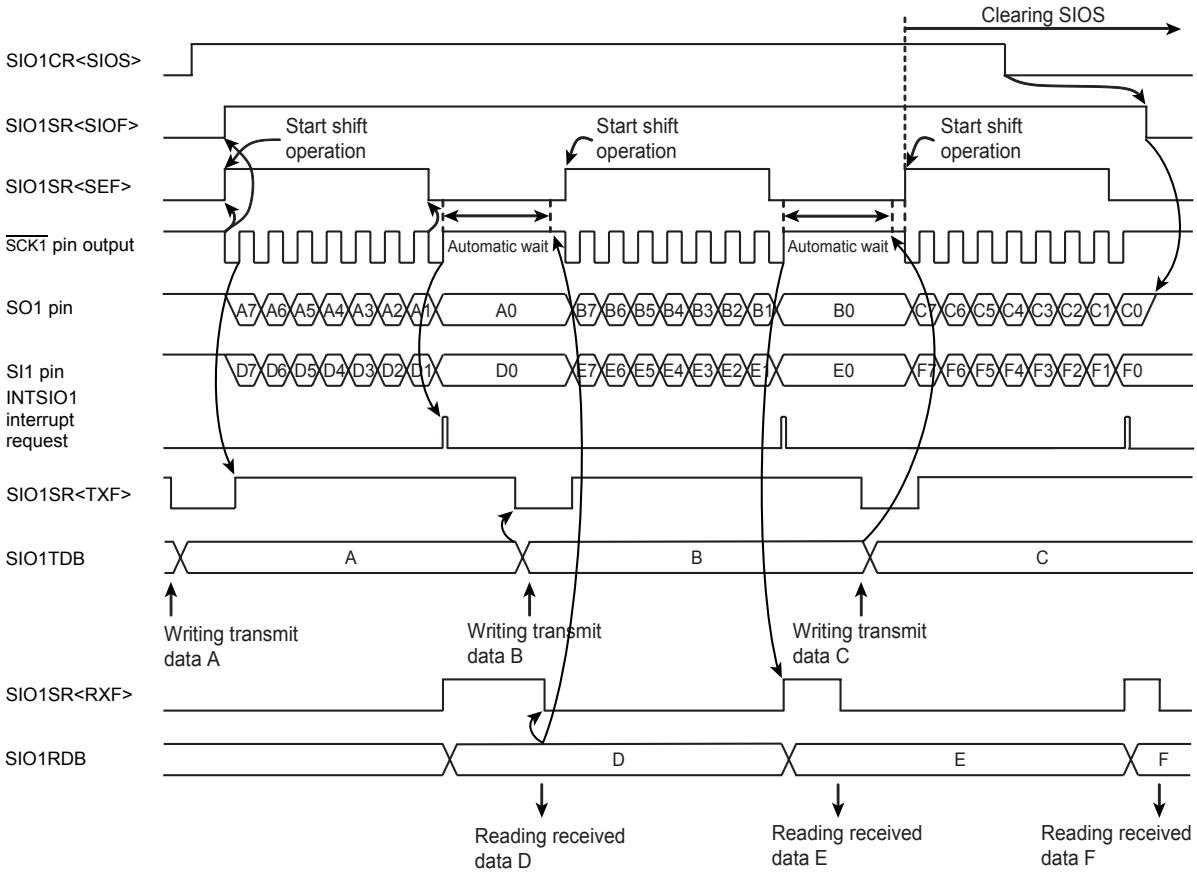


Figure 14-13 Example of Internal Clock and MSB Transmit/Receive Mode

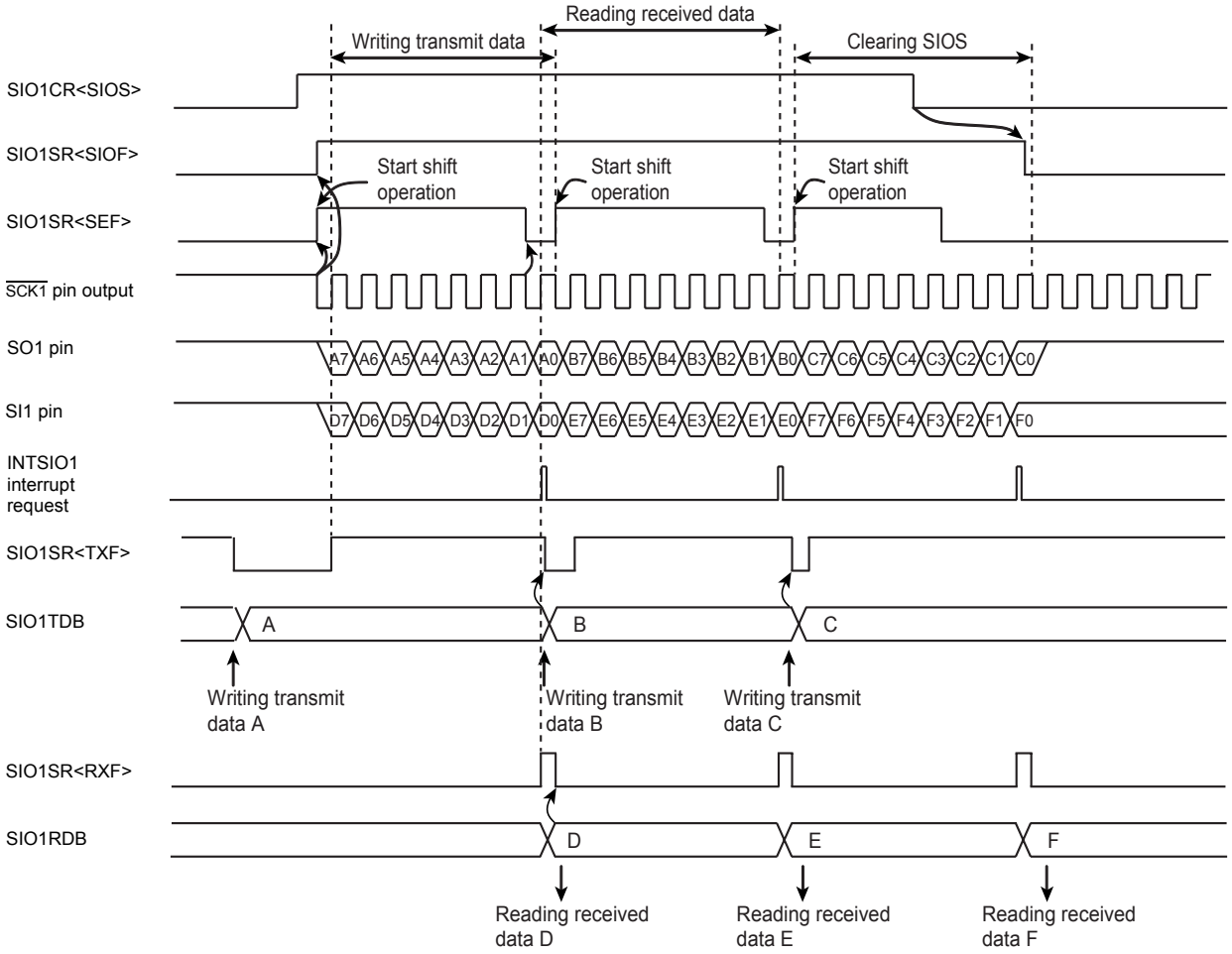


Figure 14-14 Example of External Clock and MSB Transmit/Receive Mode

(4) Transmit/receive error processing

Transmit/receive errors occur on the following situation. Corrective action is different, which errors occur transmits or receives.

(a) Transmit errors

Transmit errors occur on the following situation.

- Shift operation starts before writing next transmit data to SIO1TDB in external clock operation.
  If transmit errors occur during transmit operation, SIO1SR<TXERR> is set to “1” immediately after starting shift operation. And INTSIO1 interrupt request is generated after all of the 8-bit data has been received.
  If shift operation starts before writing data to SIO1TDB after SIO1CR<SIOS> is set to “1”, SIO1SR<TXERR> is set immediately after starting shift operation. And INTSIO1 interrupt request is generated after all of the 8-bit data has been received.
  SO1 pin is kept in high level when SIO1SR<TXERR> is set to “1”. When transmit error occurs, transmit operation must be forcibly stop by writing SIO1CR<SIOINH> to “1” after the received data is read from SIO1RDB. In this case, SIO1CR<SIOS>, SIO1SR register, SIO1RDB register and SIO1TDB register are initialized.

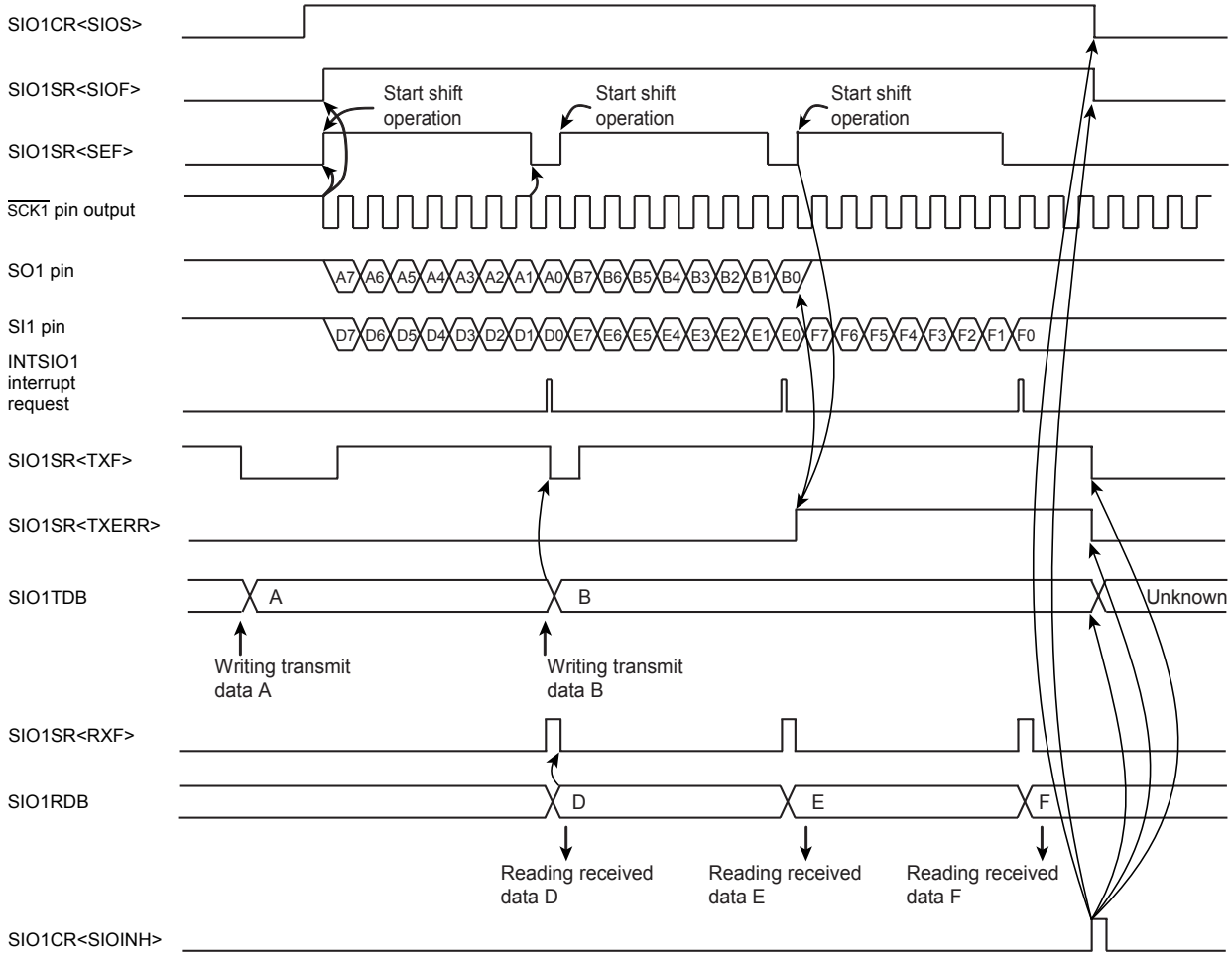


Figure 14-15 Example of Transmit/Receive (Transmit) Error Processing

(b) Receive errors

Receive errors occur on the following situation. To protect SIO1RDB and the shift register contents, the received data is ignored while the SIO1SR<RXERR> is "1".

- Shift operation is finished before reading out received data from SIO1RDB at SIO1SR<RXF> is "1" in an external clock operation.
  If receive error occurs, set the SIO1CR<SIOS> to "0" for reading the data that received immediately before error occurence. And read the data from SIO1RDB. Data in shift register (at errors occur) can be read by reading the SIO1RDB again.
  When SIO1SR<RXERR> is cleared to "0" after reading the received data, SIO1SR<RXF> is cleared to "0".
  After clearing SIO1CR<SIOS> to "0", when 8-bit serial clock is input to $\overline{\text{SCK1}}$ pin, receive operation is stopped. To restart the receive operation, confirm that SIO1SR<SIOF> is cleared to "0".
  If the received error occurs, set the SIO1CR<SIOINH> to "1" for stopping the receive operation immediately. In this case, SIO1CR<SIOS>, SIO1SR register, SIO1RDB register and SIO1TDB register are initialized.

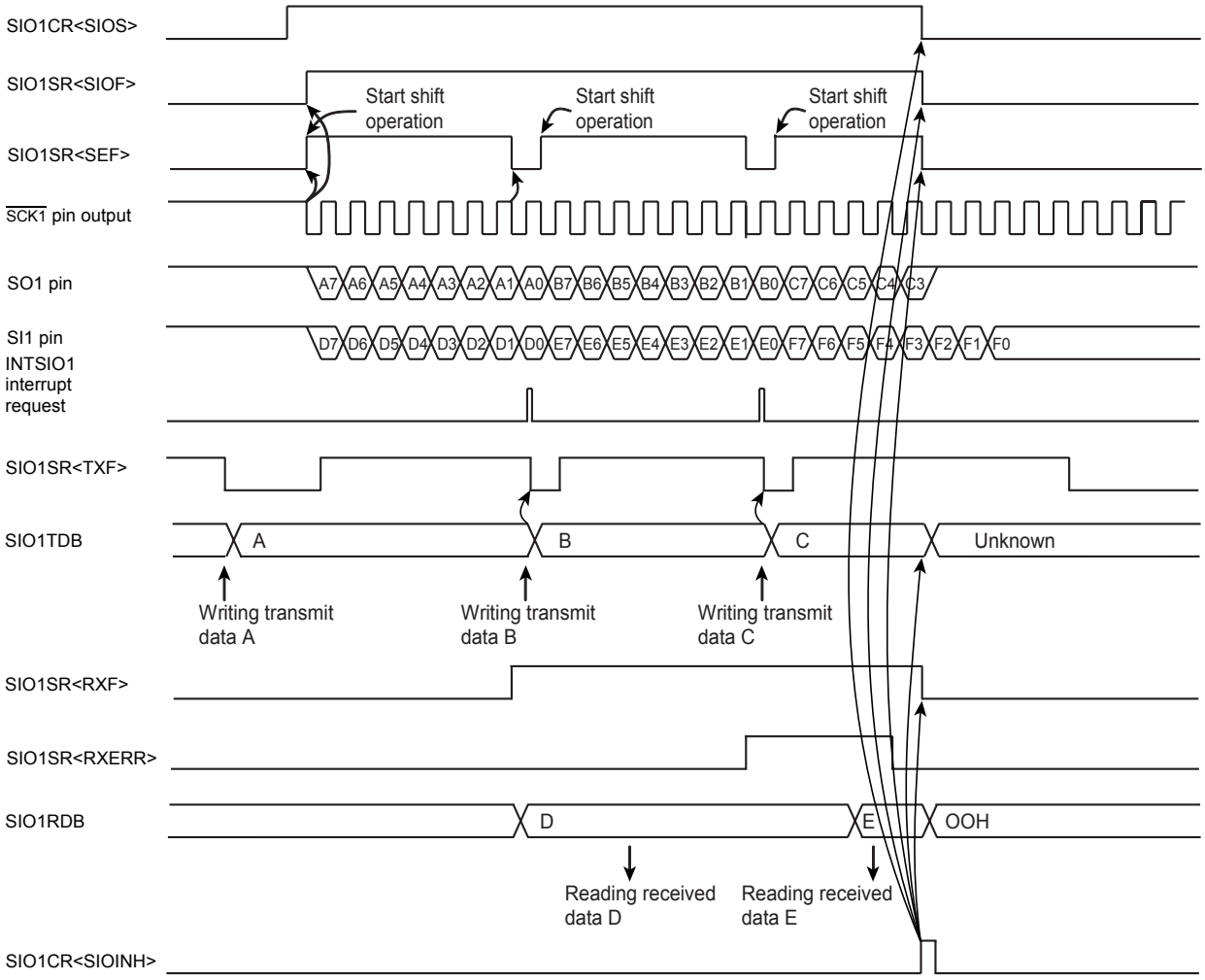


Figure 14-16 Example of Transmit/Receive (Receive) Error Processing

Note: If receive error is not corrected, an interrupt request does not generate after the error occurs.

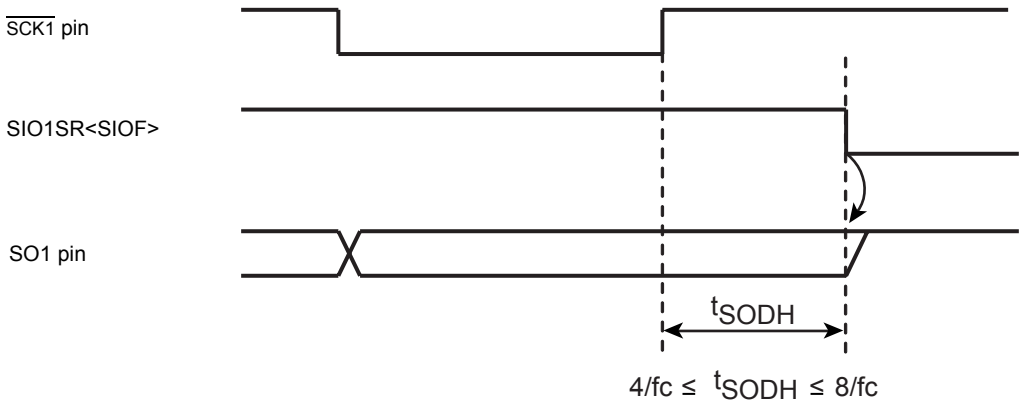


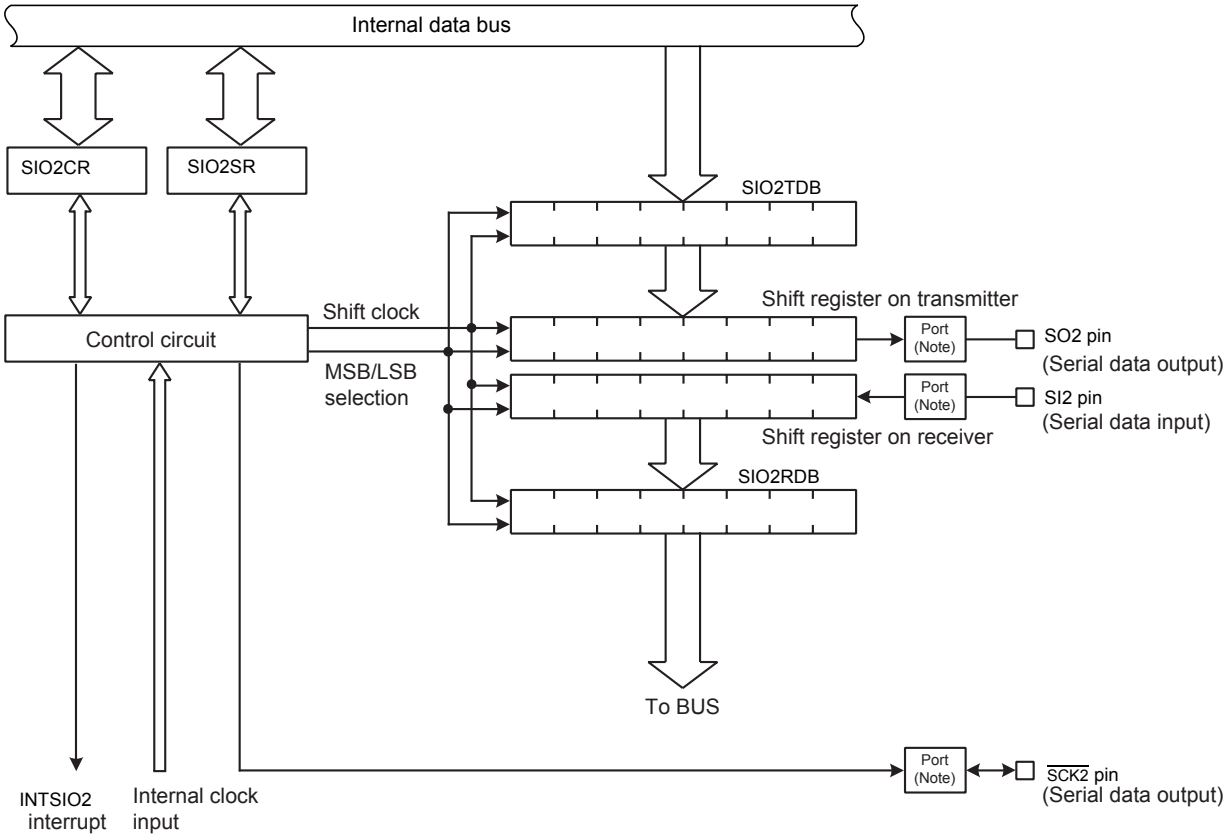
Figure 14-17 Hold Time of the End of Transmit/Receive Mode

15. Synchronous Serial Interface (SIO2)

The serial interfaces connect to an external device via SI2, SO2, and $\overline{SCK2}$ pins.

When these pins are used as serial interface, the output latches for each port should be set to "1".

15.1 Configuration



Note: Set the register of port correctly for the port assigned as serial interface pins.
For details, see the description of the input/output port control register.

Figure 15-1 Synchronous Serial Interface (SIO)

15.2 Control

The SIO is controlled using the serial interface control register (SIO2CR). The operating status of the serial interface can be inspected by reading the status register (SIO2CR).

Serial Interface Control Register

SIO2CR (0031H)

7	6	5	4	3	2	1	0
SIOS	SIOINH	SIOM		SIODIR	SCK		

(Initial value: 0000 0000)

SIOS	Specify start/stop of transfer	0: Stop 1: Start			R/W
SIOINH	Forcibly stops transfer (Note 1)	0: – 1: Forcibly stop (Automatically cleared to "0" after stopping)			
SIOM	Selects transfer mode	00: Transmit mode 01: Receive mode 10: Transmit/receive mode 11: Reserved			
SIODIR	Selects direction of transfer	0: MSB (Transfer beginning with bit7) 1: LSB (Transfer beginning with bit0)			
SCK	Selects serial clock		NORMAL1/2 or IDLE1/2 modes		SLOW/SLEEP mode
			TBTCR <DV7CK> = "0"	TBTCR <DV7CK> = "1"	
		000	$fc/2^{12}$	$fs/2^4$	$fs/2^4$
		001	$fc/2^8$	$fc/2^8$	Reserved
		010	$fc/2^7$	$fc/2^7$	Reserved
		011	$fc/2^6$	$fc/2^6$	Reserved
		100	$fc/2^5$	$fc/2^5$	Reserved
		101	$fc/2^4$	$fc/2^4$	Reserved
		110	$fc/2^3$	$fc/2^3$	Reserved
		111	External clock (Input from $\overline{SCK2}$ pin)		

Note 1: When SIO2CR<SIOINH> is set to “1”, SIO2CR<SIOS>, SIO2SR register, SIO2RDB register and SIO2TDB register are initialized.

Note 2: Transfer mode, direction of transfer and serial clock must be select during the transfer is stopping (when SIO2SR<SIOF> "0").

Note 3: fc: High-frequency clock [Hz], fs: Low-frequency clock [Hz], *: Don’t care

Serial Interface Status Register

SIO2SR (0032H)

7	6	5	4	3	2	1	0
SIOF	SEF	TXF	RXF	TXERR	RXERR		

(Initial value: 0010 00**)

SIOF	Serial transfer operation status monitor	0: Transfer finished 1: Transfer in progress	Read only
SEF	Number of clocks monitor	0: 8 clocks 1: 1 to 7 clocks	
TXF	Transmit buffer empty flag	0: Data exists in transmit buffer 1: No data exists in transmit buffer	
RXF	Receive buffer full flag	0: No data exists in receive buffer 1: Data exists in receive buffer	
TXERR	Transfer operation error flag	Read 0: – (No error exist) 1: Transmit buffer under run occurs in an external clock mode Write 0: Clear the flag 1: – (A write of "1" to this bit is ignored)	R/W
RXERR	Receive operation error flag	Read 0: – (No error exist) 1: Receive buffer over run occurs in an external clock mode Write 0: Clear the flag 1: – (A write of "1" to this bit is ignored)	

Note 1: The operation error flag (TXERR and RXERR) are not automatically cleared by stopping transfer with SIO2CR<SIOS> "0". Therefore, set these bits to "0" for clearing these error flag. Or set SIO2CR<SIOINH> to "1".

Note 2: *: Don't care

Receive buffer register

SIO2RDB (002BH)

7	6	5	4	3	2	1	0

Read only

(Initial value: 0000 0000)

Transmit buffer register

SIO2TDB (002BH)

7	6	5	4	3	2	1	0

Write only

(Initial value: **** ****)

Note 1: SIO2TDB is write only register. A bit manipulation should not be performed on the transmit buffer register using a read-modify-write instruction.

Note 2: The SIO2TDB should be written after checking SIO2SR<TXF> "1". When SIO2SR<TXF> is "0", the writing data can't be transferred to SIO2TDB even if write instruction is executed to SIO2TDB .

Note 3: *: Don't care

15.3 Function

15.3.1 Serial clock

15.3.1.1 Clock source

The serial clock can be selected by using SIO2CR<SCK>. When the serial clock is changed, the writing instruction to SIO2CR<SCK> should be executed while the transfer is stopped (when SIO2SR<SIOF> “0”)

(1) Internal clock

Setting the SIO2CR<SCK> to other than “111B” outputs the clock (shown in " Table 15-1 Serial Clock Rate (fc = 16 MHz, fs = 32.768kHz) ") as serial clock outputs from $\overline{SCK2}$ pin. At the before beginning or finishing of a transfer, $\overline{SCK2}$ pin is kept in high level.

When writing (in the transmit mode) or reading (in the receive mode) data can not follow the serial clock rate, an automatic-wait function is executed to stop the serial clock automatically and hold the next shift operation until reading or writing is completed (shown in " Figure 15-2 Automatic-wait Function (Example of transmit mode) "). The maximum time from releasing the automatic-wait function by reading or writing a data is 1 cycle of the selected serial clock until the serial clock comes out from $\overline{SCK2}$ pin.

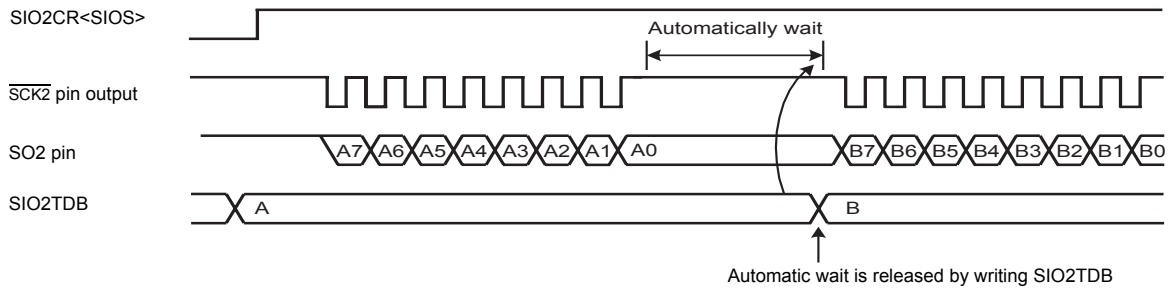


Figure 15-2 Automatic-wait Function (Example of transmit mode)

Table 15-1 Serial Clock Rate (fc = 16 MHz, fs = 32.768kHz)

	NORMAL1/2, IDLE1/2 Mode				SLOW1/2, SLEEP1/2 Mode	
	TBTCR<DV7CK> = "0"		TBTCR<DV7CK> = "1"		Serial Clock	Baud Rate
SCK	Serial Clock	Baud Rate	Serial Clock	Baud Rate		
000	$fc/2^{12}$	3.906 kbps	$fs/2^{4}$	2048 bps	$fs/2^{4}$	2048 bps
001	$fc/2^{8}$	62.5 kbps	$fc/2^{8}$	62.5 kbps	Reserved	–
010	$fc/2^{7}$	125 kbps	$fc/2^{7}$	125 kbps	Reserved	–
011	$fc/2^{6}$	250 kbps	$fc/2^{6}$	250 kbps	Reserved	–
100	$fc/2^{5}$	500 kbps	$fc/2^{5}$	500 kbps	Reserved	–
101	$fc/2^{4}$	1.00 Mbps	$fc/2^{4}$	1.00 Mbps	Reserved	–
110	$fc/2^{3}$	2.00 Mbps	$fc/2^{3}$	2.00 Mbps	Reserved	

(2) External clock

When an external clock is selected by setting SIO2CR<SCK> to "111B", the clock via the $\overline{SCK2}$ pin from an external source is used as the serial clock.

To ensure shift operation, the serial clock pulse width must be 4/fc or more for both "H" and "L" levels.

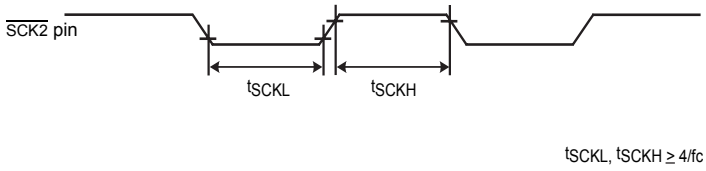


Figure 15-3 External Clock

15.3.1.2 Shift edge

The leading edge is used to transmit data, and the trailing edge is used to receive data.

(1) Leading edge shift

Data is shifted on the leading edge of the serial clock (falling edge of the $\overline{SCK2}$ pin input/output).

(2) Trailing edge shift

Data is shifted on the trailing edge of the serial clock (rising edge of the $\overline{SCK2}$ pin input/output).

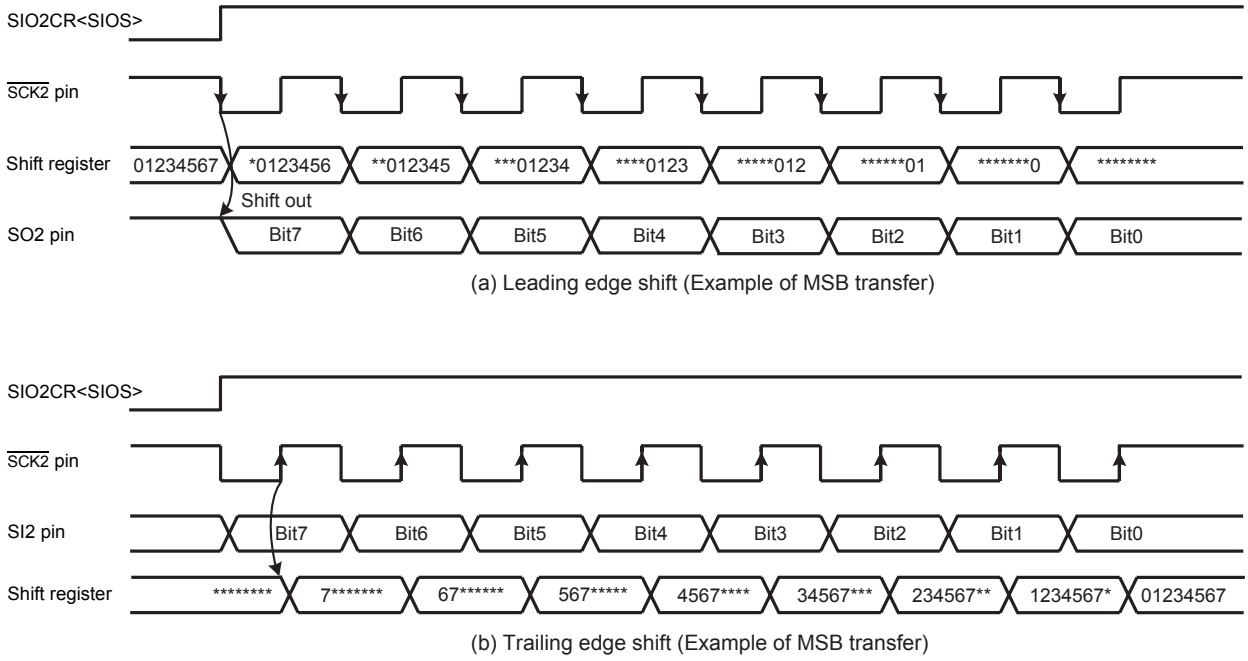


Figure 15-4 Shift Edge

15.3.2 Transfer bit direction

Transfer data direction can be selected by using SIO2CR<SIODIR>. The transfer data direction can't be set individually for transmit and receive operations.

When the data direction is changed, the writing instruction to SIO2CR<SIODIR> should be executed while the transfer is stopped (when SIO2CR<SIOF>= “0”)

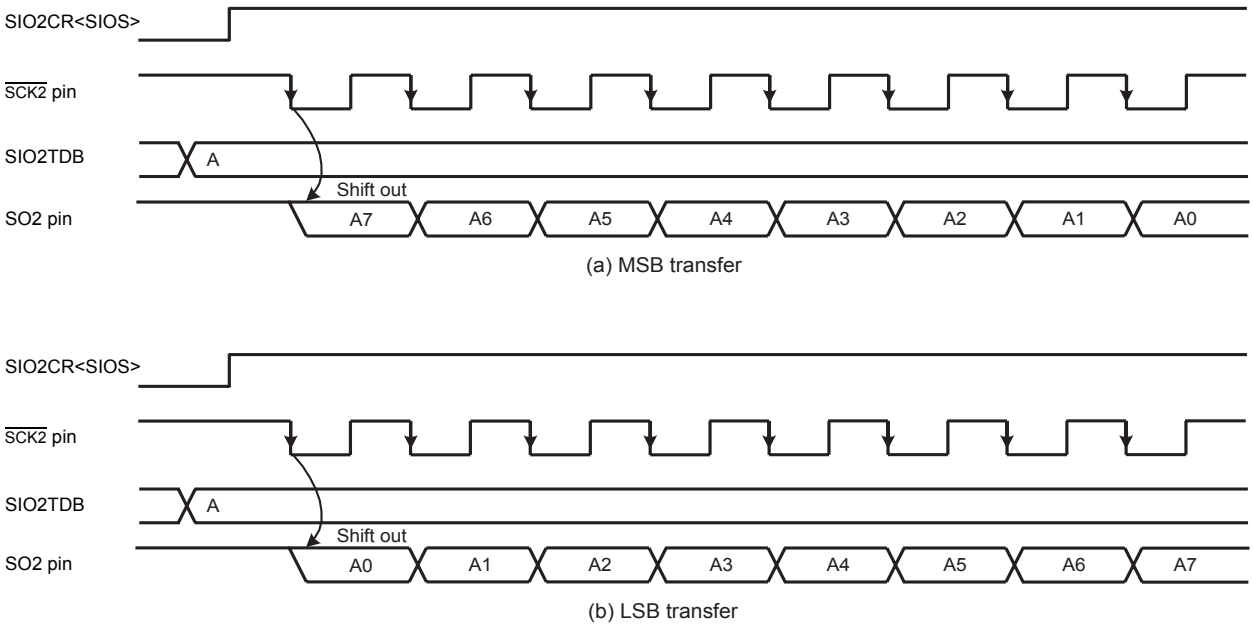


Figure 15-5 Transfer Bit Direction (Example of transmit mode)

15.3.2.1 Transmit mode

(1) MSB transmit mode

MSB transmit mode is selected by setting SIO2CR<SIODIR> to “0”, in which case the data is transferred sequentially beginning with the most significant bit (Bit7).

(2) LSB transmit mode

LSB transmit mode is selected by setting SIO2CR<SIODIR> to “1”, in which case the data is transferred sequentially beginning with the least significant bit (Bit0).

15.3.2.2 Receive mode

(1) MSB receive mode

MSB receive mode is selected by setting SIO2CR<SIODIR> to “0”, in which case the data is received sequentially beginning with the most significant bit (Bit7).

(2) LSB receive mode

LSB receive mode is selected by setting SIO2CR<SIODIR> to “1”, in which case the data is received sequentially beginning with the least significant bit (Bit0).

15.3.2.3 Transmit/receive mode

(1) MSB transmit/receive mode

MSB transmit/receive mode are selected by setting SIO2CR<SIODIR> to “0” in which case the data is transferred sequentially beginning with the most significant bit (Bit7) and the data is received sequentially beginning with the most significant (Bit7).

(2) LSB transmit/receive mode

LSB transmit/receive mode are selected by setting SIO2CR<SIODIR> to “1”, in which case the data is transferred sequentially beginning with the least significant bit (Bit0) and the data is received sequentially beginning with the least significant (Bit0).

15.3.3 Transfer modes

Transmit, receive and transmit/receive mode are selected by using SIO2CR<SIOM>.

15.3.3.1 Transmit mode

Transmit mode is selected by writing “00B” to SIO2CR<SIOM>.

(1) Starting the transmit operation

Transmit mode is selected by setting “00B” to SIO2CR<SIOM>. Serial clock is selected by using SIO2CR<SCK>. Transfer direction is selected by using SIO2CR<SIODIR>.

When a transmit data is written to the transmit buffer register (SIO2TDB), SIO2SR<TXF> is cleared to “0”.

After SIO2CR<SIOS> is set to “1”, SIO2SR<SIOF> is set synchronously to “1” the falling edge of $\overline{\text{SCK2}}$ pin.

The data is transferred sequentially starting from SO2 pin with the direction of the bit specified by SIO2CR<SIODIR>, synchronizing with the $\overline{\text{SCK2}}$ pin's falling edge.

SIO2SR<SEF> is kept in high level, between the first clock falling edge of $\overline{\text{SCK2}}$ pin and eighth clock falling edge.

SIO2SR<TXF> is set to “1” at the rising edge of pin after the data written to the SIO2TDB is transferred to shift register, then the INTSIO2 interrupt request is generated, synchronizing with the next falling edge on $\overline{\text{SCK2}}$ pin.

Note 1: In internal clock operation, when SIO2CR<SIOS> is set to "1", transfer mode does not start without writing a transmit data to the transmit buffer register (SIO2TDB).

Note 2: In internal clock operation, when the SIO2CR<SIOS> is set to "1", SIO2TDB is transferred to shift register after maximum 1-cycle of serial clock frequency, then a serial clock is output from $\overline{\text{SCK2}}$ pin.

Note 3: In external clock operation, when the falling edge is input from $\overline{\text{SCK2}}$ pin after SIO2CR<SIOS> is set to "1", SIO2TDB is transferred to shift register immediately.

(2) During the transmit operation

When data is written to SIO2TDB, SIO2SR<TXF> is cleared to “0”.

In internal clock operation, in case a next transmit data is not written to SIO2TDB, the serial clock stops to “H” level by an automatic-wait function when all of the bit set in the SIO2TDB has been transmitted. Automatic-wait function is released by writing a transmit data to SIO2TDB. Then, transmit operation is restarted after maximum 1-cycle of serial clock.

When the next data is written to the SIO2TDB before termination of previous 8-bit data with SIO2SR<TXF> “1”, the next data is continuously transferred after transmission of previous data.

In external clock operation, after SIO2SR<TXF> is set to “1”, the transmit data must be written to SIO2TDB before the shift operation of the next data begins.

If the transmit data is not written to SIO2TDB, transmit error occurs immediately after shift operation is started. Then, INTSIO2 interrupt request is generated after SIO2SR<TXERR> is set to “1”.

(3) Stopping the transmit operation

There are two ways for stopping transmits operation.

- The way of clearing SIO2CR<SIOS>.
  When SIO2CR<SIOS> is cleared to “0”, transmit operation is stopped after all transfer of the data is finished. When transmit operation is finished, SIO2SR<SIOF> is cleared to “0” and SO2 pin is kept in high level.
  In external clock operation, SIO2CR<SIOS> must be cleared to “0” before SIO2SR<SEF> is set to “1” by beginning next transfer.
- The way of setting SIO2CR<SIOINH>.
  Transmit operation is stopped immediately after SIO2CR<SIOINH> is set to “1”. In this case, SIO2CR<SIOS>, SIO2SR register, SIO2RDB register and SIO2TDB register are initialized.

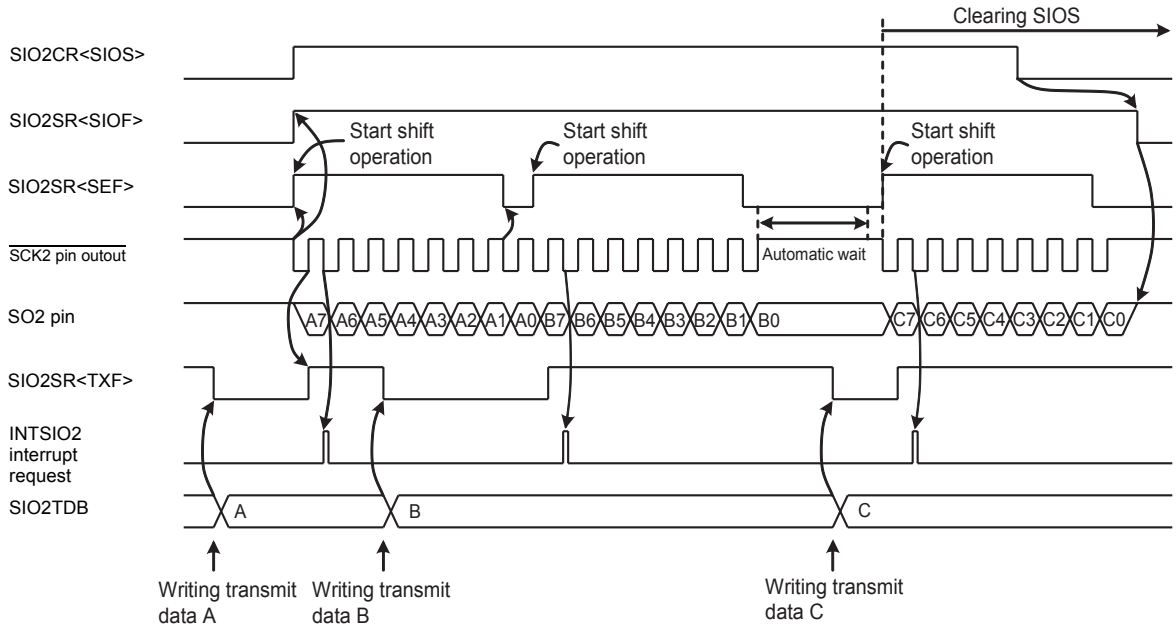


Figure 15-6 Example of Internal Clock and MSB Transmit Mode

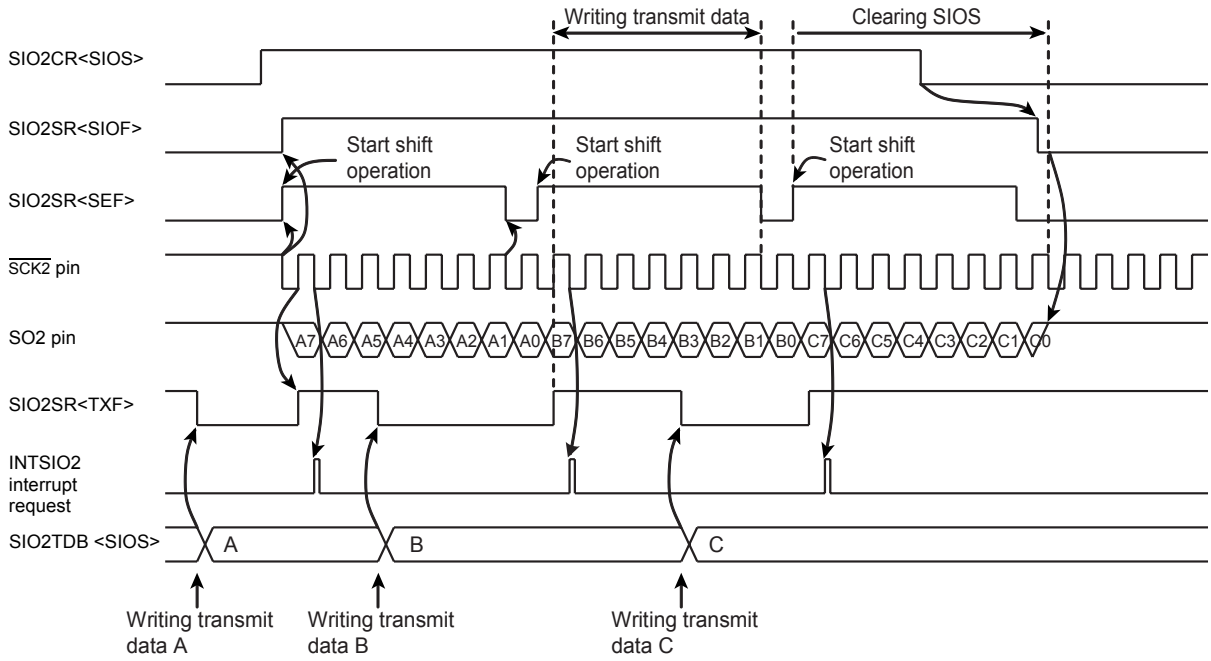


Figure 15-7 Exaple of External Clock and MSB Transmit Mode

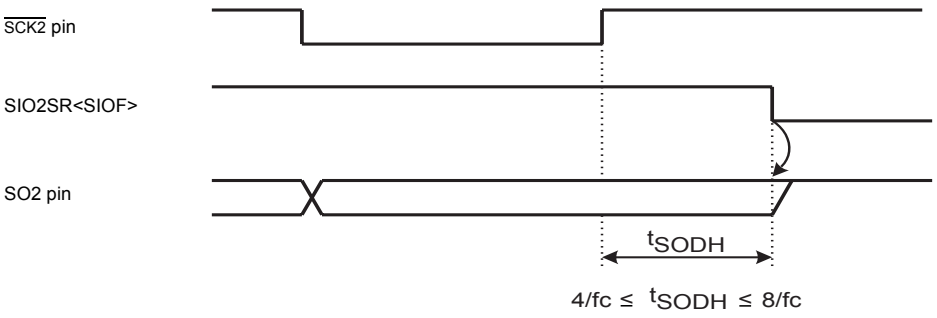


Figure 15-8 Hold Time of the End of Transmit Mode

(4) Transmit error processing

Transmit errors occur on the following situation.

- Shift operation starts before writing next transmit data to SIO2TDB in external clock operation.
  If transmit errors occur during transmit operation, SIO2SR<TXERR> is set to “1” immediately after starting shift operation. Synchronizing with the next serial clock falling edge, INTSIO2 interrupt request is generated.
  If shift operation starts before writing data to SIO2TDB after SIO2CR<SIOS> is set to “1”, SIO2SR<TXERR> is set to “1” immediately after shift operation is started and then INTSIO2 interrupt request is generated.
  SIO2 pin is kept in high level when SIO2SR<TXERR> is set to “1”. When transmit error occurs, transmit operation must be forcibly stop by writing SIO2CR<SIOINH> to “1”. In this case, SIO2CR<SIOS>, SIO2SR register, SIO2RDB register and SIO2TDB register are initialized.

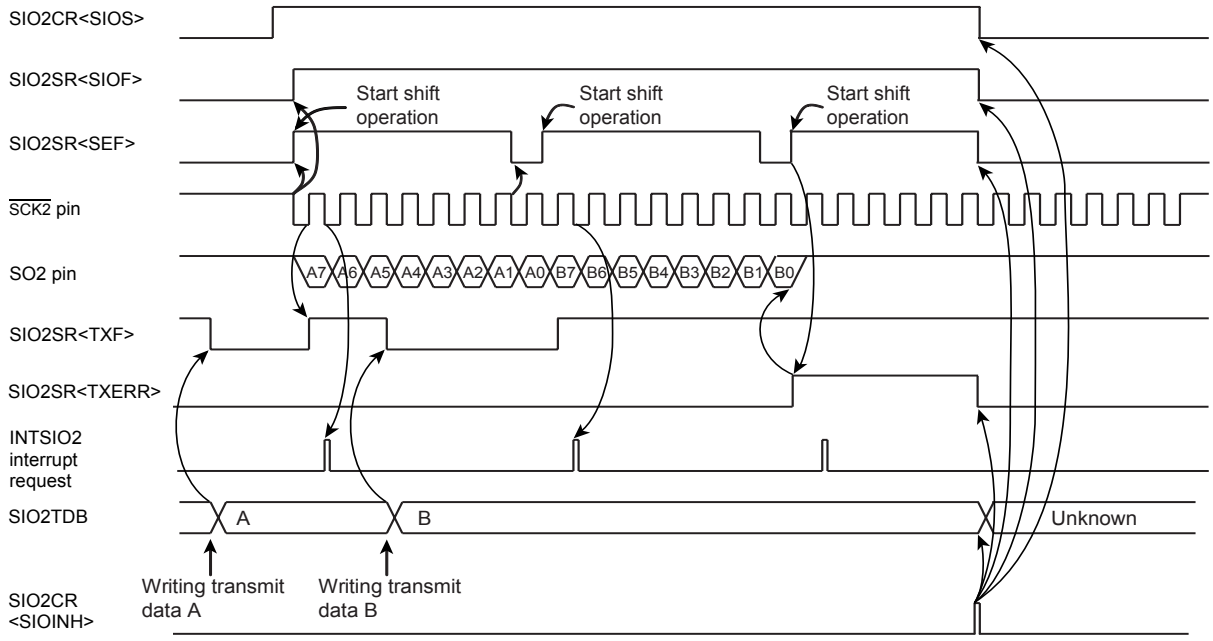


Figure 15-9 Example of Transmit Error Processingme

15.3.3.2 Receive mode

The receive mode is selected by writing “01B” to SIO2CR<SIOM>.

(1) Starting the receive operation

Receive mode is selected by setting “01” to SIO2CR<SIOM>. Serial clock is selected by using SIO2CR<SCK>. Transfer direction is selected by using SIO2CR<SIODIR>.

After SIO2CR<SIOS> is set to “1”, SIO2SR<SIOF> is set synchronously to “1” the falling edge of $\overline{\text{SCK2}}$ pin.

Synchronizing with the $\overline{\text{SCK2}}$ pin's rising edge, the data is received sequentially from SI2 pin with the direction of the bit specified by SBI2DIR<SIODIR>.

SIO2SR<SEF> is kept in high level, between the first clock falling edge of $\overline{\text{SCK2}}$ pin and eighth clock falling edge.

When 8-bit data is received, the data is transferred to SIO2RDB from shift register. INTSIO2 interrupt request is generated and SIO2SR<RXF> is set to “1”

Note: In internal clock operation, when the SIO2CR<SIOS> is set to "1", the serial clock is generated from $\overline{\text{SCK2}}$ pin after maximum 1-cycle of serial clock frequency.

(2) During the receive operation

The SIO2SR<RXF> is cleared to “0” by reading a data from SIO2RDB.

In the internal clock operation, the serial clock stops to “H” level by an automatic-wait function when the all of the 8-bit data has been received. Automatic-wait function is released by reading a received data from SIO2RDB. Then, receive operation is restarted after maximum 1-cycle of serial clock.

In external clock operation, after SIO2SR<RXF> is set to “1”, the received data must be read from SIO2RDB, before the next data shift-in operation is finished.

If received data is not read out from SIO2RDB receive error occurs immediately after shift operation is finished. Then INTSIO2 interrupt request is generated after SIO2SR<RXERR> is set to "1".

(3) Stopping the receive operation

There are two ways for stopping the receive operation.

- The way of clearing SIO2CR<SIOS>.
  When SIO2CR<SIOS> is cleared to "0", receive operation is stopped after all of the data is finished to receive. When receive operation is finished, SIO2SR<SIOF> is cleared to "0". In external clock operation, SIO2CR<SIOS> must be cleared to "0" before SIO2SR<SEF> is set to "1" by starting the next shift operation.
- The way of setting SIO2CR<SIOINH>.
  Receive operation is stopped immediately after SIO2CR<SIOINH> is set to "1". In this case, SIO2CR<SIOS>, SIO2SR register, SIO2RDB register and SIO2TDB register are initialized.

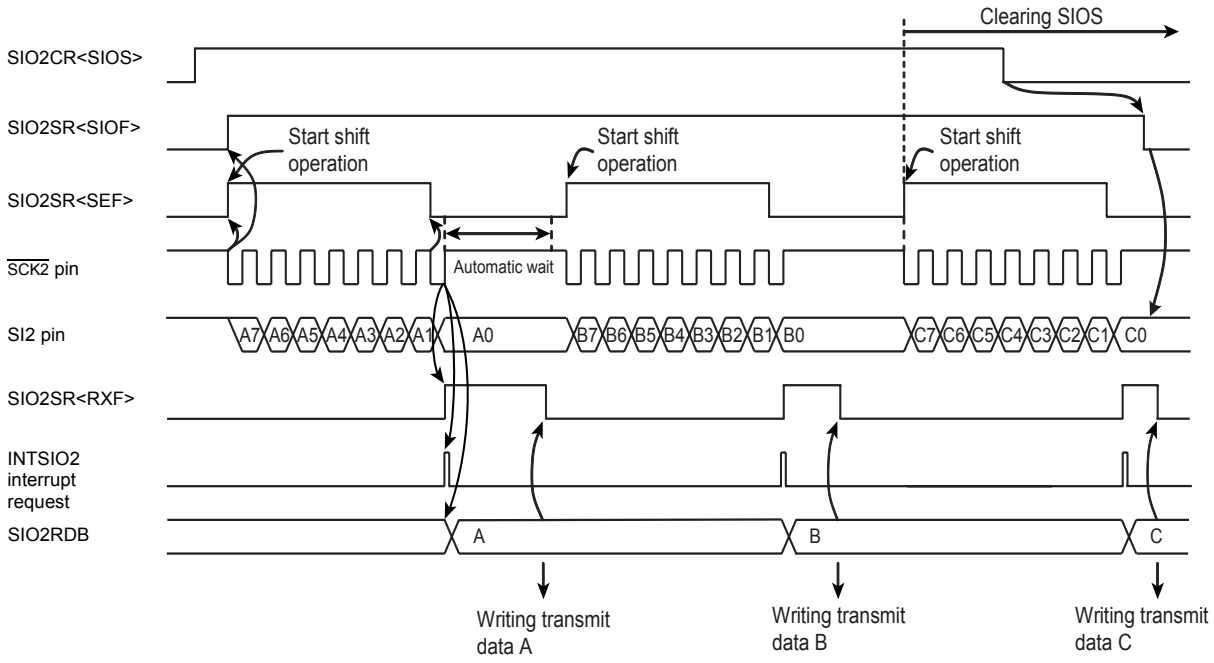


Figure 15-10 Example of Internal Clock and MSB Receive Mode

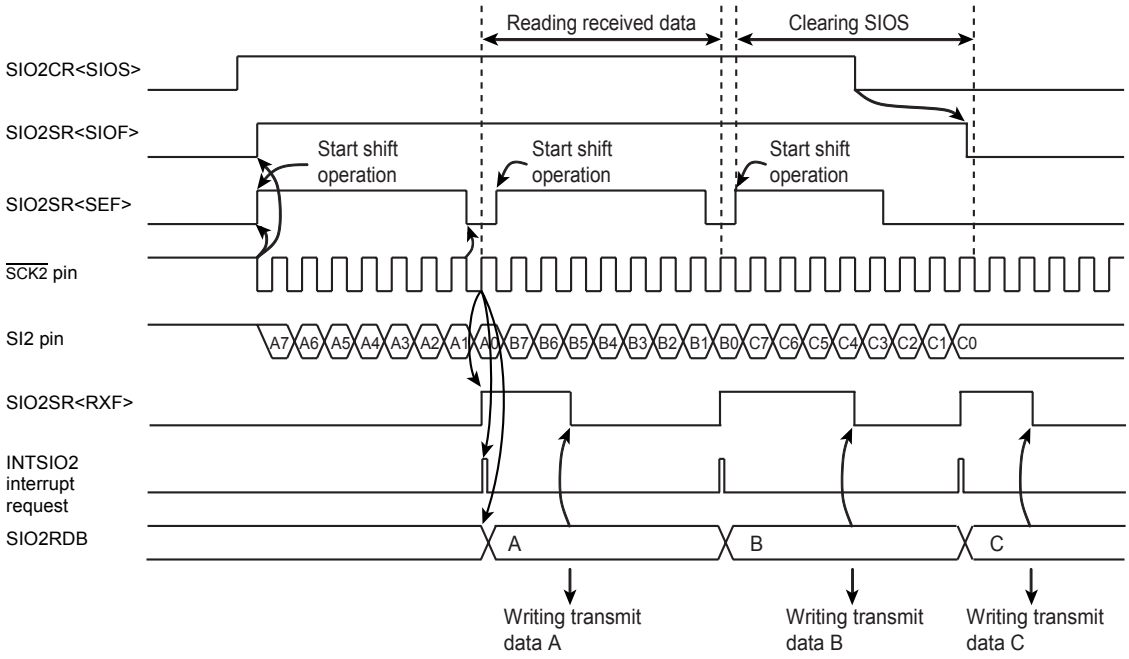


Figure 15-11 Example of External Clock and MSB Receive Mode

(4) Receive error processing

Receive errors occur on the following situation. To protect SIO2RDB and the shift register contents, the received data is ignored while the SIO2SR<RXERR> is "1".

- Shift operation is finished before reading out received data from SIO2RDB at SIO2SR<RXF> is "1" in an external clock operation.
  If receive error occurs, set the SIO2CR<SIOS> to "0" for reading the data that received immediately before error occurence. And read the data from SIO2RDB. Data in shift register (at errors occur) can be read by reading the SIO2RDB again.
  When SIO2SR<RXERR> is cleared to "0" after reading the received data, SIO2SR<RXF> is cleared to "0".
  After clearing SIO2CR<SIOS> to "0", when 8-bit serial clock is input to $\overline{\text{SCK2}}$ pin, receive operation is stopped. To restart the receive operation, confirm that SIO2SR<SIOF> is cleared to "0".
  If the receive error occurs, set the SIO2CR<SIOINH> to "1" for stopping the receive operation immediately. In this case, SIO2CR<SIOS>, SIO2SR register, SIO2RDB register and SIO2TDB register are initialized.

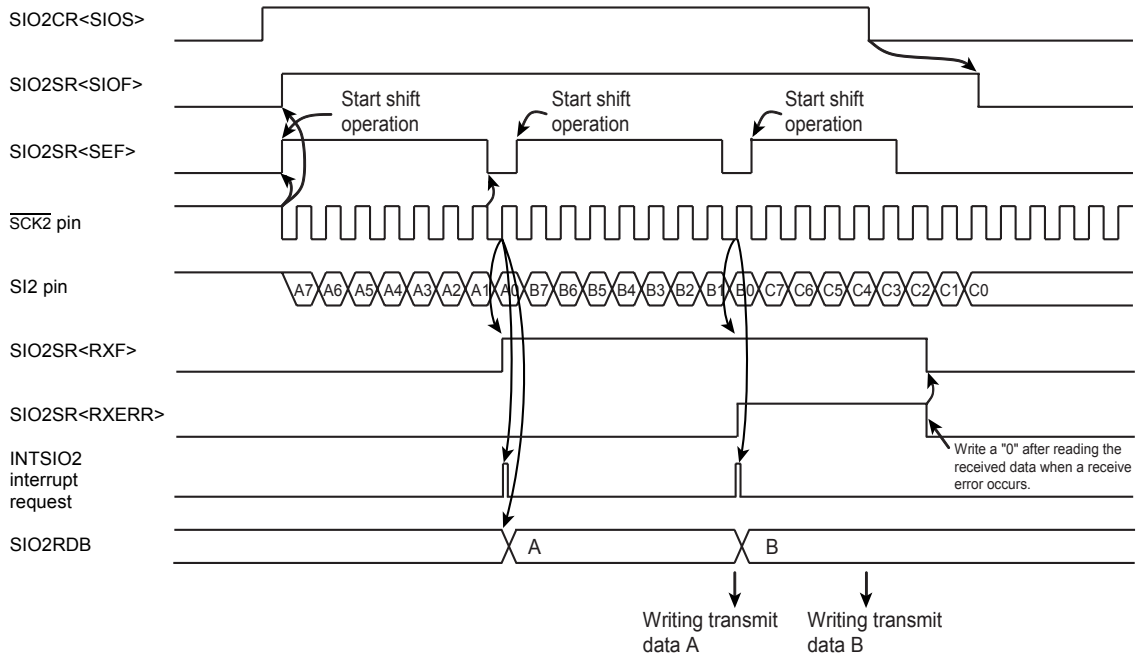


Figure 15-12 Example of Receive Error Processing

Note: If receive error is not corrected, an interrupt request does not generate after the error occurs.

15.3.3.3 Transmit/receive mode

The transmit/receive mode are selected by writing “10” to SIO2CR<SIOM>.

(1) Starting the transmit/receive operation

Transmit/receive mode is selected by writing “10B” to SIO2CR<SIOM>. Serial clock is selected by using SIO2CR<SCK>. Transfer direction is selected by using SIO2CR<SIODIR>.

When a transmit data is written to the transmit buffer register (SIO2TDB), SIO2SR<TXF> is cleared to “0”.

After SIO2CR<SIOS> is set to “1”, SIO2SR<SIOF> is set synchronously to the falling edge of $\overline{\text{SCK2}}$ pin.

The data is transferred sequentially starting from SO2 pin with the direction of the bit specified by SIO2CR<SIODIR>, synchronizing with the $\overline{\text{SCK2}}$ pin's falling edge. And receiving operation also starts with the direction of the bit specified by SIO2CR<SIODIR>, synchronizing with the $\overline{\text{SCK2}}$ pin's rising edge.

SIO2SR<SEF> is kept in high level between the first clock falling edge of $\overline{\text{SCK2}}$ pin and eighth clock falling edge.

SIO2SR<TXF> is set to “1” at the rising edge of $\overline{\text{SCK2}}$ pin after the data written to the SIO2TDB is transferred to shift register. When 8-bit data has been received, the received data is transferred to SIO2RDB from shift register, then the INTSIO2 interrupt request occurs, synchronizing with setting SIO2SR<RXF> to “1”.

Note 1: In internal clock operation, when the SIO2CR<SIOS> is set to "1", SIO2TDB is transferred to shift register after maximum 1-cycle of serial clock frequency, then a serial clock is output from $\overline{\text{SCK2}}$ pin.

Note 2: In external clock operation, when the falling edge is input from $\overline{\text{SCK2}}$ pin after SIO2CR<SIOS> is set to "1", SIO2TDB is transferred to shift register immediately. When the rising edge is input from $\overline{\text{SCK2}}$ pin, receive operation also starts.

(2) During the transmit/receive operation

When data is written to SIO2TDB, SIO2SR<TXF> is cleared to “0” and when a data is read from SIO2RDB, SIO2SR<RXF> is cleared to “0”.

In internal clock operation, in case of the condition described below, the serial clock stops to “H” level by an automatic-wait function when all of the bit set in the data has been transmitted.

- Next transmit data is not written to SIO2TDB after reading a received data from SIO2RDB.
- Received data is not read from SIO2RDB after writing a next transmit data to SIO2TDB.
- Neither SIO2TDB nor SIO2RDB is accessed after transmission.

The automatic wait function is released by writing the next transmit data to SIO2TDB after reading the received data from SIO2RDB, or reading the received data from SIO2RDB after writing the next data to SIO2TDB.
Then, transmit/receive operation is restarted after maximum 1 cycle of serial clock.
In external clock operation, reading the received data from SIO2RDB and writing the next data to SIO2TDB must be finished before the shift operation of the next data begins.
If the transmit data is not written to SIO2TDB after SIO2SR<TXF> is set to “1”, transmit error occurs immediately after shift operation is started. When the transmit error occurred, SIO2SR<TXERR> is set to “1”.
If received data is not read out from SIO2RDB before next shift operation starts after setting SIO2SR<RXF> to “1”, receive error occurs immediately after shift operation is finished. When the receive error has occurred, SIO2SR<RXERR> is set to “1”.

(3) Stopping the transmit/receive operation

There are two ways for stopping the transmit/receive operation.

- The way of clearing SIO2CR<SIOS>.
  When SIO2CR<SIOS> is cleared to “0”, transmit/receive operation is stopped after all transfer of the data is finished. When transmit/receive operation is finished, SIO2SR<SIOF> is cleared to “0” and SO2 pin is kept in high level.
  In external clock operation, SIO2CR<SIOS> must be cleared to “0” before SIO2SR<SEF> is set to “1” by beginning next transfer.
- The way of setting SIO2CR<SIOINH>.
  Transmit/receive operation is stopped immediately after SIO2CR<SIOINH> is set to “1”. In this case, SIO2CR<SIOS>, SIO2SR register, SIO2RDB register and SIO2TDB register are initialized.

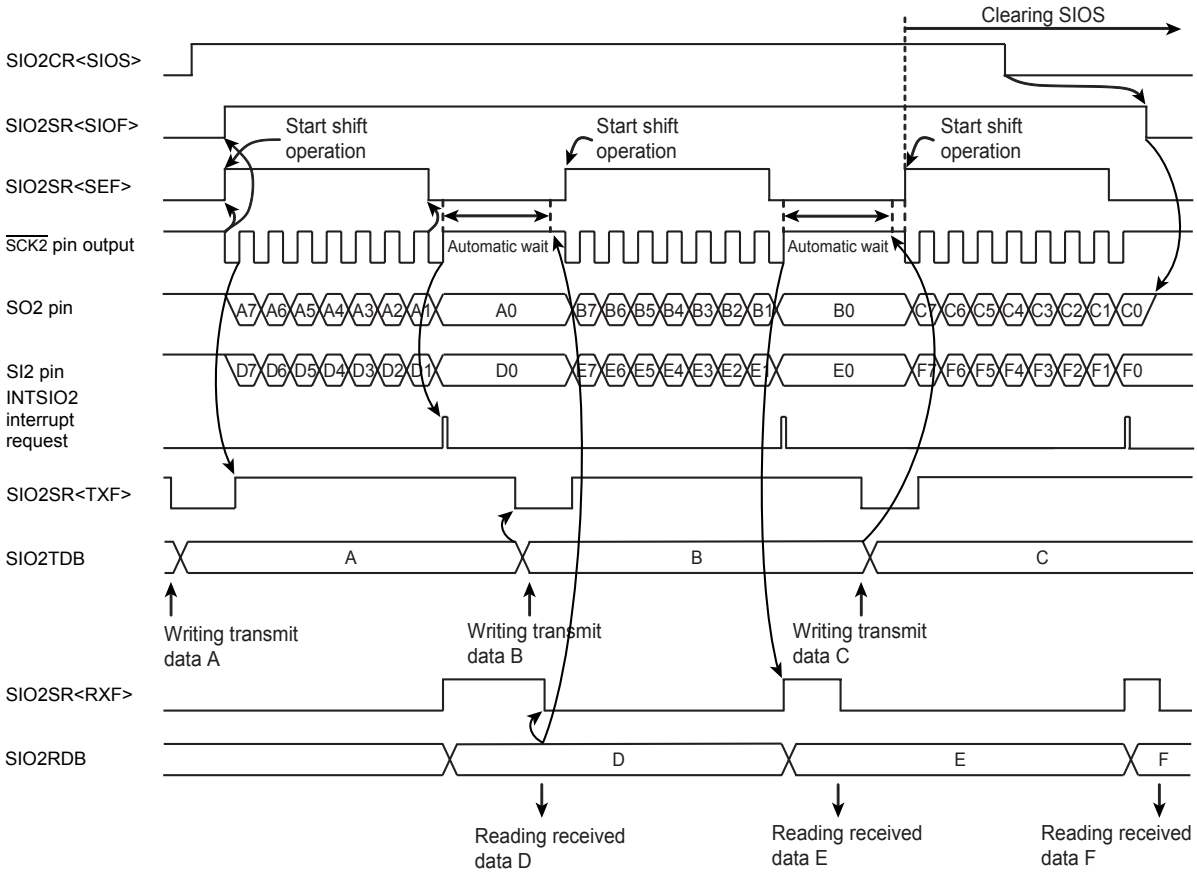


Figure 15-13 Example of Internal Clock and MSB Transmit/Receive Mode

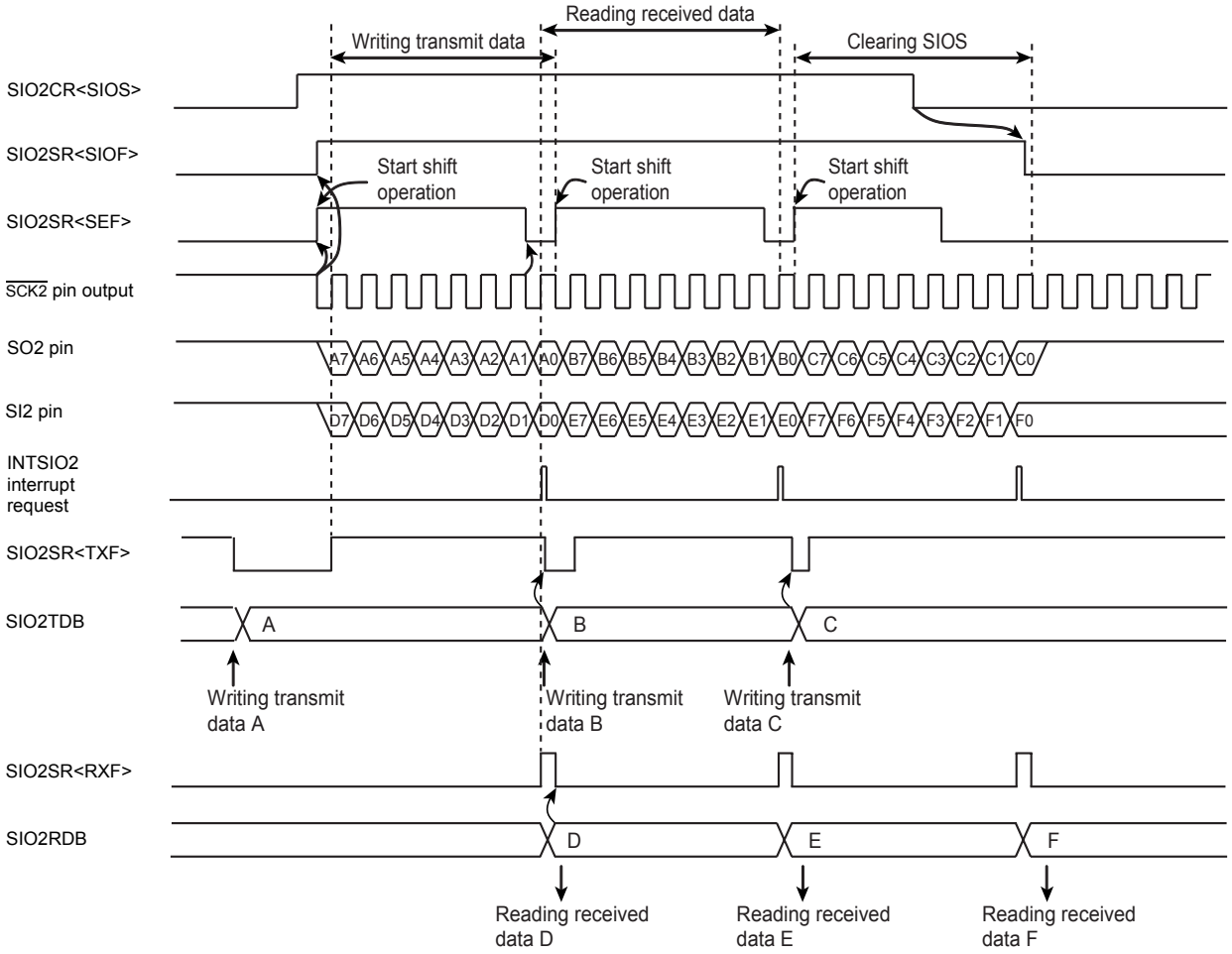


Figure 15-14 Example of External Clock and MSB Transmit/Receive Mode

(4) Transmit/receive error processing

Transmit/receive errors occur on the following situation. Corrective action is different, which errors occur transmits or receives.

(a) Transmit errors

Transmit errors occur on the following situation.

- Shift operation starts before writing next transmit data to SIO2TDB in external clock operation.
  If transmit errors occur during transmit operation, SIO2SR<TXERR> is set to “1” immediately after starting shift operation. And INTSIO2 interrupt request is generated after all of the 8-bit data has been received.
  If shift operation starts before writing data to SIO2TDB after SIO2CR<SIOS> is set to “1”, SIO2SR<TXERR> is set immediately after starting shift operation. And INTSIO2 interrupt request is generated after all of the 8-bit data has been received.
  SO2 pin is kept in high level when SIO2SR<TXERR> is set to “1”. When transmit error occurs, transmit operation must be forcibly stop by writing SIO2CR<SIOINH> to “1” after the received data is read from SIO2RDB. In this case, SIO2CR<SIOS>, SIO2SR register, SIO2RDB register and SIO2TDB register are initialized.

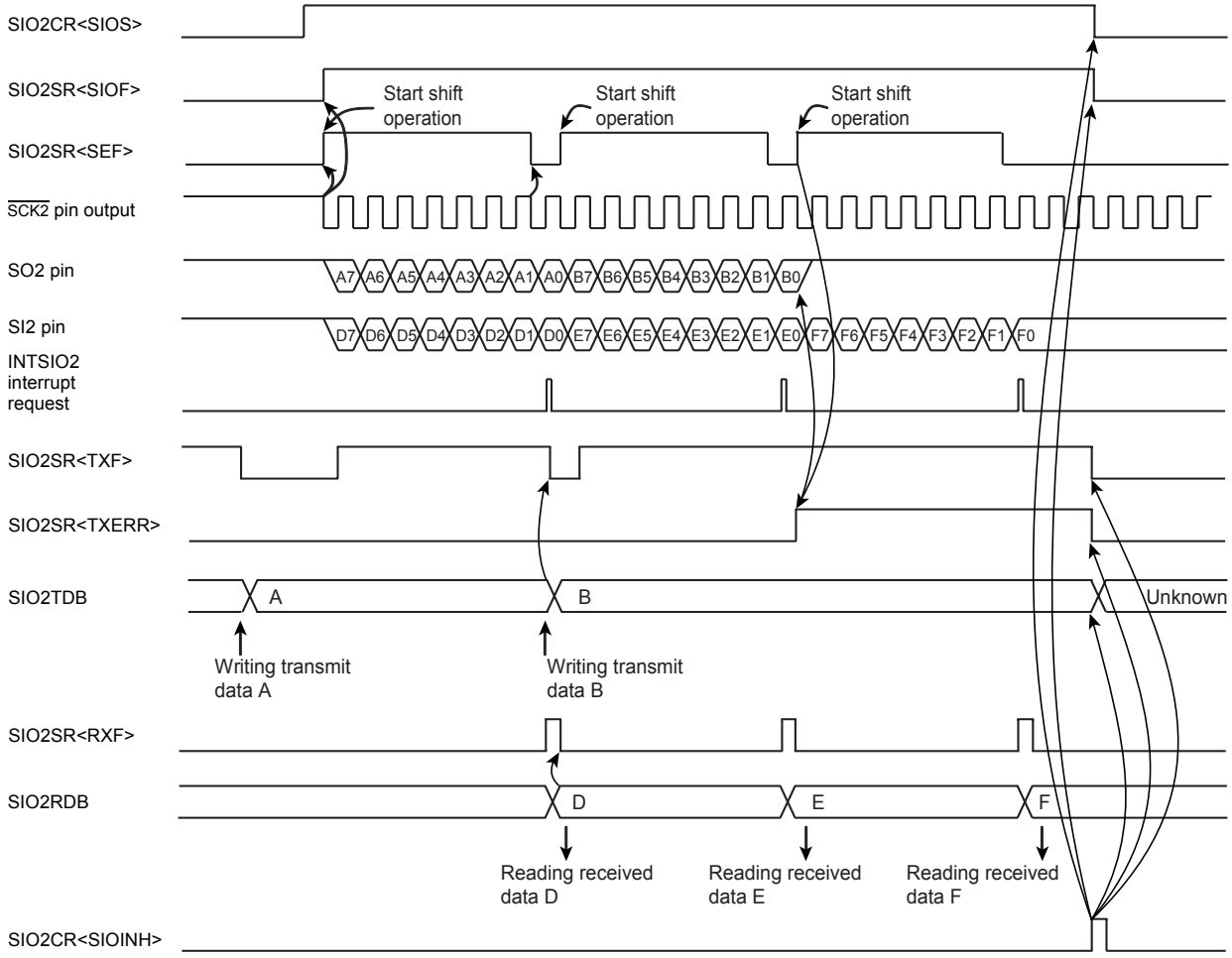


Figure 15-15 Example of Transmit/Receive (Transmit) Error Processing

(b) Receive errors

Receive errors occur on the following situation. To protect SIO2RDB and the shift register contents, the received data is ignored while the SIO2SR<RXERR> is "1".

- Shift operation is finished before reading out received data from SIO2RDB at SIO2SR<RXF> is "1" in an external clock operation.
  If receive error occurs, set the SIO2CR<SIOS> to "0" for reading the data that received immediately before error occurence. And read the data from SIO2RDB. Data in shift register (at errors occur) can be read by reading the SIO2RDB again.
  When SIO2SR<RXERR> is cleared to "0" after reading the received data, SIO2SR<RXF> is cleared to "0".
  After clearing SIO2CR<SIOS> to "0", when 8-bit serial clock is input to $\overline{\text{SCK2}}$ pin, receive operation is stopped. To restart the receive operation, confirm that SIO2SR<SIOF> is cleared to "0".
  If the received error occurs, set the SIO2CR<SIOINH> to "1" for stopping the receive operation immediately. In this case, SIO2CR<SIOS>, SIO2SR register, SIO2RDB register and SIO2TDB register are initialized.

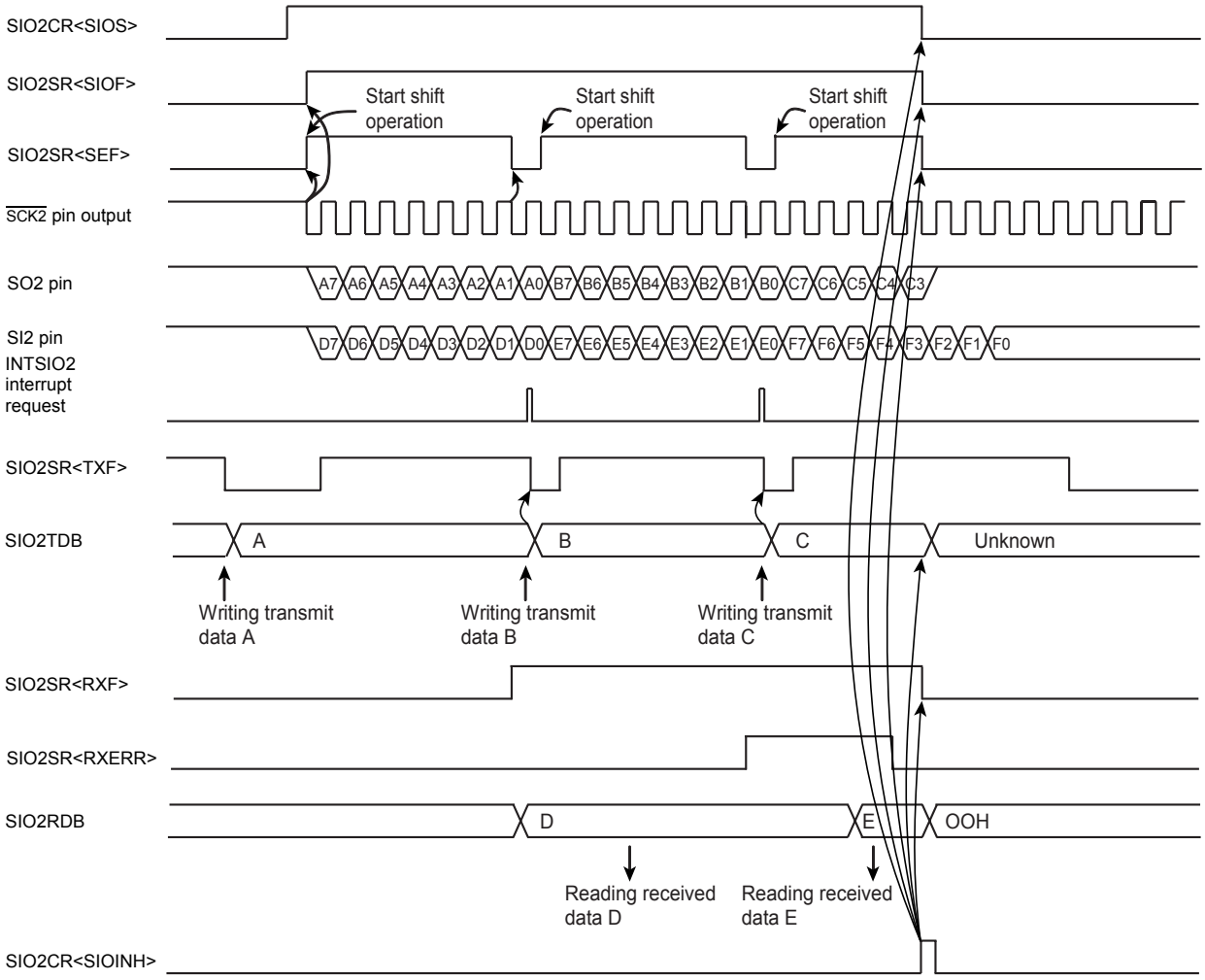


Figure 15-16 Example of Transmit/Receive (Receive) Error Processing

Note: If receive error is not corrected, an interrupt request does not generate after the error occurs.

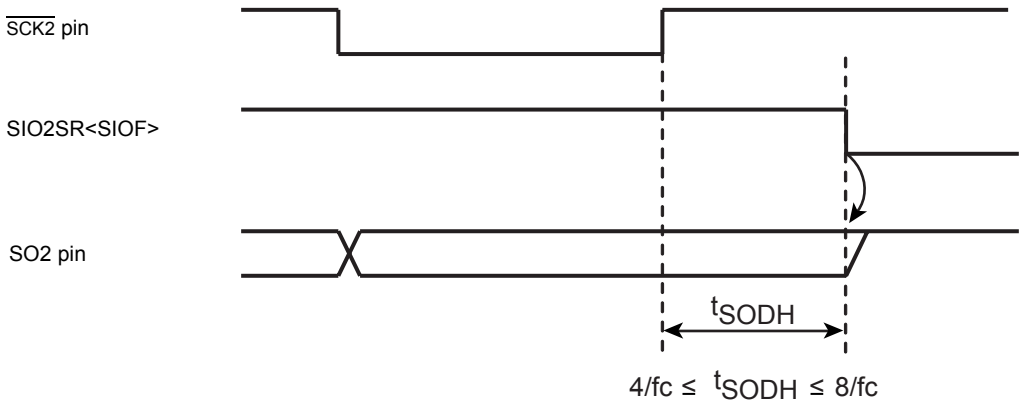


Figure 15-17 Hold Time of the End of Transmit/Receive Mode

16. Serial Bus Interface(I^2C Bus) Ver.-D (SBI)

The T5CL8 has a serial bus interface which employs an I^2C bus.

The serial interface is connected to an external devices through SDA and SCL.

The serial bus interface pins are also used as the port. When used as serial bus interface pins, set the output latches of these pins to "1". When not used as serial bus interface pins, the port is used as a normal I/O port.

Note 1: The serial bus interface can be used only in NORMAL1/2 and IDLE1/2 mode. It can not be used in IDLE0, SLOW1/2 and SLEEP0/1/2 mode.

Note 2: The serial bus interface can be used only in the Standard mode of I^2C. The fast mode and the high-speed mode can not be used.

Note 3: Please refer to the I/O port section about the detail of setting port.

16.1 Configuration

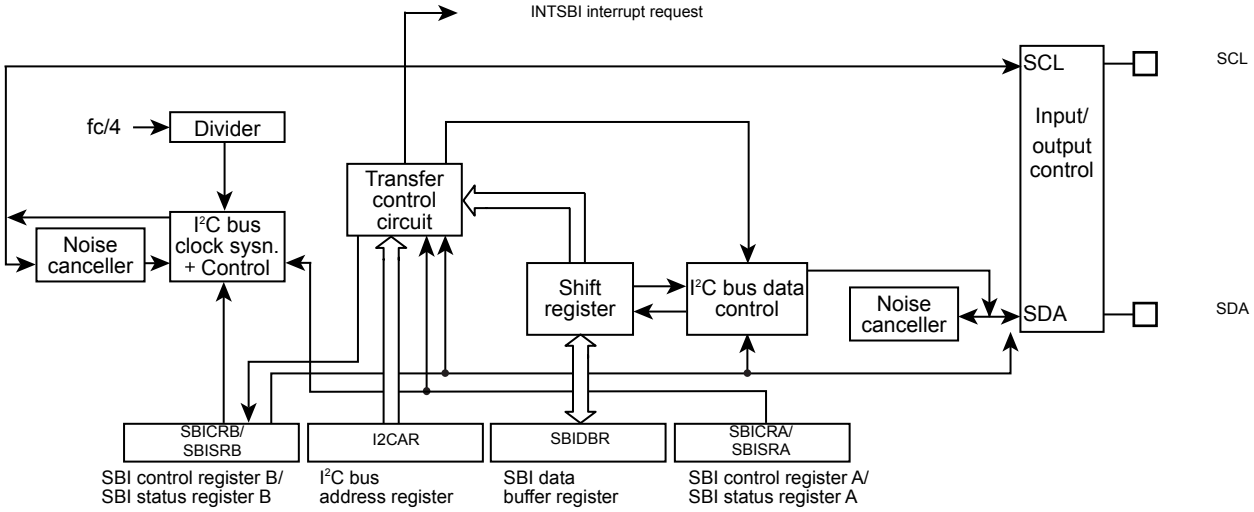


Figure 16-1 Serial Bus Interface (SBI)

16.2 Control

The following registers are used for control the serial bus interface and monitor the operation status.

- Serial bus interface control register A (SBICRA)
- Serial bus interface control register B (SBICRB)
- Serial bus interface data buffer register (SBIDBR)
- I^2C bus address register (I2CAR)
- Serial bus interface status register A (SBISRA)
- Serial bus interface status register B (SBISRB)

16.3 Software Reset

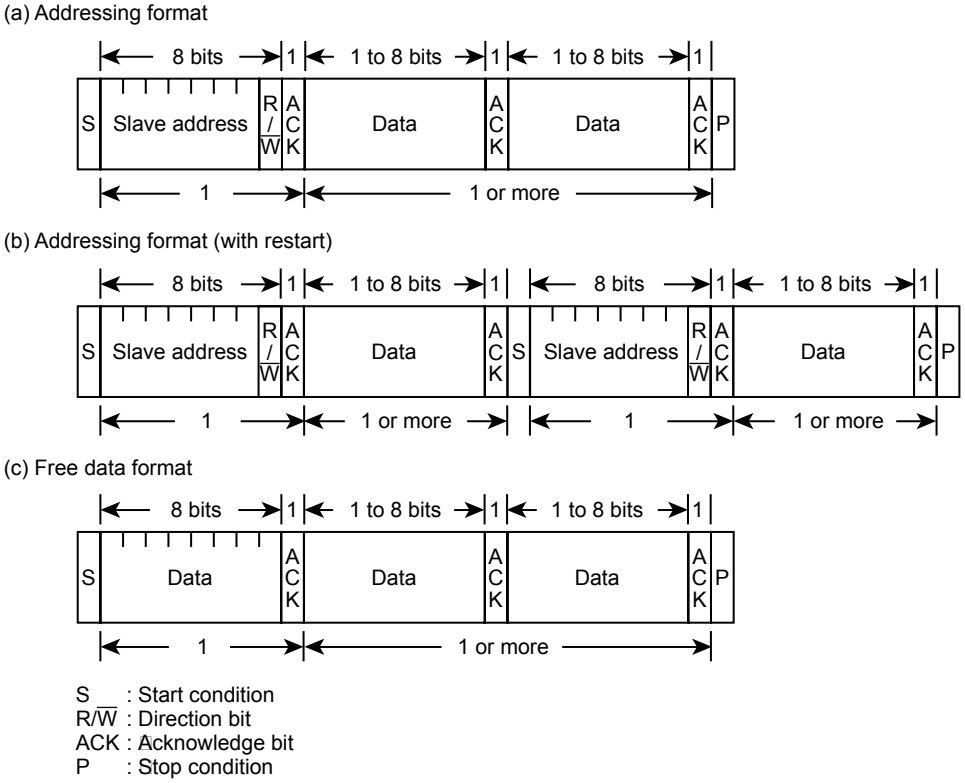
A serial bus interface circuit has a software reset function, when a serial bus interface circuit is locked by an external noise, etc.

To reset the serial bus interface circuit, write “10”, “01” into the SWRST (Bit1, 0 in SBICRB).

And a status of software reset canbe read from SWRMON (Bit0 in SBISRA).

16.4 The Data Format in the I^2C Bus Mode

The data format of the I^2C bus is shown below.



S : Start condition
R/$\overline{W}$: Direction bit
ACK : Acknowledge bit
P : Stop condition

Figure 16-2 Data Format in of I^2C Bus

16.5 I^2C Bus Control

The following registers are used to control the serial bus interface and monitor the operation status of the I^2C bus.

Serial Bus Interface Control Register A

SBICRA (0F90H)

7	6	5	4	3	2	1	0
BC			ACK		SCK		

(Initial value: 0000 *000)

		BC	ACK = 0		ACK = 1		
			Number of Clock	Bits	Number of Clock	Bits	
BC	Number of transferred bits	000:	8	8	9	8	Write only
		001:	1	1	2	1	
		010:	2	2	3	2	
		011:	3	3	4	3	
		100:	4	4	5	4	
		101:	5	5	6	5	
		110:	6	6	7	6	
		111:	7	7	8	7	
ACK	Acknowledgement mode specification	ACK	Master mode		Slave mode		R/W
		0:	Not generate a clock pulse for an acknowledgement.		Not count a clock pulse for an acknowledgement.		
		1:	Generate a clock pulse for an acknowledgement.		Count a clock pulse for an acknowledgement.		
SCK	Serial clock (fscl) selection (Output on SCL pin) [fscl = $1/(2^{n+1}/fc + 8/fc)$]	SCK	n	At fc = 16 MHz	At fc = 8 MHz	At fc = 4 MHz	Write only
		000:	4	Reserved	Reserved	100.0 kHz	
		001:	5	Reserved	Reserved	55.6 kHz	
		010:	6	Reserved	58.8 kHz	29.4 kHz	
		011:	7	60.6 kHz	30.3 kHz	15.2 kHz	
		100:	8	30.8 kHz	15.4 kHz	7.7 kHz	
		101:	9	15.5 kHz	7.8 kHz	3.9 kHz	
		110:	10	7.8 kHz	3.9 kHz	1.9 kHz	
		111:	Reserved				

Note 1: fc: High-frequency clock [Hz], *: Don't care

Note 2: SBICRA cannot be used with any of read-modify-write instructions such as bit manipulation, etc.

Note 3: Do not set SCK as the frequency that is over 100 kHz.

Serial Bus Interface Data Buffer Register

SBIDBR (0F91H)

7	6	5	4	3	2	1	0

(Initial value: **** ****) R/W

Note 1: For writing transmitted data, start from the MSB (Bit7).

Note 2: The data which was written into SBIDBR can not be read, since a write data buffer and a read buffer are independent in SBIDBR. Therefore, SBIDBR cannot be used with any of read-modify-write instructions such as bit manipulation, etc.

Note 3: *: Don't care

I^2C bus Address Register

I2CAR (0F92H)

7	6	5	4	3	2	1	0	
Slave address							ALS	(Initial value: 0000 0000)
SA6	SA5	SA4	SA3	SA2	SA1	SA0		

SA	Slave address selection		Write only
ALS	Address recognition mode specification	0: Slave address recognition 1: Non slave address recognition	

Note 1: I2CAR is write-only register, which cannot be used with any of read-modify-write instruction such as bit manipulation, etc.

Note 2: Do not set I2CAR to "00H" to avoid the incorrect response of acknowledgment in slave mode. (If "00H" is set to I2CAR as the Slave Address and a START Byte "01H" in I^2C bus standard is recived, the device detects slave address match.)

Serial Bus Interface Control Register B

SBICRB (0F93H)

7	6	5	4	3	2	1	0	
MST	TRX	BB	PIN	SBIM		SWRST1	SWRST0	(Initial value: 0001 0000)

MST	Master/slave selection	0: Slave 1: Master	Write only
TRX	Transmitter/receiver selection	0: Receiver 1: Transmitter	
BB	Start/stop generation	0: Generate a stop condition when MST, TRX and PIN are "1" 1: Generate a start condition when MST, TRX and PIN are "1"	
PIN	Cancel interrupt service request	0: – (Can not clear this bit by a software) 1: Cancel interrupt service request	
SBIM	Serial bus interface operating mode selection	00: Port mode (Serial bus interface output disable) 01: Reserved 10: I^2C bus mode 11: Reserved	
SWRST1 SWRST0	Software reset start bit	Software reset starts by first writing "10" and next writing "01"	

Note 1: Switch a mode to port after confirming that the bus is free.

Note 2: Switch a mode to I^2C bus mode after confiming that the port is high level.

Note 3: SBICRB has write-only register and must not be used with any of read-modify-write instructions such as bit manipulation, etc.

Note 4: When the SWRST (Bit1, 0 in SBICRB) is written to "10", "01" in I^2C bus mode, software reset is occurred. In this case, the SBICRA, I2CAR, SBISRA and SBISRB registers are initialized and the bits of SBICRB except the SBIM (Bit3, 2 in SBICRB) are also initialized.

Serial Bus Interface Status Register A

SBISRA (0F90H)

7	6	5	4	3	2	1	0	
							SWRMON	(Initial value: **** ***1)

SWRMON	Software reset monitor	0: During software reset 1: – (Initial value)	Read only

Serial Bus Interface Status Register B

SBISRB (0F93H)

7	6	5	4	3	2	1	0	
MST	TRX	BB	PIN	AL	AAS	AD0	LRB	(Initial value: 0001 0000)

MST	Master/slave selection status monitor	0: Slave 1: Master	Read only
TRX	Transmitter/receiver selection status monitor	0: Receiver 1: Transmitter	
BB	Bus status monitor	0: Bus free 1: Bus busy	
PIN	Interrupt service requests status monitor	0: Requesting interrupt service 1: Releasing interrupt service request	
AL	Arbitration lost detection monitor	0: – 1: Arbitration lost detected	
AAS	Slave address match detection monitor	0: - 1: Detect slave address match or "GENERAL CALL"	
AD0	"GENERAL CALL" detection monitor	0: - 1: Detect "GENERAL CALL"	
LRB	Last received bit monitor	0: Last receive bit is "0" 1: Last receiv bit is "1"	

16.5.1 Acknowledgement mode specification

16.5.1.1 Acknowledgment mode (ACK = “1”)

To set the device as an acknowledgment mode, the ACK (Bit4 in SBICRA) should be set to “1”. When a serial bus interface circuit is a master mode, an additional clock pulse is generated for an acknowledge signal. In a slave mode, a clock is counted for the acknowledge signal.

In the master transmitter mode, the SDA pin is released in order to receive an acknowledge signal from the receiver during additional clock pulse cycle. In the master receiver mode, the SDA pin is set to low level generation an acknowledge signal during additional clock pulse cycle.

In a slave mode, when a received slave address matches to a slave address which is set to the I2CAR or when a “GENERAL CALL” is received, the SDA pin is set to low level generating an acknowledge signal. After the matching of slave address or the detection of “GENERAL CALL”, in the transmitter, the SDA pin is released in order to receive an acknowledge signal from the receiver during additional clock pulse cycle. In a receiver, the SDA pin is set to low level generation an acknowledge signal during additional clock pulse cycle after the matching of slave address or the detection of “GENERAL CALL”

The Table 16-1 shows the SCL and SDA pins status in acknowledgment mode.

Table 16-1 SCL and SDA Pins Status in Acknowledgement Mode

Mode	Pin		Transmitter	Receiver
Master	SCL		An additional clock pulse is generated.	
	SDA		Released in order to receive an acknowledge signal.	Set to low level generating an acknowledge signal
Slave	SCL		A clock is counted for the acknowledge signal.	
	SDA	When slave address matches or a general call is detected	–	Set to low level generating an acknowledge signal.
		After matching of slave address or general call	Released in order to receive an acknowledge signal.	Set to low level generating an acknowledge signal.

16.5.1.2 Non-acknowledgment mode (ACK = “0”)

To set the device as a non-acknowledgement mode, the ACK (Bit4 in SBICRA) should be cleared to “0”.

In the master mode, a clock pulse for an acknowledge signal is not generated.

In the slave mode, a clock for a acknowledge signal is not counted.

16.5.2 Number of transfer bits

The BC (Bits7 to 5 in SBICRA) is used to select a number of bits for next transmitting and receiving data.

Since the BC is cleared to "000" by a start condition, a slave address and direction bit transmissions are always executed in 8 bits. Other than these, the BC retains a specified value.

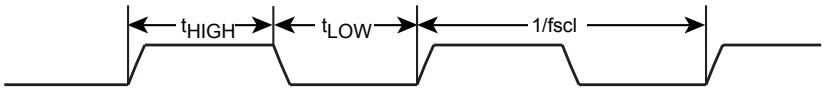
16.5.3 Serial clock

16.5.3.1 Clock source

The SCK (Bits2 to 0 in SBICRA) is used to select a maximum transfer frequency output from the SCL pin in the master mode.

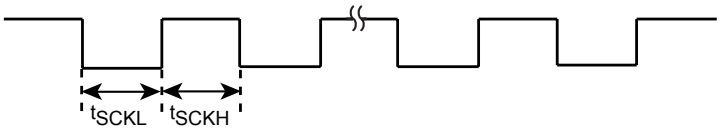
Four or more machine cycles are required for both high and low levels of pulse width in the external clock which is input from SCL pin.

Note: Since the serial bus interface can not be used as the fast mode and the high-speed mode, do not set SCK as the frequency that is over 100 kHz.



$t_{LOW} = 2^n/fc$
$t_{HIGH} = 2^n/fc + 8/fc$
$fscl = 1/(t_{LOW} + t_{HIGH})$

SCK (Bits2 to 0 in the SBICRA)	n
000	4
001	5
010	6
011	7
100	8
101	9
110	10



t_{SCKL}, t_{SCKH} > 4 tcyc

Note 1: fc = High-frequency clock
Note 2: tcyc = 4/fc (in NORMAL mode, IDLE mode)

Figure 16-3 Clock Source

16.5.3.2 Clock synchronization

In the I^2C bus, in order to drive a bus with a wired AND, a master device which pulls down a clock pulse to low will, in the first place, invalidate a clock pulse of another master device which generates a high-level clock pulse.

The serial bus interface circuit has a clock synchronization function. This function ensures normal transfer even if there are two or more masters on the same bus.

The example explains clock synchronization procedures when two masters simultaneously exist on a bus.

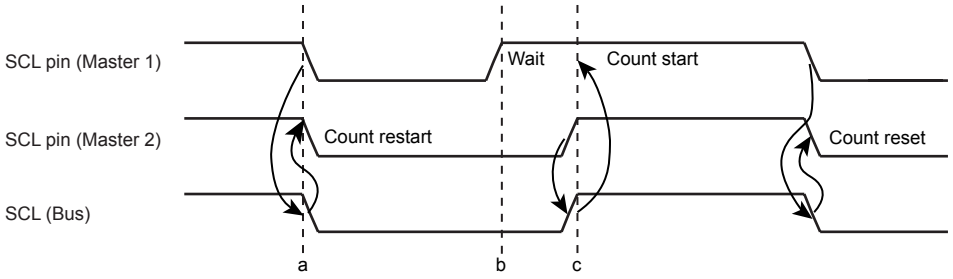


Figure 16-4 Clock Synchronization

As Master 1 pulls down the SCL pin to the low level at point “a”, the SCL line of the bus becomes the low level. After detecting this situation, Master 2 resets counting a clock pulse in the high level and sets the SCL pin to the low level.

Master 1 finishes counting a clock pulse in the low level at point “b” and sets the SCL pin to the high level. Since Master 2 holds the SCL line of the bus at the low level, Master 1 waits for counting a clock pulse in the high level. After Master 2 sets a clock pulse to the high level at point “c” and detects the SCL line of the bus at the high level, Master 1 starts counting a clock pulse in the high level. Then, the master, which has finished the counting a clock pulse in the high level, pulls down the SCL pin to the low level.

The clock pulse on the bus is determined by the master device with the shortest high-level period and the master device with the longest low-level period from among those master devices connected to the bus.

16.5.4 Slave address and address recognition mode specification

When the serial bus interface circuit is used with an addressing format to recognize the slave address, clear the ALS (Bit0 in I2CAR) to “0”, and set the SA (Bits7 to 1 in I2CAR) to the slave address.

When the serial bus interface circuit is used with a free data format not to recognize the slave address, set the ALS to “1”. With a free data format, the slave address and the direction bit are not recognized, and they are processed as data from immediately after start condition.

16.5.5 Master/slave selection

To set a master device, the MST (Bit7 in SBICRB) should be set to “1”. To set a slave device, the MST should be cleared to “0”.

When a stop condition on the bus or an arbitration lost is detected, the MST is cleared to “0” by the hardware.

16.5.6 Transmitter/receiver selection

To set the device as a transmitter, the TRX (Bit6 in SBICRB) should be set to "1". To set the device as a receiver, the TRX should be cleared to “0”. When data with an addressing format is transferred in the slave mode, the TRX is set to "1" by a hardware if the direction bit (R/$\overline{W}$) sent from the master device is “1”, and is cleared to “0” by a hardware if the bit is “0”. In the master mode, after an acknowledge signal is returned from the slave device, the TRX is cleared to “0” by a hardware if a transmitted direction bit is “1”, and is set to "1" by a hardware if it is “0”. When an acknowledge signal is not returned, the current condition is maintained.

When a stop condition on the bus or an arbitration lost is detected, the TRX is cleared to “0” by the hardware. " Table 16-2 TRX changing conditions in each mode " shows TRX changing conditions in each mode and TRX value after changing

Table 16-2 TRX changing conditions in each mode

Mode	Direction Bit	Conditions	TRX after Changing
Slave Mode	"0"	A received slave address is the same value set to I2CAR	"0"
	"1"		"1"
Master Mode	"0"	ACK signal is returned	"1"
	"1"		"0"

When a serial bus interface circuit operates in the free data format, a slave address and a direction bit are not recognized. They are handled as data just after generating a start condition. The TRX is not changed by a hardware.

16.5.7 Start/stop condition generation

When the BB (Bit5 in SBISRB) is “0”, a slave address and a direction bit which are set to the SBIDBR are output on a bus after generating a start condition by writing “1” to the MST, TRX, BB and PIN. It is necessary to set ACK to “1” beforehand.

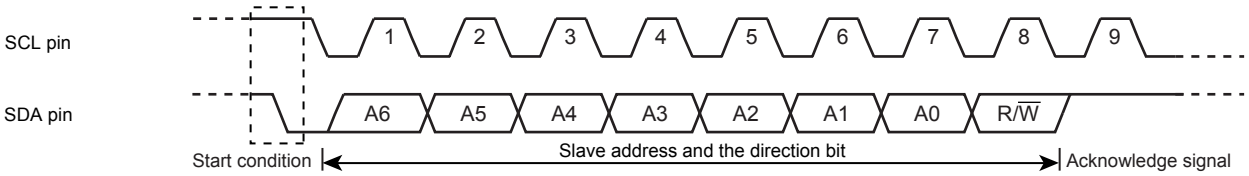


Figure 16-5 Start Condition Generation and Slave Address Generation

When the BB is “1”, sequence of generating a stop condition is started by writing “1” to the MST, TRX and PIN, and “0” to the BB. Do not modify the contents of MST, TRX, BB and PIN until a stop condition is generated on a bus.

When a stop condition is generated and the SCL line on a bus is pulled-down to low level by another device, a stop condition is generated after releasing the SCL line.

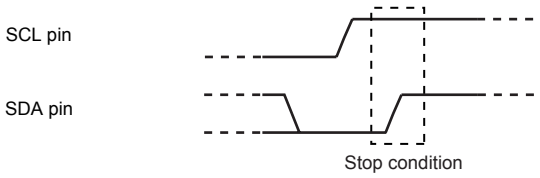


Figure 16-6 Stop Condition Generation

The bus condition can be indicated by reading the contents of the BB (Bit5 in SBISRB). The BB is set to “1” when a start condition on a bus is detected (Bus Busy State) and is cleared to “0” when a stop condition is detected (Bus Free State).

16.5.8 Interrupt service request and cancel

When a serial bus interface circuit is in the master mode and transferring a number of clocks set by the BC and the ACK is complete, a serial bus interface interrupt request (INTSBI) is generated.

In the slave mode, the conditions of generating INTSBI interrupt request are follows:

- At the end of acknowledge signal when the received slave address matches to the value set by the I2CAR
- At the end of acknowledge signal when a “GENERAL CALL” is received
- At the end of transferring or receiving after matching of slave address or receiving of “GENERAL CALL”

When a serial bus interface interrupt request occurs, the PIN (Bit4 in SBISRB) is cleared to “0”. During the time that the PIN is “0”, the SCL pin is pulled-down to low level.

Either writing data to SBIDBR or reading data from the SBIDBR sets the PIN to “1”.

The time from the PIN being set to “1” until the SCL pin is released takes t_{LOW}.

Although the PIN (Bit4 in SBICRB) can be set to “1” by the softrware, the PIN can not be cleared to “0” by the softrware.

Note: When the arbitration lost occurs, if the slave address sent from the other master devices is not match, the INTSBI interrupt request is generated. But the PIN is not cleared.

16.5.9 Setting of I^2C bus mode

The SBIM (Bit3 and 2 in SBICRB) is used to set I^2C bus mode.

Set the SBIM to “10” in order to set I^2C bus mode. Before setting of I^2C bus mode, confirm serial bus interface pins in a high level, and then, write “10” to SBIM. And switch a port mode after confirming that a bus is free.

16.5.10 Arbitration lost detection monitor

Since more than one master device can exist simultaneously on a bus, a bus arbitration procedure is implemented in order to guarantee the contents of transferred data.

Data on the SDA line is used for bus arbitration of the I^2C bus.

The following shows an example of a bus arbitration procedure when two master devices exist simultaneously on a bus. Master 1 and Master 2 output the same data until point “a”. After that, when Master 1 outputs “1” and Master 2 outputs “0”, since the SDA line of a bus is wired AND, the SDA line is pulled-down to the low level by Master 2. When the SCL line of a bus is pulled-up at point “b”, the slave device reads data on the SDA line, that is data in Master 2. Data transmitted from Master 1 becomes invalid. The state in Master 1 is called “arbitration lost”. A master device which loses arbitration releases the SDA pin and the SCL pin in order not to effect data transmitted from other masters with arbitration. When more than one master sends the same data at the first word, arbitration occurs continuously after the second word.

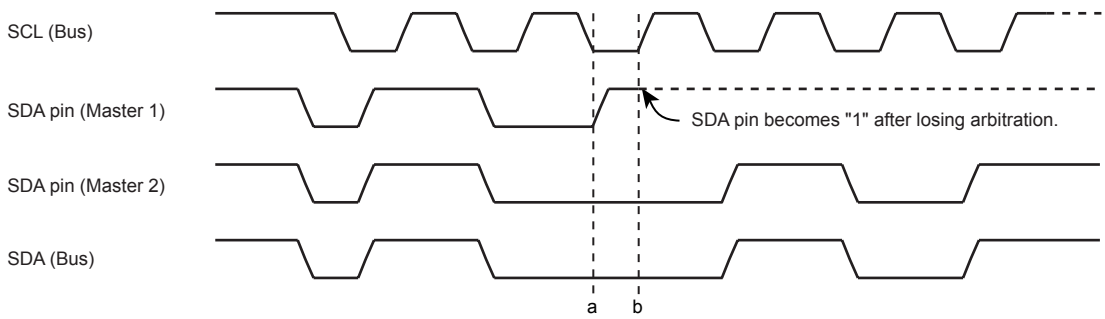


Figure 16-7 Arbitration Lost

The serial bus interface circuit compares levels of a SDA line of a bus with its SDA pin at the rising edge of the SCL line. If the levels are unmatched, arbitration is lost and the AL (Bit3 in SBISRB) is set to “1”.

When the AL is set to “1”, the MST and TRX are cleared to “0” and the mode is switched to a slave receiver mode. Thus, the serial bus interface circuit stops output of clock pulses during data transfer after the AL is set to “1”.

The AL is cleared to “0” by writing data to the SBIDBR, reading data from the SBIDBR or writing data to the SBICRB.

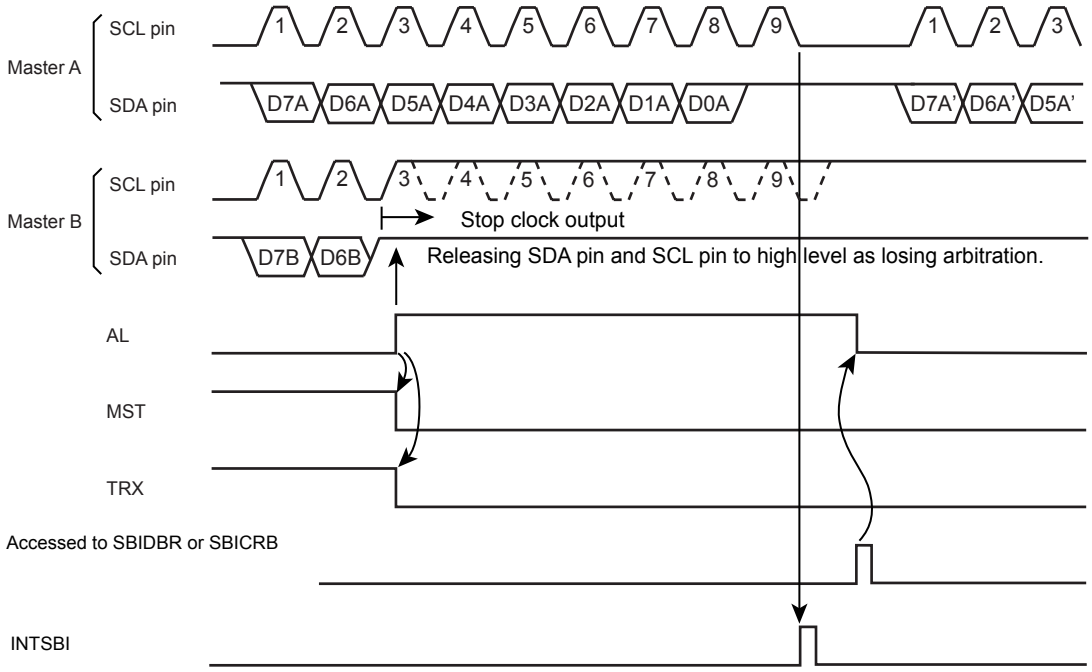

Master A
SCL pin
SDA pin
1 2 3 4 5 6 7 8 9 1 2 3
D7A D6A D5A D4A D3A D2A D1A D0A D7A' D6A' D5A'
Master B
SCL pin
SDA pin
1 2 3 4 5 6 7 8 9
Stop clock output
D7B D6B
Releasing SDA pin and SCL pin to high level as losing arbitration.
AL
MST
TRX
Accessed to SBIDBR or SBICRB
INTSBI

Figure 16-8 Example of when a Serial Bus Interface Circuit is a Master B

16.5.11 Slave address match detection monitor

In the slave mode, the AAS (Bit2 in SBISRB) is set to “1” when the received data is “GENERAL CALL” or the received data matches the slave address setting by I2CAR with an address recognition mode (ALS = 0).

When a serial bus interface circuit operates in the free data format (ALS = 1), the AAS is set to “1” after receiving the first 1-word of data.

The AAS is cleared to “0” by writing data to the SBIDBR or reading data from the SBIDBR.

16.5.12 GENERAL CALL detection monitor

The AD0 (Bit1 in SBISRB) is set to “1” when all 8-bit received data is “0” immediately after a start condition in a slave mode. The AD0 is cleared to “0” when a start or stop condition is detected on a bus.

16.5.13 Last received bit monitor

The SDA line value stored at the rising edge of the SCL line is set to the LRB (Bit0 in SBISRB). In the acknowledge mode, immediately after an INTSBI interrupt request is generated, an acknowledge signal is read by reading the contents of the LRB.

16.6 Data Transfer of I^2C Bus

16.6.1 Device initialization

For initialization of device, set the ACK in SBICRA to “1” and the BC to “000”. Specify the data length to 8 bits to count clocks for an acknowledge signal. Set a transfer frequency to the SCK in SBICRA.

Next, set the slave address to the SA in I2CAR and clear the ALS to “0” to set an addressing format.

After confirming that the serial bus interface pin is high level, for specifying the default setting to a slave receiver mode, clear “0” to the MST, TRX and BB in SBICRB, set “1” to the PIN, “10” to the SBIM, and “00” to bits SWRST1 and SWRST0.

Note: The initialization of a serial bus interface circuit must be complete within the time from all devices which are connected to a bus have initialized to and device does not generate a start condition. If not, the data can not be received correctly because the other device starts transferring before an end of the initialization of a serial bus interface circuit.

16.6.2 Start condition and slave address generation

Confirm a bus free status (BB = 0).

Set the ACK to “1” and specify a slave address and a direction bit to be transmitted to the SBIDBR.

By writing “1” to the MST, TRX, BB and PIN, the start condition is generated on a bus and then, the slave address and the direction bit which are set to the SBIDBR are output. The time from generating the START condition until the falling SCL pin takes t_{LOW}.

An INTSBI interrupt request occurs at the 9th falling edge of a SCL clock cycle, and the PIN is cleared to “0”. The SCL pin is pulled-down to the low level while the PIN is “0”. When an interrupt request occurs, the TRX changes by the hardware according to the direction bit only when an acknowledge signal is returned from the slave device.

Note 1: Do not write a slave address to be output to the SBIDBR while data is transferred. If data is written to the SBIDBR, data to been outputting may be destroyed.

Note 2: The bus free must be confirmed by software within 98.0 μs (The shortest transmitting time according to the I^2C bus standard) after setting of the slave address to be output. Only when the bus free is confirmed, set "1" to the MST, TRX, BB, and PIN to generate the start conditions. If the writing of slave address and setting of MST, TRX, BB and PIN doesn't finish within 98.0 μs, the other masters may start the transferring and the slave address data written in SBIDBR may be broken.

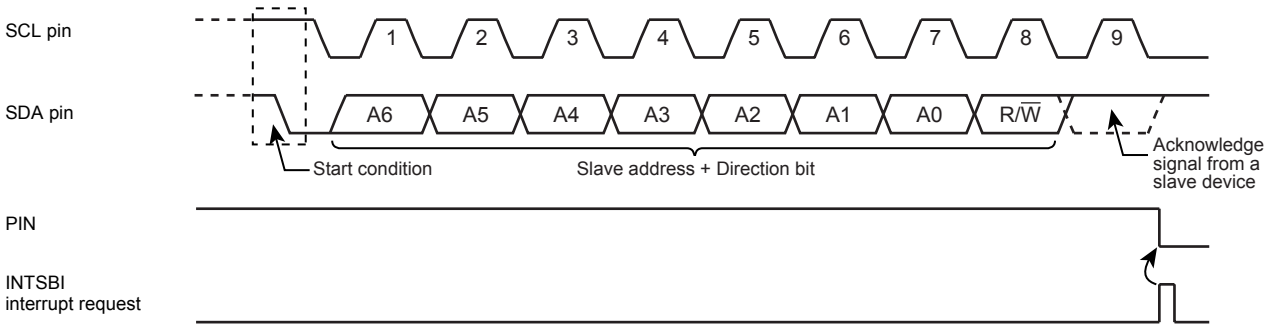


Figure 16-9 Start Condition Generation and Slave Address Transfer

16.6.3 1-word data transfer

Check the MST by the INTSBI interrupt process after an 1-word data transfer is completed, and determine whether the mode is a master or slave.

16.6.3.1 When the MST is “1” (Master mode)

Check the TRX and determine whether the mode is a transmitter or receiver.

(1) When the TRX is “1” (Transmitter mode)

Test the LRB. When the LRB is “1”, a receiver does not request data. Implement the process to generate a stop condition (Described later) and terminate data transfer.

When the LRB is “0”, the receiver requests next data. When the next transmitted data is other than 8 bits, set the BC, set the ACK to “1”, and write the transmitted data to the SBIDBR. After writing the data, the PIN becomes “1”, a serial clock pulse is generated for transferring a next 1 word of data from the SCL pin, and then the 1 word of data is transmitted. After the data is transmitted, and an INTSBI interrupt request occurs. The PIN become “0” and the SCL pin is set to low level. If the data to be transferred is more than one word in length, repeat the procedure from the LRB test above.

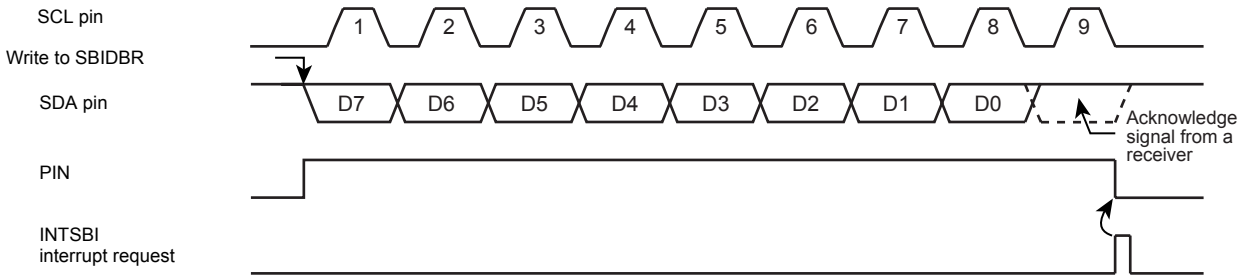


Figure 16-10 Example of when BC = “000”, ACK = “1”

(2) When the TRX is “0” (Receiver mode)

When the next transmitted data is other than of 8 bits, set the BC again. Set the ACK to “1” and read the received data from the SBIDBR (Reading data is undefined immediately after a slave address is sent). After the data is read, the PIN becomes “1”. A serial bus interface circuit outputs a serial clock pulse to the SCL pin to transfer next 1-word of data and sets the SDA pin to “0” at the acknowledge signal timing.

An INTSBI interrupt request occurs and the PIN becomes “0”. Then a serial bus interface circuit outputs a clock pulse for 1-word of data transfer and the acknowledge signal each time that received data is read from the SBIDBR.

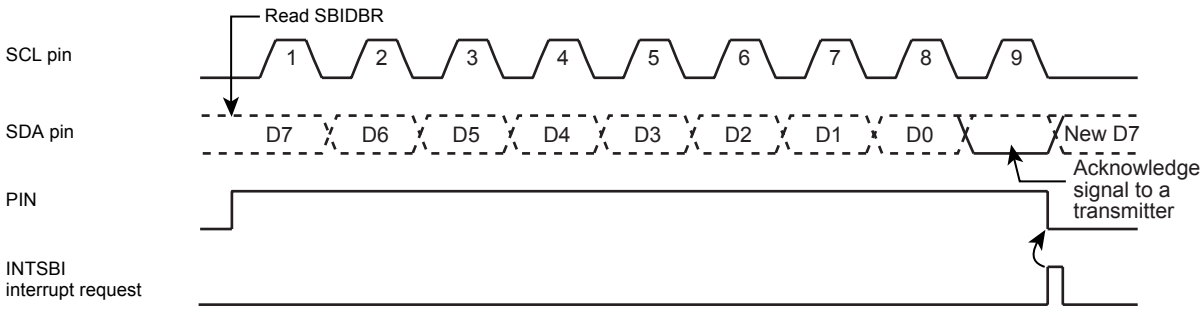


Figure 16-11 Example of when BC = “000”, ACK = “1”

To make the transmitter terminate transmit, clear the ACK to “0” before reading data which is 1-word before the last data to be received. A serial bus interface circuit does not generate a clock pulse for the acknowledge signal by clearing ACK. In the interrupt routine of end of transmission, when the BC is set to “001” and read the data, PIN is set to “1” and generates a clock pulse for a 1-bit data transfer. In this case, since the master device is a receiver, the SDA line on a bus keeps the high-level. The transmitter receives the high-level signal as an ACK signal. The receiver indicates to the transmitter that data transfer is complete.

After 1-bit data is received and an interrupt request has occurred, generate the stop condition to terminate data transfer.

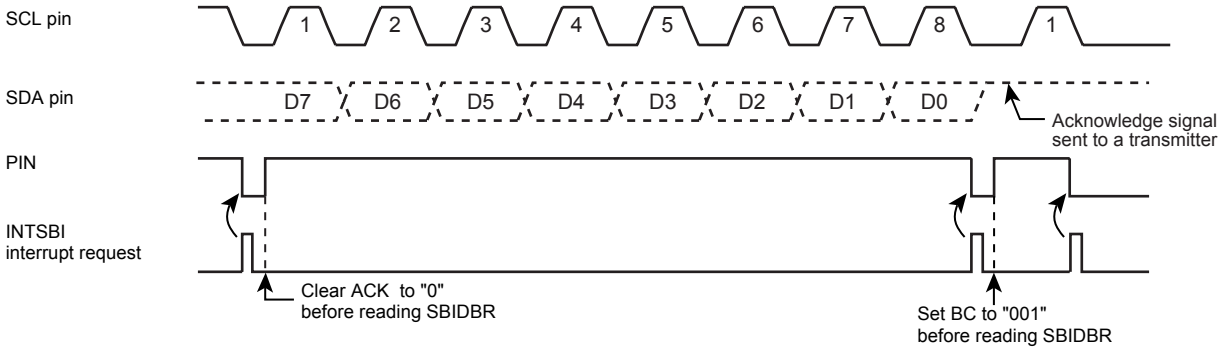


Figure 16-12 Termination of Data Transfer in Master Receiver Mode

16.6.3.2 When the MST is “0” (Slave mode)

In the slave mode, a serial bus interface circuit operates either in normal slave mode or in slave mode after losing arbitration.

In the slave mode, the conditions of generating INTSBI interrupt request are follows:

- At the end of acknowledge signal when the received slave address matches to the value set by the I2CAR
- At the end of acknowledge signal when a “GENERAL CALL” is received
- At the end of transferring or receiving after matching of slave address or receiving of “GENERAL CALL”

A serial bus interface circuit changes to a slave mode if arbitration is lost in the master mode. And an INTSBI interrupt request occurs when word data transfer terminates after losing arbitration. The behavior of INTSBI interrupt request and PIN after losing arbitration are shown in Table 16-3.

Table 16-3 The Behavior of INTSBI interrupt request and PIN after Losing Arbitration

	When the Arbitration Lost Occurs during Transmission of Slave Address as a Master	When the Arbitration Lost Occurs during Transmission of Data as a Master Transmit Mode
INTSBI interrupt request	INTSBI interrupt request is generated at the termination of word data.	
PIN	When the slave address matches the value set by I2CAR, the PIN is cleared to "0" by generating of INTSBI interrupt request. When the slave address doesn't match the value set by I2CAR, the PIN keeps "1".	PIN keeps "1" (PIN is not cleared to "0").

When an INTSBI interrupt request occurs, the PIN (bit 4 in the SBICRB) is reset, and the SCL pin is set to low level. Either reading or writing from or to the SBIDBR or setting the PIN to “1” releases the SCL pin after taking t_{LOW}.

Check the AL (Bit3 in the SBISRB), the TRX (Bit6 in the SBISRB), the AAS (Bit2 in the SBISRB), and the AD0 (Bit1 in the SBISRB) and implements processes according to conditions listed in " Table 16-4 Operation in the Slave Mode ".

Table 16-4 Operation in the Slave Mode

TRX	AL	AAS	AD0	Conditions	Process
1	1	1	0	A serial bus interface circuit loses arbitration when transmitting a slave address. And receives a slave address of which the value of the direction bit sent from another master is "1".	Set the number of bits in 1 word to the BC and write transmitted data to the SBIDBR.
	0	1	0	In the slave receiver mode, a serial bus interface circuit receives a slave address of which the value of the direction bit sent from the master is "1".	
		0	0	In the slave transmitter mode, 1-word data is transmitted.	Test the LRB. If the LRB is set to "1", set the PIN to "1" since the receiver does not request next data. Then, clear the TRX to "0" to release the bus. If the LRB is set to "0", set the number of bits in 1 word to the BC and write transmitted data to the SBIDBR since the receiver requests next data.
0	1	1	1/0	A serial bus interface circuit loses arbitration when transmitting a slave address. And receives a slave address of which the value of the direction bit sent from another master is "0" or receives a "GENERAL CALL".	Read the SBIDBR for setting the PIN to "1" (Reading dummy data) or write "1" to the PIN.
		0	0	A serial bus interface circuit loses arbitration when transmitting a slave address or data. And terminates transferring word data.	A serial bus interface circuit is changed to slave mode. To clear AL to "0", read the SBIDBR or write the data to SBIDBR.
	0	1	1/0	In the slave receiver mode, a serial bus interface circuit receives a slave address of which the value of the direction bit sent from the master is "0" or receives "GENERAL CALL".	Read the SBIDBR for setting the PIN to "1" (Reading dummy data) or write "1" to the PIN.
		0	1/0	In the slave receiver mode, a serial bus interface circuit terminates receiving of 1-word data.	Set the number of bits in 1-word to the BC and read received data from the SBIDBR.

Note: In the slave mode, if the slave address set in I2CAR is "00H", a START Byte "01H" in I^2C bus standard is recived, the device detects slave address match and the TRX is set to "1".

16.6.4 Stop condition generation

When the BB is “1”, a sequence of generating a stop condition is started by setting “1” to the MST, TRX and PIN, and clear “0” to the BB. Do not modify the contents of the MST, TRX, BB, PIN until a stop condition is generated on a bus.

When a SCL line on a bus is pulled-down by other devices, a serial bus interface circuit generates a stop condition after they release a SCL line.

The time from the releasing SCL line until the generating the STOP condition takes t_{LOW}.

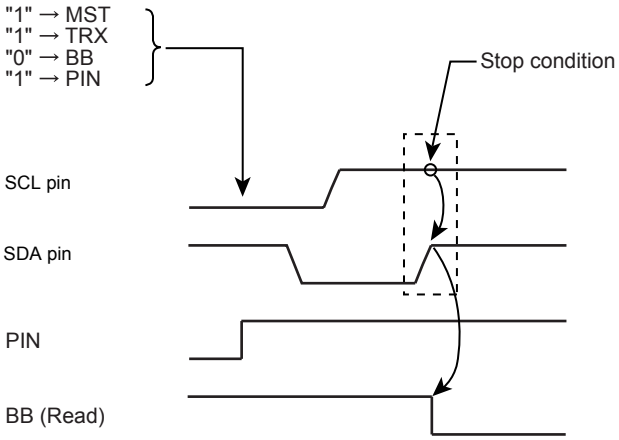


Figure 16-13 Stop Condition Generation

16.6.5 Restart

Restart is used to change the direction of data transfer between a master device and a slave device during transferring data. The following explains how to restart a serial bus interface circuit.

Clear “0” to the MST, TRX and BB and set “1” to the PIN. The SDA pin retains the high-level and the SCL pin is released. Since a stop condition is not generated on a bus, a bus is assumed to be in a busy state from other devices. Test the BB until it becomes “0” to check that the SCL pin of a serial bus interface circuit is released. Test the LRB until it becomes “1” to check that the SCL line on a bus is not pulled-down to the low level by other devices. After confirming that a bus stays in a free state, generate a start condition with procedure " 16.6.2 Start condition and slave address generation ".

In order to meet setup time when restarting, take at least 4.7 μs of waiting time by software from the time of restarting to confirm that a bus is free until the time to generate a start condition.

Note: When the master is in the receiver mode, it is necessary to stop the data transmission from the slave devcie before the STOP condtion is generated. To stop the transmission, the master device make the slave device receiving a negative acknowledge. Therefore, the LRB is "1" before generating the Restart and it can not be confirmed that SCL line is not pulled-down by other devices. Please confirm the SCL line state by reading the port.

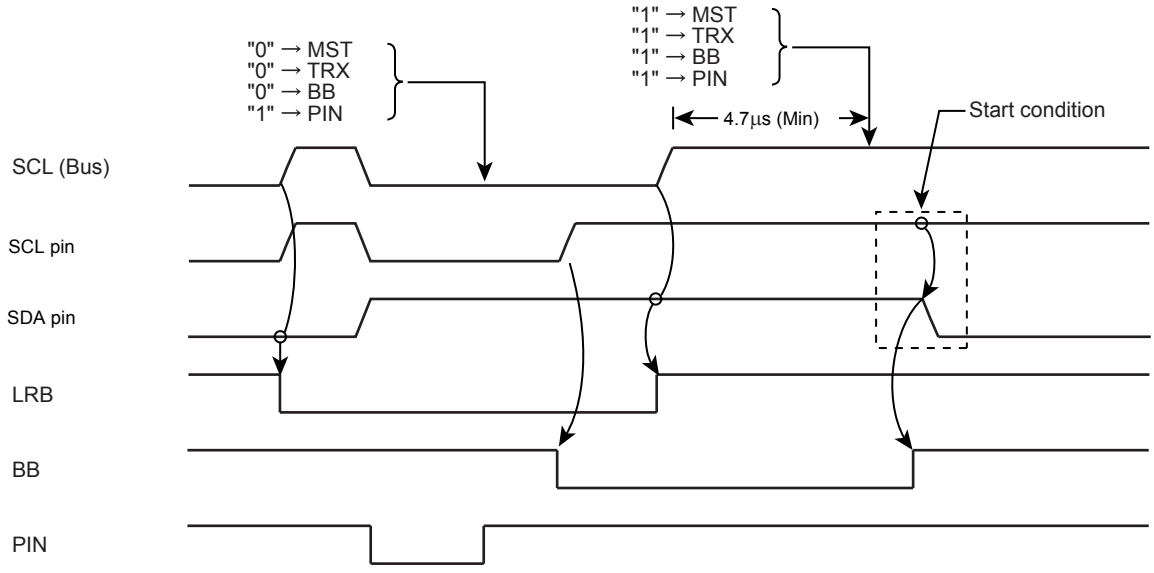


Figure 16-14 Timing Diagram when Restarting

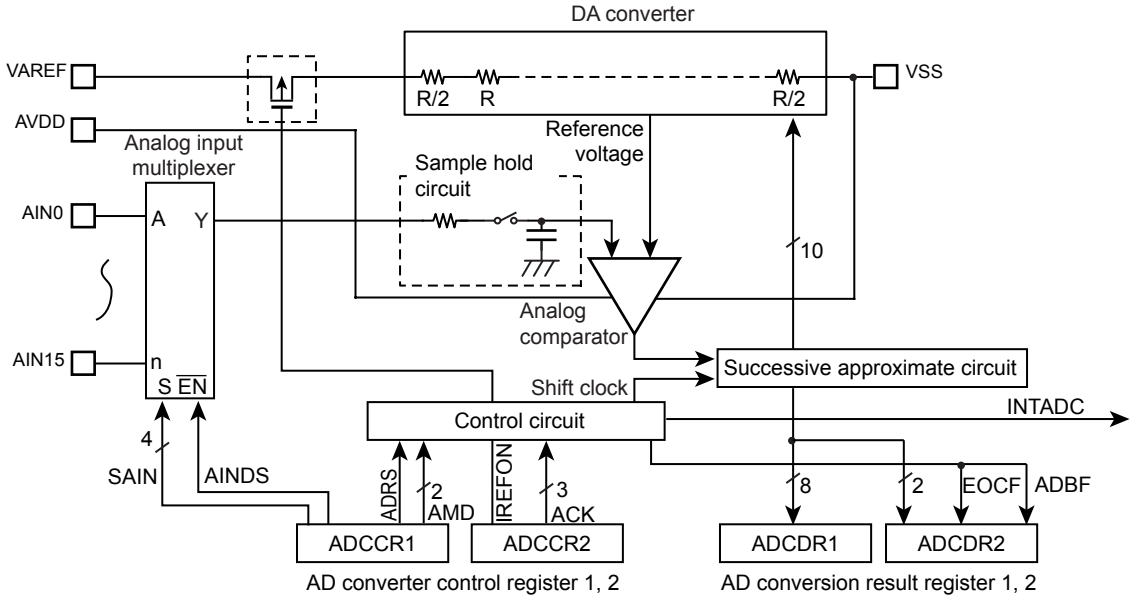
17. 10-bit AD Converter (ADC)

The T5CL8 have a 10-bit successive approximation type AD converter.

17.1 Configuration

The circuit configuration of the 10-bit AD converter is shown in Figure 17-1.

It consists of control register ADCCR1 and ADCCR2, converted value register ADCDR1 and ADCDR2, a DA converter, a sample-hold circuit, a comparator, and a successive comparison circuit.



Note: Before using AD converter, set appropriate value to I/O port register conbining a analog input port. For details, see the section on "I/O ports".

Figure 17-1 10-bit AD Converter

17.2 Register configuration

The AD converter consists of the following four registers:

1. AD converter control register 1 (ADCCR1)

   This register selects the analog channels and operation mode (Software start or repeat) in which to perform AD conversion and controls the AD converter as it starts operating.

2. AD converter control register 2 (ADCCR2)

   This register selects the AD conversion time and controls the connection of the DA converter (Ladder resistor network).

3. AD converted value register 1 (ADCDR1)

   This register used to store the digital value fter being converted by the AD converter.

4. AD converted value register 2 (ADCDR2)

   This register monitors the operating status of the AD converter.

AD Converter Control Register 1

ADCCR1 (001CH)

7	6	5	4	3	2	1	0
ADRS	AMD		AINDS	SAIN			

(Initial value: 0001 0000)

ADRS	AD conversion start	0: - 1: AD conversion start	R/W
AMD	AD operating mode	00: AD operation disable 01: Software start mode 10: Reserved 11: Repeat mode	
AINDS	Analog input control	0: Analog input enable 1: Analog input disable	
SAIN	Analog input channel select	0000: AIN0 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 1000: AIN8 1001: AIN9 1010: AIN10 1011: AIN11 1100: AIN12 1101: AIN13 1110: AIN14 1111: AIN15	

Note 1: Select analog input channel during AD converter stops (ADCDR2<ADBF> = "0").

Note 2: When the analog input channel is all use disabling, the ADCCR1<AINDS> should be set to "1".

Note 3: During conversion, Do not perform port output instruction to maintain a precision for all of the pins because analog input port use as general input port. And for port near to analog input, Do not input intense signaling of change.

Note 4: The ADCCR1<ADRS> is automatically cleared to "0" after starting conversion.

Note 5: Do not set ADCCR1<ADRS> newly again during AD conversion. Before setting ADCCR1<ADRS> newly again, check ADCDR2<EOCF> to see that the conversion is completed or wait until the interrupt signal (INTADC) is generated (e.g., interrupt handling routine).

Note 6: After STOP or SLOW/SLEEP mode are started, AD converter control register1 (ADCCR1) is all initialized and no data can be written in this register. Therfore, to use AD converter again, set the ADCCR1 newly after returning to NORMAL1 or NORMAL2 mode.

AD Converter Control Register 2

ADCCR2 (001DH)	7	6	5	4	3	2	1	0	
			IREFON	"1"	ACK			"0"	(Initial value: **0* 000*)

IREFON	DA converter (Ladder resistor) connection control	0: Connected only during AD conversion 1: Always connected	R/W
ACK	AD conversion time select (Refer to the following table about the conversion time)	000: 39/fc 001: Reserved 010: 78/fc 011: 156/fc 100: 312/fc 101: 624/fc 110: 1248/fc 111: Reserved	

Note 1: Always set bit0 in ADCCR2 to "0" and set bit4 in ADCCR2 to "1".

Note 2: When a read instruction for ADCCR2, bit6 to 7 in ADCCR2 read in as undefined data.

Note 3: After STOP or SLOW/SLEEP mode are started, AD converter control register2 (ADCCR2) is all initialized and no data can be written in this register. Therfore, to use AD converter again, set the ADCCR2 newly after returning to NORMAL1 or NORMAL2 mode.

Table 17-1 ACK setting and Conversion time

Condition / ACK	Conversion time	16 MHz	8 MHz	4 MHz	2 MHz	10 MHz	5 MHz	2.5 MHz
000	39/fc	-	-	-	19.5 μs	-	-	15.6 μs
001	Reserved							
010	78/fc	-	-	19.5 μs	39.0 μs	-	15.6 μs	31.2 μs
011	156/fc	-	19.5 μs	39.0 μs	78.0 μs	15.6 μs	31.2 μs	62.4 μs
100	312/fc	19.5 μs	39.0 μs	78.0 μs	156.0 μs	31.2 μs	62.4 μs	124.8 μs
101	624/fc	39.0 μs	78.0 μs	156.0 μs	-	62.4 μs	124.8 μs	-
110	1248/fc	78.0 μs	156.0 μs	-	-	124.8 μs	-	-
111	Reserved							

Note 1: Setting for "–" in the above table are inhibited. fc: High Frequency oscillation clock [Hz]

Note 2: Set conversion time setting should be kept more than the following time by Analog reference voltage (VAREF) .

- VAREF = 4.5 to 5.5 V 15.6 μs and more
- VAREF = 2.7 to 5.5 V 31.2 μs and more

AD Converted value Register 1

ADCDR1 (001FH)	7	6	5	4	3	2	1	0	
	AD09	AD08	AD07	AD06	AD05	AD04	AD03	AD02	(Initial value: 0000 0000)

AD Converted value Register 2

ADCDR2 (001EH)	7	6	5	4	3	2	1	0	
	AD01	AD00	EOCF	ADBF					(Initial value: 0000 ****)

EOCF	AD conversion end flag	0: Before or during conversion 1: Conversion completed	Read only
ADBF	AD conversion BUSY flag	0: During stop of AD conversion 1: During AD conversion	

Note 1: The ADCDR2<EOCF> is cleared to "0" when reading the ADCDR1. Therfore, the AD conversion result should be read to ADCDR2 more first than ADCDR1.

Note 2: The ADCDR2<ADBF> is set to "1" when AD conversion starts, and cleared to "0" when AD conversion finished. It also is cleared upon entering STOP mode or SLOW mode .

Note 3: If a read instruction is executed for ADCDR2, read data of bit3 to bit0 are unstable.

17.3 Function

17.3.1 Software Start Mode

After setting ADCCR1<AMD> to “01” (software start mode), set ADCCR1<ADRS> to “1”. AD conversion of the voltage at the analog input pin specified by ADCCR1<SAIN> is thereby started.

After completion of the AD conversion, the conversion result is stored in AD converted value registers (ADCDR1, ADCDR2) and at the same time ADCDR2<EOCF> is set to 1, the AD conversion finished interrupt (INTADC) is generated.

ADRS is automatically cleared after AD conversion has started. Do not set ADCCR1<ADRS> newly again (Restart) during AD conversion. Before setting ADRS newly again, check ADCDR2<EOCF> to see that the conversion is completed or wait until the interrupt signal (INTADC) is generated (e.g., interrupt handling routine).

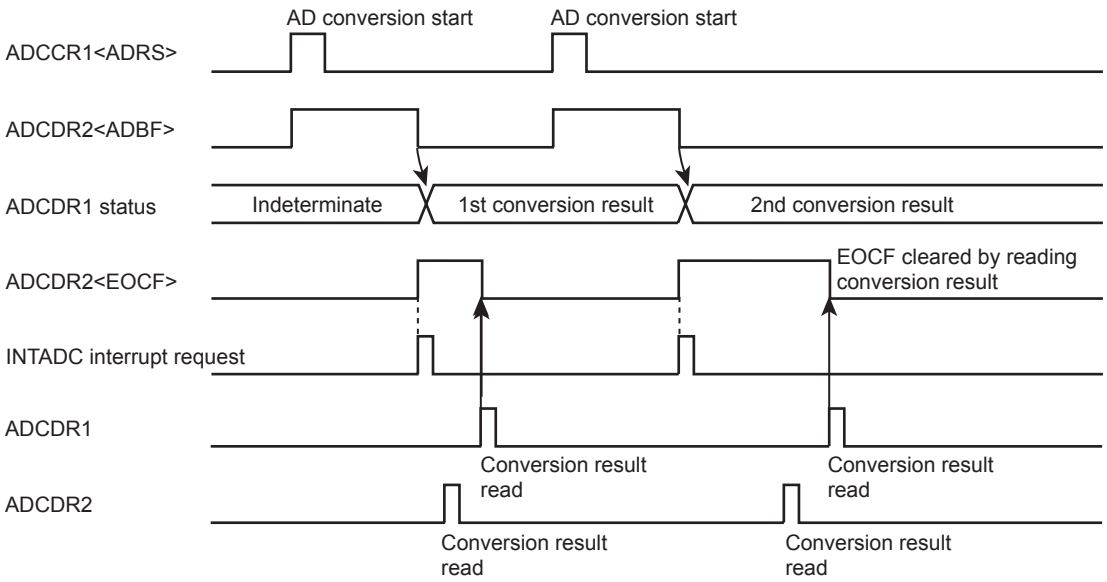


Figure 17-2 Software Start Mode

17.3.2 Repeat Mode

AD conversion of the voltage at the analog input pin specified by ADCCR1<SAIN> is performed repeatedly. In this mode, AD conversion is started by setting ADCCR1<ADRS> to “1” after setting ADCCR1<AMD> to “11” (Repeat mode).

After completion of the AD conversion, the conversion result is stored in AD converted value registers (ADCDR1, ADCDR2) and at the same time ADCDR2<EOCF> is set to 1, the AD conversion finished interrupt (INTADC) is generated.

In repeat mode, each time one AD conversion is completed, the next AD conversion is started. To stop AD conversion, set ADCCR1<AMD> to “00” (Disable mode) by writing 0s. The AD convert operation is stopped immediately. The converted value at this time is not stored in the AD converted value register.

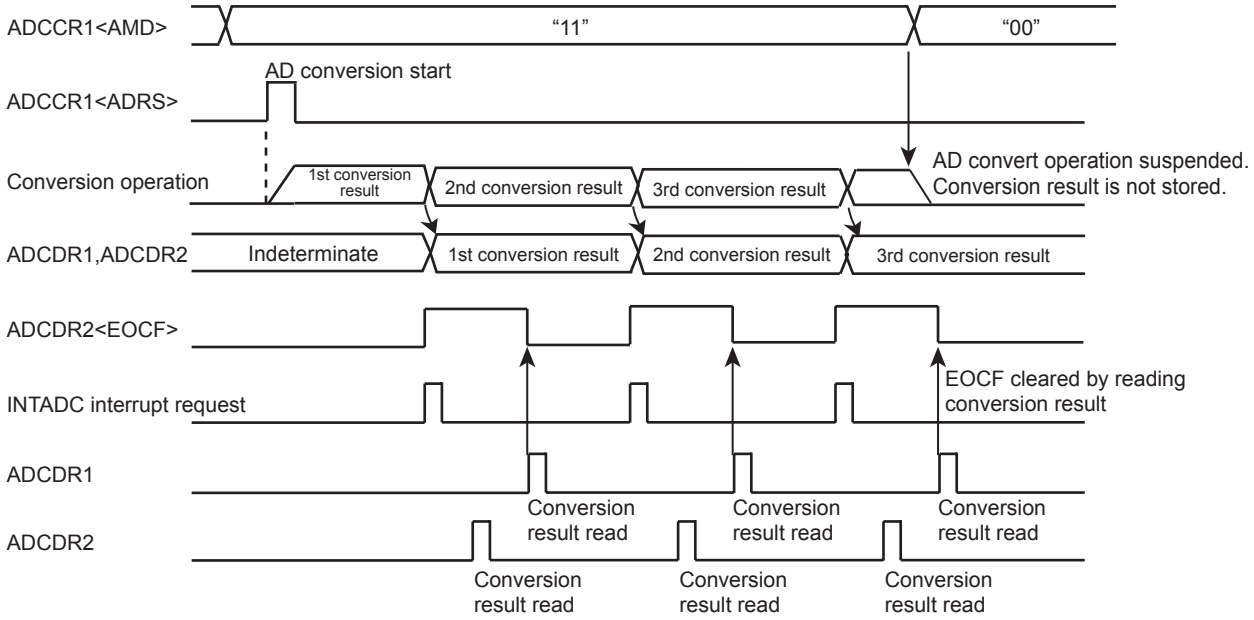


Figure 17-3 Repeat Mode

17.3.3 Register Setting

1. Set up the AD converter control register 1 (ADCCR1) as follows:
   - Choose the channel to AD convert using AD input channel select (SAIN).
   - Specify analog input enable for analog input control (AINDS).
   - Specify AMD for the AD converter control operation mode (software or repeat mode).
2. Set up the AD converter control register 2 (ADCCR2) as follows:
   - Set the AD conversion time using AD conversion time (ACK). For details on how to set the conversion time, refer to Figure 17-1 and AD converter control register 2.
   - Choose IREFON for DA converter control.
3. After setting up (1) and (2) above, set AD conversion start (ADRS) of AD converter control register 1 (ADCCR1) to "1". If software start mode has been selected, AD conversion starts immediately.
4. After an elapse of the specified AD conversion time, the AD converted value is stored in AD converted value register 1 (ADCDR1) and the AD conversion finished flag (EOCF) of AD converted value register 2 (ADCDR2) is set to "1", upon which time AD conversion interrupt INTADC is generated.
5. EOCF is cleared to "0" by a read of the conversion result. However, if reconverted before a register read, although EOCF is cleared the previous conversion result is retained until the next conversion is completed.

Example :After selecting the conversion time 19.5 μs at 16 MHz and the analog input channel AIN3 pin, perform AD conversion once. After checking EOCF, read the converted value, store the lower 2 bits in address 0009EH nd store the upper 8 bits in address 0009FH in RAM. The operation mode is software start mode.

```
                : (port setting)      :                      ;Set port register approrriately before setting AD
                                                             converter registers.
                :                     :                      (Refer to section I/O port in details)
                LD                    (ADCCR1) ,  00100011B  ; Select AIN3
                LD                    (ADCCR2) ,  11011000B  ;Select conversion time(312/fc) and operation
                                                             mode

                SET                   (ADCCR1) . 7           ; ADRS = 1(AD conversion start)
SLOOP :         TEST                  (ADCDR2) . 5           ; EOCF= 1 ?
                JRS                   T, SLOOP

                LD                    A , (ADCDR2)           ; Read result data
                LD                    (9EH) , A
                LD                    A , (ADCDR1)           ; Read  result data
                LD                    (9FH), A
```

17.4 STOP/SLOW Modes during AD Conversion

When standby mode (STOP or SLOW mode) is entered forcibly during AD conversion, the AD convert operation is suspended and the AD converter is initialized (ADCCR1 and ADCCR2 are initialized to initial value). Also, the conversion result is indeterminate. (Conversion results up to the previous operation are cleared, so be sure to read the conversion results before entering standby mode (STOP or SLOW mode).) When restored from standby mode (STOP or SLOW mode), AD conversion is not automatically restarted, so it is necessary to restart AD conversion. Note that since the analog reference voltage is automatically disconnected, there is no possibility of current flowing into the analog reference voltage.

17.5 Analog Input Voltage and AD Conversion Result

The analog input voltage is corresponded to the 10-bit digital value converted by the AD as shown in Figure 17-4.

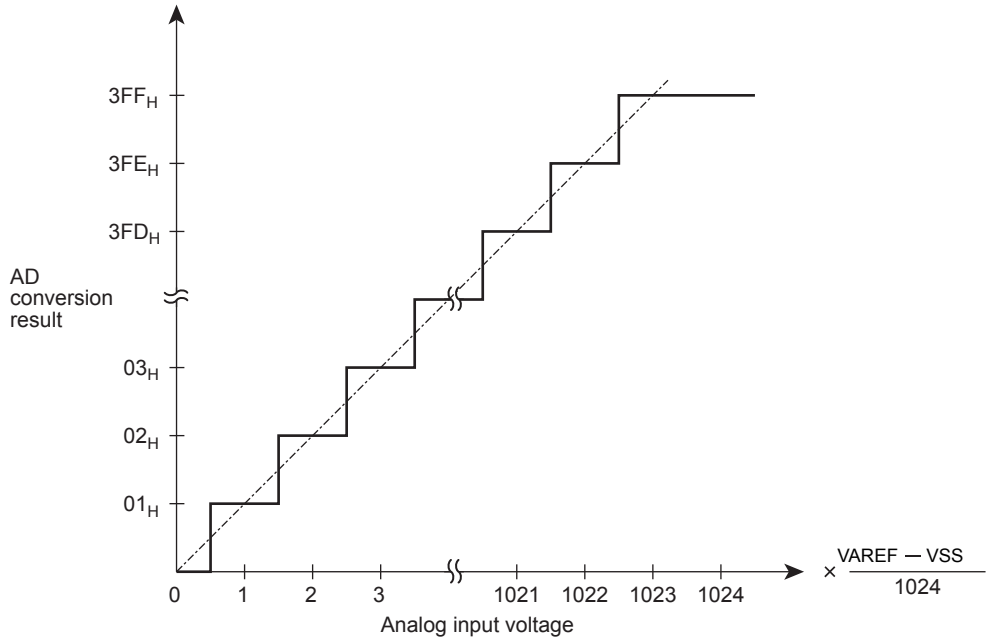


Figure 17-4 Analog Input Voltage and AD Conversion Result (Typ.)

17.6 Precautions about AD Converter

17.6.1 Restrictions for AD Conversion interrupt (INTADC) usage

When an AD interrupt is used, it may not be processed depending on program composition. For example, if an INTADC interrupt request is generated while an interrupt with priority lower than the interrupt latch IL15 (INTADC) is being accepted, the INTADC interrupt latch may be cleared without the INTADC interrupt being processed.

The completion of AD conversion can be detected by the following methods:

(1) Method not using the AD conversion end interrupt

Whether or not AD conversion is completed can be detected by monitoring the AD conversion end flag (EOCF) by software. This can be done by polling EOCF or monitoring EOCF at regular intervals after start of AD conversion.

(2) Method for detecting AD conversion end while a lower-priority interrupt is being processed

While an interrupt with priority lower than INTADC is being processed, check the AD conversion end flag (EOCF) and interrupt latch IL15. If IL15 = 0 and EOCF = 1, call the AD conversion end interrupt processing routine with consideration given to PUSH/POP operations. At this time, if an interrupt request with priority higher than INTADC has been set, the AD conversion end interrupt processing routine will be executed first against the specified priority. If necessary, we recommend that the AD conversion end interrupt processing routine be called after checking whether or not an interrupt request with priority higher than INTADC has been set.

17.6.2 Analog input pin voltage range

Make sure the analog input pins (AIN0 to AIN15) are used at voltages within VAREF to VSS. If any voltage outside this range is applied to one of the analog input pins, the converted value on that pin becomes uncertain. The other analog input pins also are affected by that.

17.6.3 Analog input shared pins

The analog input pins (AIN0 to AIN15) are shared with input/output ports. When using any of the analog inputs to execute AD conversion, do not execute input/output instructions for all other ports. This is necessary to prevent the accuracy of AD conversion from degrading. Not only these analog input shared pins, some other pins may also be affected by noise arising from input/output to and from adjacent pins.

17.6.4 Noise Countermeasure

The internal equivalent circuit of the analog input pins is shown in Figure 17-5. The higher the output impedance of the analog input source, more easily they are susceptible to noise. Therefore, make sure the output impedance of the signal source in your design is 5 kΩ or less. Toshiba also recommends attaching a capacitor external to the chip.

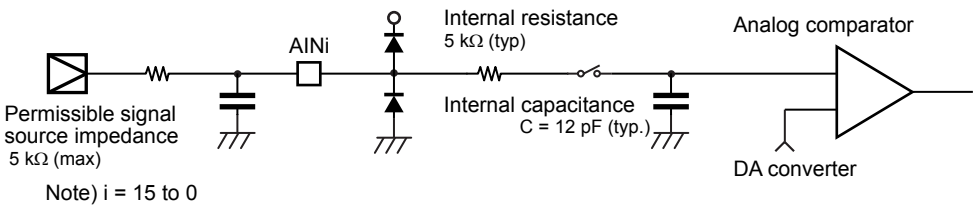


Figure 17-5 Analog Input Equivalent Circuit and Example of Input Pin Processing

18. Key-on Wakeup (KWU)

In the T5CL8 , the STOP mode is released by not only P20($\overline{INT5}$/$\overline{STOP}$) pin but also four (STOP0 to STOP3) pins.

When the STOP mode is released by STOP0 to STOP3 pins, the $\overline{STOP}$ pin needs to be used.
In details, refer to the following section " 18.2 Control ".

18.1 Configuration

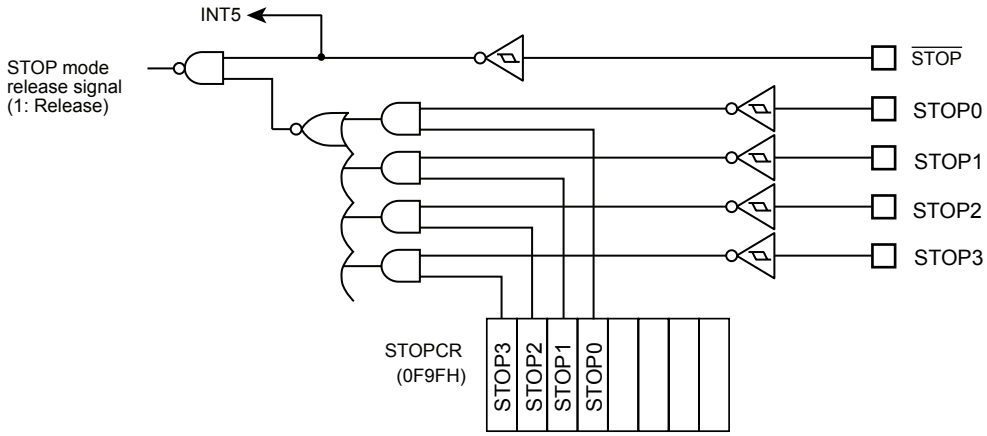


Figure 18-1 Key-on Wakeup Circuit

18.2 Control

STOP0 to STOP3 pins can controlled by Key-on Wakeup Control Register (STOPCR). It can be configured as enable/disable in 1-bit unit. When those pins are used for STOP mode release, configure corresponding I/O pins to input mode by I/O port register beforehand.

Key-on Wakeup Control Register

STOPCR	7	6	5	4	3	2	1	0	
(0F9FH)	STOP3	STOP2	STOP1	STOP0					(Initial value: 0000 ****)

STOP3	STOP mode released by STOP3	0:Disable 1:Enable	Write only
STOP2	STOP mode released by STOP2	0:Disable 1:Enable	Write only
STOP1	STOP mode released by STOP1	0:Disable 1:Enable	Write only
STOP0	STOP mode released by STOP0	0:Disable 1:Enable	Write only

18.3 Function

Stop mode can be entered by setting up the System Control Register (SYSCR1), and can be exited by detecting the "L" level on STOP0 to STOP3 pins, which are enabled by STOPCR, for releasing STOP mode (Note1).

Also, each level of the STOP0 to STOP3 pins can be confirmed by reading corresponding I/O port data register, check all STOP0 to STOP3 pins "H" that is enabled by STOPCR before the STOP mode is started (Note2,3).

Note 1: When the STOP mode released by the edge release mode (SYSCR1<RELM> = “0”), inhibit input from STOP0 to STOP3 pins by Key-on Wakeup Control Register (STOPCR) or must be set "H" level into STOP0 to STOP3 pins that are available input during STOP mode.

Note 2: When the $\overline{\text{STOP}}$ pin input is high or STOP0 to STOP3 pins input which is enabled by STOPCR is low, executing an instruction which starts STOP mode will not place in STOP mode but instead will immediately start the release sequence (Warm up).

Note 3: The input circuit of Key-on Wakeup input and Port input is separated, so each input voltage threshold value is different. Therefore, a value comes from port input before STOP mode start may be different from a value which is detected by Key-on Wakeup input (Figure 18-2).

Note 4: $\overline{\text{STOP}}$ pin doesn’t have the control register such as STOPCR, so when STOP mode is released by STOP0 to STOP3 pins, $\overline{\text{STOP}}$ pin also should be used as STOP mode release function.

Note 5: In STOP mode, Key-on Wakeup pin which is enabled as input mode (for releasing STOP mode) by Key-on Wakeup Control Register (STOPCR) may generate the penetration current, so the said pin must be disabled AD conversion input (analog voltage input).

Note 6: When the STOP mode is released by STOP0 to STOP3 pins, the level of $\overline{\text{STOP}}$ pin should hold "L" level (Figure 18-3).

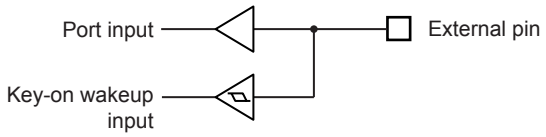


Figure 18-2 Key-on Wakeup Input and Port Input

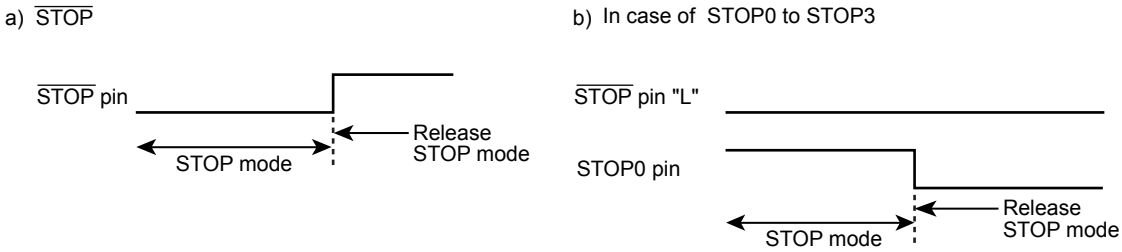


Figure 18-3 Priority of $\overline{\text{STOP}}$ pin and STOP0 to STOP3 pins

Table 18-1 Release level (edge) of STOP mode

Pin name	Release level (edge)	
	SYSCR1<RELM>="1" (Note2)	SYSCR1<RELM>="0"
$\overline{\text{STOP}}$	"H" level	Rising edge
STOP0	"L" level	Don’t use (Note1)
STOP1	"L" level	Don’t use (Note1)
STOP2	"L" level	Don’t use (Note1)
STOP3	"L" level	Don’t use (Note1)

19. Flash Memory

T5CL8 has 61440byte flash memory (address: 1000H to FFFFH). The write and erase operations to the flash memory are controlled in the following three types of mode.

- MCU mode

  The flash memory is accessed by the CPU control in the MCU mode. This mode is used for software bug correction and firmware change after shipment of the device since the write operation to the flash memory is available by retaining the application behavior.

- Serial PROM mode

  The flash memory is accessed by the CPU control in the serial PROM mode. Use of the serial interface (UART) enables the flash memory to be controlled by the small number of pins. T5CL8 in the serial PROM mode supports on-board programming which enables users to program flash memory after the microcontroller is mounted on a user board.

- Parallel PROM mode

  The parallel PROM mode allows the flash memory to be accessed as a stand-alone flash memory by the program writer provided by the third party. High-speed access to the flash memory is available by controlling address and data signals directly. For the support of the program writer, please ask Toshiba sales representative.

In the MCU and serial PROM modes, the flash memory control register (FLSCR) is used for flash memory control. This chapter describes how to access the flash memory using the flash memory control register (FLSCR) in the MCU and serial PROM modes.

Note 1: The 'Read Protect' described by data sheet of old edition was changed into 'Security Program'.

19.1 Flash Memory Control

The flash memory is controlled via the flash memory control register (FLSCR) .

Flash Memory Control Register

FLSCR	7	6	5	4	3	2	1	0	
(0FFFH)	FLSMD				BANKSEL				(Initial value : 1100 1***)

FLSMD	Flash memory command sequence execution control	1100: Disable command sequence execution 0011: Enable command sequence execution Others: Reserved	R/W
BANKSEL	Flash memory bank select control (Serial PROM mode only)	0: Select BANK0 1: Select BANK1	R/W

Note 1: The command sequence of the flash memory can be executed only when FLSMD="0011B". In other cases, any attempts to execute the command sequence are ineffective.

Note 2: FLSMD must be set to either "1100B" or "0011B".

Note 3: BANKSEL is effective only in the serial PROM mode. In the MCU mode, the flash memory is always accessed with actual addresses (1000-FFFFH) regardless of BANKSEL.

Note 4: Bits 2 through 0 in FLSCR are always read as don't care.

19.1.1 Flash Memory Command Sequence Execution Control (FLSCR<FLSMD>)

The flash memory can be protected from inadvertent write due to program error or microcontroller misoperation. This write protection feature is realized by disabling flash memory command sequence execution via the flash memory control register (write protect). To enable command sequence execution, set FLSCR<FLSMD> to "0011B". To disable command sequence execution, set FLSCR<FLSMD> to "1100B". After reset, FLSCR<FLSMD> is initialized to "1100B" to disable command sequence execution. Normally, FLSCR<FLSMD> should be set to "1100B" except when the flash memory needs to be written or erased.

19.1.2 Flash Memory Bank Select Control (FLSCR<BANKSEL>)

In the serial PROM mode, a 2-kbyte BOOTROM is mapped to addresses 7800H-7FFFH and the flash memory is mapped to 2 banks at 8000H-FFFFH. Flash memory addresses 1000H-7FFFH are mapped to 9000H-FFFFH as BANK0, and flash memory addresses 8000H-FFFFH are mapped to 8000H-FFFFH as BANK1. FLSCR<BANKSEL> is used to switch between these banks. For example, to access the flash memory address 7000H, set FLSCR<BANKSEL> to "0" and then access F000H. To access the flash memory address 9000H, set FLSCR<BANKSEL> to "1" and then access 9000H.

In the MCU mode, the flash memory is accessed with actual addresses at 1000H-FFFFH. In this case, FLSCR<BANKSEL> is ineffective (i.e., its value has no effect on other operations).

Table 19-1 Flash Memory Access

Operating Mode	FLSCR <BANKSEL>	Access Area	Specified Address
MCU mode	Don't care	1000H-FFFFH	
Serial PROM mode	0 (BANK0)	1000H-7FFFH	9000H-FFFFH
	1 (BANK1)	8000H-FFFFH	

19.2 Command Sequence

The command sequence in the MCU and the serial PROM modes consists of six commands (JEDEC compatible), as shown in Table 19-2. Addresses specified in the command sequence are recognized with the lower 12 bits (excluding BA, SA, and FF7FH used for security program). The upper 4 bits are used to specify the flash memory area, as shown in Table 19-3.

Table 19-2 Command Sequence

	Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
		Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
1	Byte program	555H	AAH	AAAH	55H	555H	A0H	BA (Note 1)	Data (Note 1)	-	-	-	-
2	Sector Erase (4-kbyte Erase)	555H	AAH	AAAH	55H	555H	80H	555H	AAH	AAAH	55H	SA (Note 2)	30H
3	Chip Erase (All Erase)	555H	AAH	AAAH	55H	555H	80H	555H	AAH	AAAH	55H	555H	10H
4	Product ID Entry	555H	AAH	AAAH	55H	555H	90H	-	-	-	-	-	-
5	Product ID Exit	XXH	F0H	-	-	-	-	-	-	-	-	-	-
	Product ID Exit	555H	AAH	AAAH	55H	555H	F0H	-	-	-	-	-	-
6	Security Program	555H	AAH	AAAH	55H	555H	A5H	FF7FH	00H	-	-	-	-

Note 1: Set the address and data to be written.

Note 2: The area to be erased is specified with the upper 4 bits of the address.

Table 19-3 Address Specification in the Command Sequence

Operating Mode	FLSCR <BANKSEL>	Specified Address
MCU mode	Don't care	1***H-F***H
Serial PROM mode	0 (BANK0)	9***H-F***H
	1 (BANK1)	8***H-F***H

19.2.1 Byte Program

This command writes the flash memory for each byte unit. The addresses and data to be written are specified in the 4th bus write cycle. Each byte can be programmed in a maximum of 40 μs. The next command sequence cannot be executed until the write operation is completed. To check the completion of the write operation, perform read operations repeatedly until the same data is read twice from the same address in the flash memory. During the write operation, any consecutive attempts to read from the same address is reversed bit 6 of the data (toggling between 0 and 1).

Note: To rewrite data to Flash memory addresses at which data (including FFH) is already written, make sure to erase the existing data by "sector erase" or "chip erase" before rewriting data.

19.2.2 Sector Erase (4-kbyte Erase)

This command erases the flash memory in units of 4 kbytes. The flash memory area to be erased is specified by the upper 4 bits of the 6th bus write cycle address. For example, in the MCU mode, to erase 4 kbytes from 7000H to 7FFFH, specify one of the addresses in 7000H-7FFFH as the 6th bus write cycle. In the serial PROM mode, to erase 4 kbytes from 7000H to 7FFFH, set FLSCR<BANKSEL> to "0" and then specify one of the addresses in F000H-FFFFH as the 6th bus write cycle. The sector erase command is effective only in the MCU and serial PROM modes, and it cannot be used in the parallel PROM mode.

A maximum of 30 ms is required to erase 4 kbytes. The next command sequence cannot be executed until the erase operation is completed. To check the completion of the erase operation, perform read operations repeatedly for data polling until the same data is read twice from the same address in the flash memory. During the erase operation, any consecutive attempts to read from the same address is reversed bit 6 of the data (toggling between 0 and 1).

19.2.3 Chip Erase (All Erase)

This command erases the entire flash memory in approximately 30 ms. The next command sequence cannot be executed until the erase operation is completed. To check the completion of the erase operation, perform read operations repeatedly for data polling until the same data is read twice from the same address in the flash memory. During the erase operation, any consecutive attempts to read from the same address is reversed bit 6 of the data (toggling between 0 and 1). After the chip is erased, all bytes contain FFH.

19.2.4 Product ID Entry

This command activates the Product ID mode. In the Product ID mode, the vendor ID, the flash ID, and the security program status can be read from the flash memory.

Table 19-4 Values To Be Read in the Product ID Mode

Address	Meaning	Read Value
F000H	Vendor ID	98H
F001H	Flash macro ID	41H
F002H	Flash size	0EH: 60 kbytes 0BH: 48 kbytes 07H: 32 kbytes 05H: 24 kbytes 03H: 16 kbytes 01H: 8 kbytes 00H: 4 kbytes
FF7FH	Security program status	FFH: Security program disabled Other than FFH: Security program enabled

Note: The value at address F002H (flash size) depends on the size of flash memory incorporated in each product. For example, if the product has 60-kbyte flash memory, "0EH" is read from address F002H.

19.2.5 Product ID Exit

This command is used to exit the Product ID mode.

19.2.6 Security Program

This command enables the read protection or write protection setting in the flash memory. When the security program is enabled, the flash memory cannot be read in the parallel PROM mode. In the serial PROM mode, the flash write and RAM loader commands cannot be executed.

To enable the security program setting in the serial PROM mode, set FLSCR<BANKSEL> to "1" before executing the security program command sequence. To disable the security program setting, it is necessary to execute the chip erase command sequence. Whether or not the security program is enabled can be checked by reading FF7FH in the Product ID mode. For details, see Table 19-4.

It takes a maximum of 40 μs to set security program in the flash memory. The next command sequence cannot be executed until this operation is completed. To check the completion of the security program operation, perform read operations repeatedly for data polling until the same data is read twice from the same address in the flash memory. During the security program operation, any attempts to read from the same address is reversed bit 6 of the data (toggling between 0 and 1).

19.3 Toggle Bit (D6)

After the byte program, chip erase, and security program command sequence is executed, any consecutive attempts to read from the same address is reversed bit 6 (D6) of the data (toggling between 0 and 1) until the operation is completed. Therefore, this toggle bit provides a software mechanism to check the completion of each operation. Usually perform read operations repeatedly for data polling until the same data is read twice from the same address in the flash memory. After the byte program, chip erase, or security program command sequence is executed, the initial read of the toggle bit always produces a "1".

19.4 Access to the Flash Memory Area

When the write, erase and security program are set in the flash memory, read and fetch operations cannot be performed in the entire flash memory area. Therefore, to perform these operations in the entire flash memory area, access to the flash memory area by the control program in the BOOTROM or RAM area. (The flash memory program cannot write to the flash memory.) The serial PROM or MCU mode is used to run the control program in the BOOTROM or RAM area.

Note 1: The flash memory can be written or read for each byte unit. Erase operations can be performed either in the entire area or in units of 4 kbytes, whereas read operations can be performed by an one transfer instruction. However, the command sequence method is adopted for write and erase operations, requiring several-byte transfer instructions for each operation.

Note 2: To rewrite data to Flash memory addresses at which data (including FFH) is already written, make sure to erase the existing data by "sector erase" or "chip erase" before rewriting data.

19.4.1 Flash Memory Control in the Serial PROM Mode

The serial PROM mode is used to access to the flash memory by the control program provided in the BOOTROM area. Since almost of all operations relating to access to the flash memory can be controlled simply by the communication data of the serial interface (UART), these functions are transparent to the user. For the details of the serial PROM mode, see “Serial PROM Mode.”

To access to the flash memory by using peripheral functions in the serial PROM mode, run the RAM loader command to execute the control program in the RAM area. The procedures to execute the control program in the RAM area is shown in " 19.4.1.1 How to write to the flash memory by executing the control program in the RAM area (in the RAM loader mode within the serial PROM mode) ".

19.4.1.1 How to write to the flash memory by executing the control program in the RAM area (in the RAM loader mode within the serial PROM mode)

(Steps 1 and 2 are controlled by the BOOTROM, and steps 3 through 10 are controlled by the control program executed in the RAM area.)

1. Transfer the write control program to the RAM area in the RAM loader mode.
2. Jump to the RAM area.
3. Disable (DI) the interrupt master enable flag (IMF←"0").
4. Set FLSCR<FLSMD> to "0011B" (to enable command sequence execution).
5. Execute the erase command sequence.
6. Read the same flash memory address twice.
   (Repeat step 6 until the same data is read by two consecutive reads operations.)
7. Specify the bank to be written in FLSCR<BANKSEL>.
8. Execute the write command sequence.
9. Read the same flash memory address twice.
   (Repeat step 9 until the same data is read by two consecutive reads operations.)
10. Set FLSCR<FLSMD> to "1100B" (to disable command sequence execution).

Note 1: Before writing to the flash memory in the RAM area, disable interrupts by setting the interrupt master enable flag (IMF) to "0". Usually disable interrupts by executing the DI instruction at the head of the write control program in the RAM area.

Note 2: Since the watchdog timer is disabled by the BOOTROM in the RAM loader mode, it is not required to disable the watchdog timer by the RAM loader program.

Example :After chip erasure, the program in the RAM area writes data 3FH to address F000H.

```
                DI                          : Disable interrupts (IMF←"0")
                LD      (FLSCR),00111000B   : Enable command sequence execution.
                LD      IX,0F555H
                LD      IY,0FAAAH
                LD      HL,0F000H
; #### Flash Memory Chip erase Process ####
                LD      (IX),0AAH           : 1st bus write cycle
                LD      (IY),55H            : 2nd bus write cycle
                LD      (IX),80H            : 3rd bus write cycle
                LD      (IX),0AAH           : 4th bus write cycle
                LD      (IY),55H            : 5th bus write cycle
                LD      (IX),10H            : 6th bus write cycle
sLOOP1:         LD      W,(HL)
                CMP     W,(HL)
                JR      NZ,sLOOP1           : Loop until the same value is read.
                SET     (FLSCR).3           : Set BANK1.
; #### Flash Memory Write Process ####
                LD      (IX),0AAH           : 1st bus write cycle
                LD      (IY),55H            : 2nd bus write cycle
                LD      (IX),0A0H           : 3rd bus write cycle
                LD      (HL),3FH            : 4th bus write cycle, (F000H)=3FH
sLOOP2:         LD      W,(HL)
                CMP     W,(HL)
                JR      NZ,sLOOP2           : Loop until the same value is read.
                LD      (FLSCR),11001000B   : Disable command sequence execution.
sLOOP3:         JP      sLOOP3
```

19.4.2 Flash Memory Control in the MCU mode

In the MCU mode, write operations are performed by executing the control program in the RAM area. Before execution of the control program, copy the control program into the RAM area or obtain it from the external using the communication pin. The procedures to execute the control program in the RAM area in the MCU mode are described below.

19.4.2.1 How to write to the flash memory by executing a user write control program in the RAM area (in the MCU mode)

(Steps 1 and 2 are controlled by the program in the flash memory, and steps 3 through 11 are controlled by the control program in the RAM area.)

1. Transfer the write control program to the RAM area.
2. Jump to the RAM area.
3. Disable (DI) the interrupt master enable flag (IMF←"0").
4. Disable the watchdog timer, if it is used.
5. Set FLSCR<FLSMD> to "0011B" (to enable command sequence execution).
6. Execute the erase command sequence.
7. Read the same flash memory address twice.
   (Repeat step 7 until the same data is read by two consecutive read operations.)
8. Execute the write command sequence. (It is not required to specify the bank to be written.)
9. Read the same flash memory address twice.
   (Repeat step 9 until the same data is read by two consecutive read operations.)
10. Set FLSCR<FLSMD> to "1100B" (to disable command sequence execution).
11. Jump to the flash memory area.

Note 1: Before writing to the flash memory in the RAM area, disable interrupts by setting the interrupt master enable flag (IMF) to "0". Usually disable interrupts by executing the DI instruction at the head of the write control program in the RAM area.

Note 2: When writing to the flash memory, do not intentionally use non-maskable interrupts (the watchdog timer must be disabled if it is used). If a non-maskable interrupt occurs while the flash memory is being written, unexpected data is read from the flash memory (interrupt vector), resulting in malfunction of the microcontroller.

Example :After sector erasure (E000H-EFFFH), the program in the RAM area writes data 3FH to address E000H.

```
                DI                          : Disable interrupts (IMF←"0")
                LD      (WDTCR2),4EH        : Clear the WDT binary counter.
                LDW     (WDTCR1),0B101H     : Disable the WDT.
                LD      (FLSCR),00111000B   : Enable command sequence execution.
                LD      IX,0F555H
                LD      IY,0FAAAH
                LD      HL,0E000H
; #### Flash Memory Sector Erase Process ####
                LD      (IX),0AAH           : 1st bus write cycle
                LD      (IY),55H            : 2nd bus write cycle
                LD      (IX),80H            : 3rd bus write cycle
                LD      (IX),0AAH           : 4th bus write cycle
                LD      (IY),55H            : 5th bus write cycle
                LD      (HL),30H            : 6th bus write cycle
sLOOP1:         LD      W,(HL)
                CMP     W,(HL)
                JR      NZ,sLOOP1           : Loop until the same value is read.
; #### Flash Memory Write Process ####
                LD      (IX),0AAH           : 1st bus write cycle
                LD      (IY),55H            : 2nd bus write cycle
                LD      (IX),0A0H           : 3rd bus write cycle
                LD      (HL),3FH            : 4th bus write cycle, (1000H)=3FH
sLOOP2:         LD      W,(HL)
                CMP     W,(HL)
                JR      NZ,sLOOP2           : Loop until the same value is read.
                LD      (FLSCR),11001000B   : Disable command sequence execution.
                JP      XXXXH               : Jump to the flash memory area.
```

Example :This write control program reads data from address F000H and stores it to 98H in the RAM area.

```
                LD      A,(0F000H)          : Read data from address F000H.
                LD      (98H),A             : Store data to address 98H.
```

20. Serial PROM Mode

20.1 Outline

The T5CL8 has a 2048 byte BOOTROM (Mask ROM) for programming to flash memory. The BOOTROM is available in the serial PROM mode, and controlled by TEST, BOOT and $\overline{\text{RESET}}$ pins. Communication is performed via UART. The serial PROM mode has seven types of operating mode: Flash memory writing, RAM loader, Flash memory SUM output, Product ID code output, Flash memory status output, Flash memory erasing and Flash memory security program setting. Memory address mapping in the serial PROM mode differs from that in the MCU mode. Figure 20-1 shows memory address mapping in the serial PROM mode.

Table 20-1 Operating Range in the Serial PROM Mode

Parameter	Min	Max	Unit
Power supply	4.5	5.5	V
High frequency (Note)	2	16	MHz

Note: Though included in above operating range, some of high frequencies are not supported in the serial PROM mode. For details, refer to “Table 20-5”.

20.2 Memory Mapping

The Figure 20-1 shows memory mapping in the Serial PROM mode and MCU mode.

In the serial PROM mode, the BOOTROM (Mask ROM) is mapped in addresses from 7800H to 7FFFH. The flash memory is divided into two banks for mapping. Therefore, when the RAM loader mode (60H) is used, it is required to specify the flash memory address according to Figure 20-1 (For detail of banks and control register, refer to the chapter of “Flash Memory Control Register”.)

To use the Flash memory writing command (30H), specify the flash memory addresses from 1000H to FFFFH, that is the same addresses in the MCU mode, because the BOOTROM changes the flash memory address.

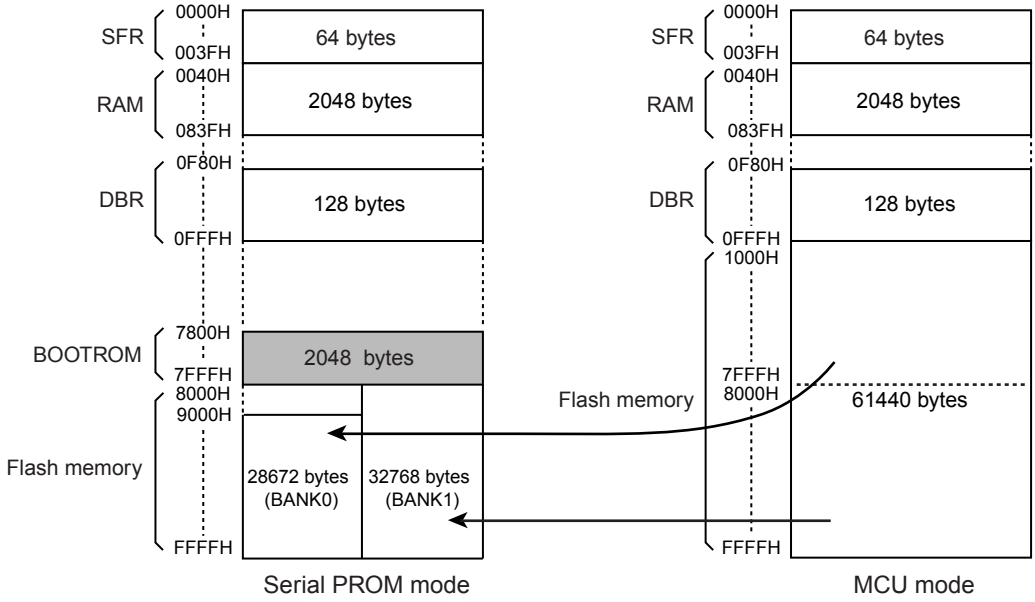


Figure 20-1 Memory Address Maps

20.3 Serial PROM Mode Setting

20.3.1 Serial PROM Mode Control Pins

To execute on-board programming, activate the serial PROM mode. Table 20-2 shows pin setting to activate the serial PROM mode.

Table 20-2 Serial PROM Mode Setting

Pin	Setting
TEST pin	High
BOOT/RXD1 pin	High
$\overline{\text{RESET}}$ pin	

Note: The BOOT pin is shared with the UART communication pin (RXD1 pin) in the serial PROM mode. This pin is used as UART communication pin after activating serial PROM mode

20.3.2 Pin Function

In the serial PROM mode, TXD1 (P02) and RXD1 (P01) are used as a serial interface pin.

Table 20-3 Pin Function in the Serial PROM Mode

Pin Name (Serial PROM Mode)	Input/ Output	Function		Pin Name (MCU Mode)
TXD1	Output	Serial data output	(Note 1)	P02
BOOT/RXD1	Input/Input	Serial PROM mode control/Serial data input		P01
$\overline{\text{RESET}}$	Input	Serial PROM mode control		$\overline{\text{RESET}}$
TEST	Input	Fixed to high		TEST
VDD, AVDD	Power supply	4.5 to 5.5 V		
VSS	Power supply	0 V		
VAREF	Power supply	Leave open or apply input reference voltage.		
I/O ports except P02, P01	I/O	These ports are in the high-impedance state in the serial PROM mode.		
XIN	Input	Self-oscillate with an oscillator.	(Note 2)	
XOUT	Output			

Note 1: During on-board programming with other parts mounted on a user board, be careful no to affect these communication control pins.

Note 2: Operating range of high frequency in serial PROM mode is 2 MHz to 16 MHz.

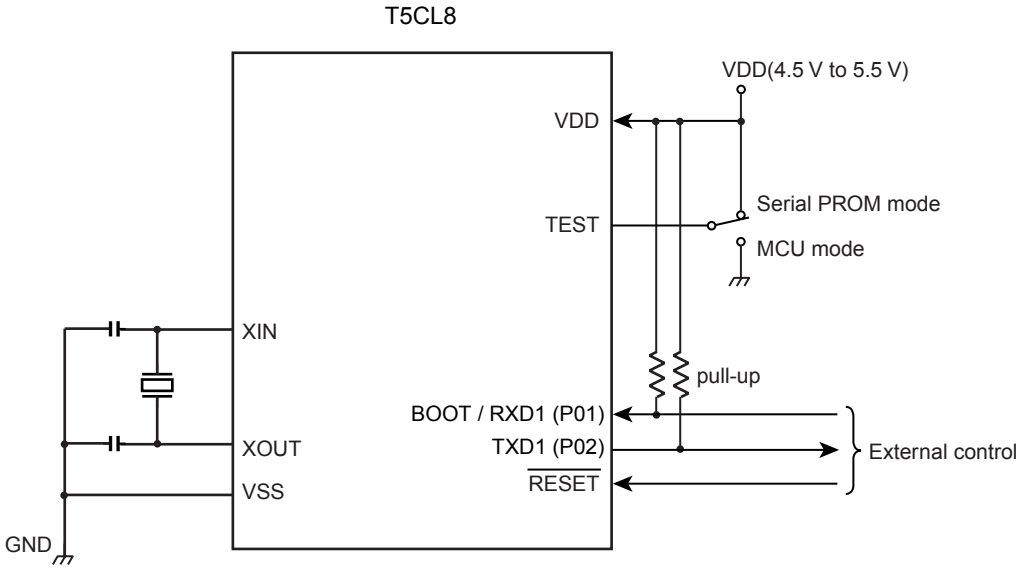


Figure 20-2 Serial PROM Mode Pin Setting

Note 1: For connection of other pins, refer to " Table 20-3 Pin Function in the Serial PROM Mode ".

20.3.3 Example Connection for On-Board Writing

Figure 20-3 shows an example connection to perform on-board wring.

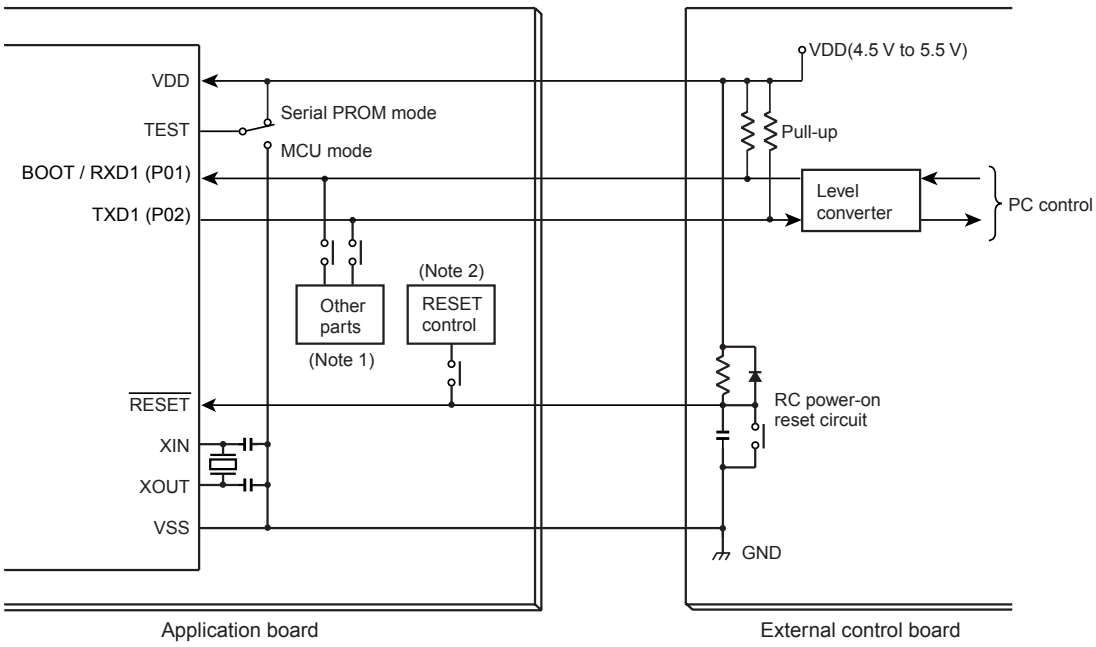


Figure 20-3 Example Connection for On-Board Writing

Note 1: When other parts on the application board effect the UART communication in the serial PROM mode, isolate these pins by a jumper or switch.

Note 2: When the reset control circuit on the application board effects activation of the serial PROM mode, isolate the pin by a jumper or switch.

Note 3: For connection of other pins, refer to " Table 20-3 Pin Function in the Serial PROM Mode ".

20.3.4 Activating the Serial PROM Mode

The following is a procedure to activate the serial PROM mode. " Figure 20-4 Serial PROM Mode Timing " shows a serial PROM mode timing.

1. Supply power to the VDD pin.
2. Set the $\overline{\text{RESET}}$ pin to low.
3. Set the TEST pin and BOOT/RXD1 pins to high.
4. Wait until the power supply and clock oscillation stabilize.
5. Set the $\overline{\text{RESET}}$ pin to high.
6. Input the matching data (5AH) to the BOOT/RXD1 pin after setup sequence. For details of the setup timing, refer to " 20.15 UART Timing ".

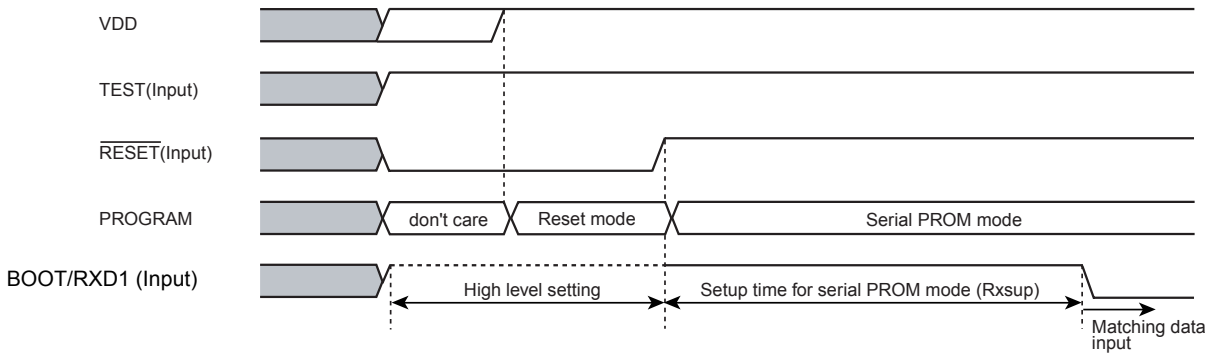


Figure 20-4 Serial PROM Mode Timing

20.4 Interface Specifications for UART

The following shows the UART communication format used in the serial PROM mode.

To perform on-board programming, the communication format of the write controller must also be set in the same manner.

The default baud rate is 9600 bps regardless of operating frequency of the microcontroller. The baud rate can be modified by transmitting the baud rate modification data shown in Table 1-4 to T5CL8. The Table 20-5 shows an operating frequency and baud rate. The frequencies which are not described in Table 20-5 can not be used.

- Baud rate (Default): 9600 bps
- Data length: 8 bits
- Parity addition: None
- Stop bit: 1 bit

Table 20-4 Baud Rate Modification Data

Baud rate modification data	04H	05H	06H	07H	0AH	18H	28H
Baud rate (bps)	76800	62500	57600	38400	31250	19200	9600

Table 20-5 Operating Frequency and Baud Rate in the Serial PROM Mode

(Note 3)	Reference Baud Rate (bps)		76800		62500		57600		38400		31250		19200		9600	
	Baud Rate Modification Data		04H		05H		06H		07H		0AH		18H		28H	
	Ref. Frequency (MHz)	Rating (MHz)	Baud rate (bps)	(%)	(bps)	(%)	(bps)	(%)	(bps)	(%)	(bps)	(%)	(bps)	(%)	(bps)	(%)
1	2	1.91 to 2.10	-	-	-	-	-	-	-	-	-	-	-	-	9615	+0.16
2	4	3.82 to 4.19	-	-	-	-	-	-	-	-	31250	0.00	19231	+0.16	9615	+0.16
	4.19	3.82 to 4.19	-	-	-	-	-	-	-	-	32734	+4.75	20144	+4.92	10072	+4.92
3	4.9152	4.70 to 5.16	-	-	-	-	-	-	38400	0.00	-	-	19200	0.00	9600	0.00
	5	4.70 to 5.16	-	-	-	-	-	-	39063	+1.73	-	-	19531	+1.73	9766	+1.73
4	6	5.87 to 6.45	-	-	-	-	-	-	-	-	-	-	-	-	9375	-2.34
	6.144	5.87 to 6.45	-	-	-	-	-	-	-	-	-	-	-	-	9600	0.00
5	7.3728	7.05 to 7.74	-	-		-	57600	0.00	-	-	-	-	19200	0.00	9600	0.00
6	8	7.64 to 8.39	-	-	62500	0.00	-	-	38462	+0.16	31250	0.00	19231	+0.16	9615	+0.16
7	9.8304	9.40 to 10.32	76800	0.00	-	-	-	-	38400	0.00	-	-	19200	0.00	9600	0.00
	10	9.40 to 10.32	78125	+1.73	-	-	-	-	39063	+1.73	-	-	19531	+1.73	9766	+1.73
8	12	11.75 to 12.90	-	-	-	-	57692	+0.16	-	-	31250	0.00	18750	-2.34	9375	-2.34
	12.288	11.75 to 12.90	-	-	-	-	59077	+2.56	-	-	32000	+2.40	19200	0.00	9600	0.00
	12.5	11.75 to 12.90	-	-	60096	-3.85	60096	+4.33	-	-	30048	-3.85	19531	+1.73	9766	+1.73
9	14.7456	14.10 to 15.48	-	-	-	-	57600	0.00	38400	0.00	-	-	19200	0.00	9600	0.00
10	16	15.27 to 16.77	76923	+0.16	62500	0.00	-	-	38462	+0.16	31250	0.00	19231	+0.16	9615	+0.16

Note 1: “Ref. Frequency” and “Rating” show frequencies available in the serial PROM mode. Though the frequency is supported in the serial PROM mode, the serial PROM mode may not be activated correctly due to the frequency difference in the external controller (such as personal computer) and oscillator, and load capacitance of communication pins.

Note 2: It is recommended that the total frequency difference is within ±3% so that auto detection is performed correctly by the reference frequency.

Note 3: The external controller must transmit the matching data (5AH) repeatedly till the auto detection of baud rate is performed. This number indicates the number of times the matching data is transmitted for each frequency.

20.5 Operation Command

The eight commands shown in Table 20-6 are used in the serial PROM mode. After reset release, the T5CL8 waits for the matching data (5AH).

Table 20-6 Operation Command in the Serial PROM Mode

Command Data	Operating Mode	Description
5AH	Setup	Matching data. Execute this command after releasing the reset.
F0H	Flash memory erasing	Erases the flash memory area (address 1000H to FFFFH).
30H	Flash memory writing	Writes to the flash memory area (address 1000H to FFFFH).
60H	RAM loader	Writes to the specified RAM area (address 0050H to 083FH).
90H	Flash memory SUM output	Outputs the 2-byte checksum upper byte and lower byte in this order for the entire area of the flash memory (address 1000H to FFFFH).
C0H	Product ID code output	Outputs the product ID code (13-byte data).
C3H	Flash memory status output	Outputs the status code (7-byte data) such as the security program condition.
FAH	Flash memory security program setting	Enables the security program.

20.6 Operation Mode

The serial PROM mode has seven types of modes, that are (1) Flash memory erasing, (2) Flash memory writing, (3) RAM loader, (4) Flash memory SUM output, (5) Product ID code output, (6) Flash memory status output and (7) Flash memory security program setting modes. Description of each mode is shown below.

1. Flash memory erasing mode
   The flash memory is erased by the chip erase (erasing an entire flash area) or sector erase (erasing sectors in 4-kbyte units). The erased area is filled with FFH. When the security program is enabled, the sector erase in the flash erasing mode can not be performed. To disable the security program, perform the chip erase. Before erasing the flash memory, T5CL8 checks the passwords except a blank product. If the password is not matched, the flash memory erasing mode is not activated.
2. Flash memory writing mode
   Data is written to the specified flash memory address for each byte unit. The external controller must transmit the write data in the Intel Hex format (Binary). If no error is encountered till the end record, T5CL8 calculates the checksum for the entire flash memory area (1000H to FFFFH), and returns the obtained result to the external controller. When the security program is enabled, the flash memory writing mode is not activated. In this case, perform the chip erase command beforehand in the flash memory erasing mode. Before activating the flash memory writing mode, T5CL8 checks the password except a blank product. If the password is not matched, flash memory writing mode is not activated.
3. RAM loader mode
   The RAM loader transfers the data in Intel Hex format sent from the external controller to the internal RAM. When the transfer is completed normally, the RAM loader calculates the checksum. After transmitting the results, the RAM loader jumps to the RAM address specified with the first data record in order to execute the user program. When the security program is enabled, the RAM loader mode is not activated. In this case, perform the chip erase beforehand in the flash memory erasing mode. Before activating the RAM loader mode, T5CL8 checks the password except a blank product. If the password is not matched, flash RAM loader mode is not activated.
4. Flash memory SUM output mode
   The checksum is calculated for the entire flash memory area (1000H to FFFFH), and the result is returned to the external controller. Since the BOOTROM does not support the operation command to read the flash memory, use this checksum to identify programs when managing revisions of application programs.
5. Product ID code output
   The code used to identify the product is output. The code to be output consists of 13-byte data, which includes the information indicating the area of the ROM incorporated in the product. The external controller reads this code, and recognizes the product to write.
   (In the case of T5CL8, the addresses from 1000H to FFFFH become the ROM area.)

6. Flash memory status output mode
   The status of the area from FFE0H to FFFFH, and the security program condition are output as 7-byte code. The external controller reads this code to recognize the flash memory status.
7. Flash memory security program setting mode
   This mode disables reading and writing the flash memory data in parallel PROM mode. In the serial PROM mode, the flash memory writing and RAM loader modes are disabled. To disable the flash memory security program, perform the chip erase in the flash memory erasing mode.

20.6.1 Flash Memory Erasing Mode (Operating command: F0H)

Table 20-7 shows the flash memory erasing mode.

Table 20-7 Flash Memory Erasing Mode

	Transfer Byte	Transfer Data from the External Controller to T5CL8	Baud Rate	Transfer Data from T5CL8 to the External Controller
BOOT ROM	1st byte 2nd byte	Matching data (5AH) -	9600 bps 9600 bps	- (Automatic baud rate adjustment) OK: Echo back data (5AH) Error: No data transmitted
	3rd byte 4th byte	Baud rate change data (Table 20-4) -	9600 bps 9600 bps	- OK: Echo back data Error: A1H × 3, A3H × 3, 62H × 3 (Note 1)
	5th byte 6th byte	Operation command data (F0H) -	Modified baud rate Modified baud rate	- OK: Echo back data (F0H) Error: A1H × 3, A3H × 3, 63H × 3 (Note 1)
	7th byte 8th byte	Password count storage address bit 15 to 08 (Note 4, 5)	Modified baud rate Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	9th byte 10th byte	Password count storage address bit 07 to 00 (Note 4, 5)	Modified baud rate Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	11th byte 12th byte	Password comparison start address bit 15 to 08 (Note 4, 5)	Modified baud rate Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	13th byte 14th byte	Password comparison start address bit 07 to 00 (Note 4, 5)	Modified baud rate Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted)
	15th byte : m'th byte	Password string (Note 4, 5) -	Modified baud rate Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	n'th - 2 byte	Erase area specification (Note 2)	Modified baud rate	-
	n'th - 1 byte	-	Modified baud rate	OK: Checksum (Upper byte) (Note 3) Error: Nothing transmitted
	n'th byte	-	Modified baud rate	OK: Checksum (Lower byte) (Note 3) Error: Nothing transmitted
	n'th + 1 byte	(Wait for the next operation command data)	Modified baud rate	-

Note 1: "xxH × 3" indicates that the device enters the halt condition after transmitting 3 bytes of xxh.

Note 2: Refer to " 20.13 Specifying the Erasure Area ".

Note 3: Refer to " 20.8 Checksum (SUM) ".

Note 4: Refer to " 20.10 Passwords ".

Note 5: Do not transmit the password string for a blank product.

Note 6: When a password error occurs, T5CL8 stops UART communication and enters the halt mode. Therefore, when a password error occurs, initialize T5CL8 by the $\overline{\text{RESET}}$ pin and reactivate the serial PROM mode.

Note 7: If an error occurs during transfer of a password address or a password string, T5CL8 stops UART communication and enters the halt condition. Therefore, when a password error occurs, initialize T5CL8 by the $\overline{\text{RESET}}$ pin and reactivate the serial PROM mode.

Description of the flash memory erasing mode

1. The 1st through 4th bytes of the transmitted and received data contain the same data as in the flash memory writing mode.

2. The 5th byte of the received data contains the command data in the flash memory erasing mode (F0H).
3. When the 5th byte of the received data contains the operation command data shown in Table 20-6, the device echoes back the value which is the same data in the 6th byte position of the received data (in this case, F0H). If the 5th byte of the received data does not contain the operation command data, the device enters the halt condition after sending 3 bytes of the operation command error code (63H).
4. The 7th thorough m'th bytes of the transmitted and received data contain the same data as in the flash memory writing mode. In the case of a blank product, do not transmit a password string. (Do not transmit a dummy password string.)
5. The n’th - 2 byte contains the erasure area specification data. The upper 4 bits and lower 4 bits specify the start address and end address of the erasure area, respectively. For the detailed description, see “1.13 Specifying the Erasure Area”.
6. The n’th - 1 byte and n’th byte contain the upper and lower bytes of the checksum, respectively. For how to calculate the checksum, refer to “1.8 Checksum (SUM)”. Checksum is calculated unless a receiving error or Intel Hex format error occurs. After sending the end record, the external controller judges whether the transmission is completed correctly by receiving the checksum sent by the device.
7. After sending the checksum, the device waits for the next operation command data.

20.6.2 Flash Memory Writing Mode (Operation command: 30H)

Table 20-8 shows flash memory writing mode process.

Table 20-8 Flash Memory Writing Mode Process

	Transfer Byte	Transfer Data from External Controller to T5CL8	Baud Rate	Transfer Data from T5CL8 to External Controller
BOOT ROM	1st byte 2nd byte	Matching data (5Ah) -	9600 bps 9600 bps	- (Automatic baud rate adjustment) OK: Echo back data (5AH) Error: Nothing transmitted
	3rd byte 4th byte	Baud rate modification data (See Table 20-4) -	9600 bps 9600 bps	- OK: Echo back data Error: A1H × 3, A3H × 3, 62H × 3 (Note 1)
	5th byte 6th byte	Operation command data (30H) -	Modified baud rate Modified baud rate	- OK: Echo back data (30H) Error: A1H × 3, A3H × 3, 63H × 3 (Note 1)
	7th byte 8th byte	Password count storage address bit 15 to 08 (Note 4)	Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	9th byte 10th byte	Password count storage address bit 07 to 00 (Note 4)	Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	11th byte 12th byte	Password comparison start address bit 15 to 08 (Note 4)	Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	13th byte 14th byte	Password comparison start address bit 07 to 00 (Note 4)	Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted)
	15th byte : m'th byte	Password string (Note 5) -	Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	m'th + 1 byte : n'th - 2 byte	Intel Hex format (binary) (Note 2)	Modified baud rate	- -
	n'th - 1 byte	-	Modified baud rate	OK: SUM (Upper byte) (Note 3) Error: Nothing transmitted
	n'th byte	-	Modified baud rate	OK: SUM (Lower byte) (Note 3) Error: Nothing transmitted
	n'th + 1 byte	(Wait state for the next operation command data)	Modified baud rate	-

Note 1: "xxH × 3" indicates that the device enters the halt condition after sending 3 bytes of xxH. For details, refer to " 20.7 Error Code ".

Note 2: Refer to " 20.9 Intel Hex Format (Binary) ".

Note 3: Refer to " 20.8 Checksum (SUM) ".

Note 4: Refer to " 20.10 Passwords ".

Note 5: If addresses from FFE0H to FFFFH are filled with "FFH", the passwords are not compared because the device is considered as a blank product. Transmitting a password string is not required. Even in the case of a blank product , it is required to specify the password count storage address and the password comparison start address. Transmit these data from the external controller. If a password error occurs due to incorrect password count storage address or password comparison start address, T5CL8 stops UART communication and enters the halt condition. Therefore, when a password error occurs, initialize T5CL8 by the $\overline{\text{RESET}}$ pin and reactivate the serial ROM mode.

Note 6: If the security program is enabled or a password error occurs, T5CL8 stops UART communication and enters the halt confition. In this case, initialize T5CL8 by the $\overline{\text{RESET}}$ pin and reactivate the serial ROM mode.

Note 7: If an error occurs during the reception of a password address or a password string, T5CL8 stops UART communication and enters the halt condition. In this case, initialize T5CL8 by the $\overline{\text{RESET}}$ pin and reactivate the serial PROM mode.

Description of the flash memory writing mode

1. The 1st byte of the received data contains the matching data. When the serial PROM mode is activated, T5CL8 (hereafter called device), waits to receive the matching data (5AH). Upon reception of the matching data, the device automatically adjusts the UART's initial baud rate to 9600 bps.
2. When receiving the matching data (5AH), the device transmits an echo back data (5AH) as the second byte data to the external controller. If the device can not recognize the matching data, it does not transmit the echo back data and waits for the matching data again with automatic baud rate adjustment. Therefore, the external controller should transmit the matching data repeatedly till the device transmits an echo back data. The transmission repetition count varies depending on the frequency of device. For details, refer to Table 20-5.
3. The 3rd byte of the received data contains the baud rate modification data. The five types of baud rate modification data shown in Table 20-4 are available. Even if baud rate is not modified, the external controller should transmit the initial baud rate data (28H: 9600 bps).
4. Only when the 3rd byte of the received data contains the baud rate modification data corresponding to the device's operating frequency, the device echoes back data the value which is the same data in the 4th byte position of the received data. After the echo back data is transmitted, baud rate modification becomes effective. If the 3rd byte of the received data does not contain the baud rate modification data, the device enters the halts condition after sending 3 bytes of baud rate modification error code (62H).
5. The 5th byte of the received data contains the command data (30H) to write the flash memory.
6. When the 5th byte of the received data contains the operation command data shown in Table 1-6, the device echoes back the value which is the same data in the 6th byte position of the received data (in this case, 30H). If the 5th byte of the received data does not contain the operation command data, the device enters the halt condition after sending 3 bytes of the operation command error code (63H).
7. The 7th byte contains the data for 15 to 8 bits of the password count storage address. When the data received with the 7th byte has no receiving error, the device does not send any data. If a receiving error or password error occurs, the device does not send any data and enters the halt condition.
8. The 9th byte contains the data for 7 to 0 bits of the password count storage address. When the data received with the 9th byte has no receiving error, the device does not send any data. If a receiving error or password error occurs, the device does not send any data and enters the halt condition.
9. The 11th byte contains the data for 15 to 8 bits of the password comparison start address. When the data received with the 11th byte has no receiving error, the device does not send any data. If a receiving error or password error occurs, the device does not send any data and enters the halt condition.
10. The 13th byte contains the data for 7 to 0 bits of the password comparison start address. When the data received with the 13th byte has no receiving error, the device does not send any data. If a receiving error or password error occurs, the device does not send any data and enters the halt condition.
11. The 15th through m'th bytes contain the password data. The number of passwords becomes the data (N) stored in the password count storage address. The external password data is compared with N-byte data from the address specified by the password comparison start address. The external controller should send N-byte password data to the device. If the passwords do not match, the device enters the halt condition without returning an error code to the external controller. If the addresses from FFE0H to FFFFH are filled with "FFH", the passwords are not conpared because the device is considered as a blank product.
12. The m'th + 1 through n'th - 2 bytes of the received data contain the binary data in the Intel Hex format. No received data is echoed back to the external controller. After receiving the start mark (3AH for ":") in the Intel Hex format, the device starts data record reception. Therefore, the received data except 3AH is ignored until the start mark is received. After receiving the start mark, the device receives the data record, that consists of data length, address, record type, write data and checksum. Since the device starts checksum calculation after receiving an end record, the external controller should wait for the checksum after sending the end record. If a receiving error or Intel Hex format error occurs, the device enters the halts condition without returning an error code to the external controller.
13. The n'th - 1 and n'th bytes contain the checksum upper and lower bytes. For details on how to calculate the SUM, refer to " 20.8 Checksum (SUM) ". The checksum is calculated only when the end record is detected and no receiving error or Intel Hex format error occurs. After sending the end

record, the external controller judges whether the transmission is completed correctly by receiving the checksum sent by the device.

14. After transmitting the checksum, the device waits for the next operation command data.

Note 1: Do not write only the address from FFE0H to FFFFH when all flash memory data is the same. If only these area are written, the subsequent operation can not be executed due to password error.

Note 2: To rewrite data to Flash memory addresses at which data (including FFH) is already written, make sure to erase the existing data by "sector erase" or "chip erase" before rewriting data.

20.6.3 RAM Loader Mode (Operation Command: 60H)

Table 20-9 shows RAM loader mode process.

Table 20-9 RAM Loader Mode Process

	Transfer Bytes	Transfer Data from External Controller to T5CL8	Baud Rate	Transfer Data from T5CL8 to External Controller
BOOT ROM	1st byte 2nd byte	Matching data (5AH) -	9600 bps 9600 bps	- (Automatic baud rate adjustment) OK: Echo back data (5AH) Error: Nothing transmitted
	3rd byte 4th byte	Baud rate modification data (See Table 20-4) -	9600 bps 9600 bps	- OK: Echo back data Error: A1H × 3, A3H × 3, 62H × 3 (Note 1)
	5th byte 6th byte	Operation command data (60H) -	Modified baud rate Modified baud rate	- OK: Echo back data (60H) Error: A1H × 3, A3H × 3, 63H × 3 (Note 1)
	7th byte 8th byte	Password count storage address bit 15 to 08 (Note 4)	Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	9th byte 10th byte	Password count storage address bit 07 to 00 (Note 4)	Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	11th byte 12th byte	Password comparison start address bit 15 to 08 (Note 4)	Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	13th byte 14th byte	Password comparison start address bit 07 to 00 (Note 4)	Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	15th byte : m'th byte	Password string (Note 5) -	Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	m'th + 1 byte : n'th - 2 byte	Intel Hex format (Binary) (Note 2)	Modified baud rate Modified baud rate	- -
	n'th - 1 byte	-	Modified baud rate	OK: SUM (Upper byte) (Note 3) Error: Nothing transmitted
	n'th byte	-	Modified baud rate	OK: SUM (Lower byte) (Note 3) Error: Nothing transmitted
RAM	-	The program jumps to the start address of RAM in which the first transferred data is written.		

Note 1: "xxH × 3" indicates that the device enters the halt condition after sending 3 bytes of xxH. For details, refer to " 20.7 Error Code ".

Note 2: Refer to " 20.9 Intel Hex Format (Binary) ".

Note 3: Refer to " 20.8 Checksum (SUM) ".

Note 4: Refer to " 20.10 Passwords ".

Note 5: If addresses from FFE0H to FFFFH are filled with "FFH", the passwords are not compared because the device is considered as a blank product. Transmitting a password string is not required. Even in the case of a blank product , it is required to specify the password count storage address and the password comparison start address. Transmit these data from the external controller. If a password error occurs due to incorrect password count storage address or password comparison start address, T5CL8 stops UART communication and enters the halt condition. Therefore, when a password error occurs, initialize T5CL8 by the $\overline{\text{RESET}}$ pin and reactivate the serial ROM mode.

Note 6: After transmitting a password string, the external controller must not transmit only an end record. If receiving an end record after a password string, the device may not operate correctly.

Note 7: If the security program is enabled or a password error occurs, T5CL8 stops UART communication and enters the halt condition. In this case, initialize T5CL8 by the $\overline{\text{RESET}}$ pin and reactivate the serial PROM mode.

Note 8: If an error occurs during the reception of a password address or a password string, T5CL8 stops UART communication and enters the halt condition. In this case, initialize T5CL8 by the $\overline{\text{RESET}}$ pin and reactivate the serial PROM mode.

Description of RAM loader mode

1. The 1st through 4th bytes of the transmitted and received data contains the same data as in the flash memory writing mode.
2. In the 5th byte of the received data contains the RAM loader command data (60H).
3. When th 5th byte of the received data contains the operation command data shown in Table 1-6, the device echoes back the value which is the same data in the 6th byte position (in this case, 60H). If the 5th byte does not contain the operation command data, the device enters the halt condition after sending 3 bytes of operation command error code (63H).
4. The 7th through m'th bytes of the transmitted and received data contain the same data as in the flash memory writing mode.
5. The m'th + 1 through n'th - 2 bytes of the received data contain the binary data in the Intel Hex format. No received data is echoed back to the external controller. After receiving the start mark (3AH for ":") in the Intel Hex format, the device starts data record reception. Therefore, the received data except 3AH is ignored until the start mark is received. After receiving the start mark, the device receives the data record, that consists of data length, address, record type, write data and checksum. The writing data of the data record is written into RAM specified by address. Since the device starts checksum calculation after receiving an end record, the external controller should wait for the checksum after sending the end record. If a receiving error or Intel Hex format error occurs, the device enters the halts condition without returning an error code to the external controller.
6. The n'th - 1 and n'th bytes contain the checksum upper and lower bytes. For details on how to calculate the SUM, refer to " 20.8 Checksum (SUM) ". The checksum is calculated only when the end record is detected and no receiving error or Intel Hex format error occurs. After sending the end record, the external controller judges whether the transmission is completed correctly by receiving the checksum sent by the device.
7. After transmitting the checksum to the external controller, the boot program jumps to the RAM address that is specified by the first received data record.

Note 1: To rewrite data to Flash memory addresses at which data (including FFH) is already written, make sure to erase the existing data by "sector erase" or "chip erase" before rewriting data.

20.6.4 Flash Memory SUM Output Mode (Operation Command: 90H)

Table 20-10 shows flash memory SUM output mode process.

Table 20-10 Flash Memory SUM Output Process

	Transfer Bytes	Transfer Data from External Controller to T5CL8	Baud Rate	Transfer Data from T5CL8 to External Controller
BOOT ROM	1st byte 2nd byte	Matching data (5AH) -	9600 bps 9600 bps	- (Automatic baud rate adjustment) OK: Echo back data (5AH) Error: Nothing transmitted
	3rd byte 4th byte	Baud rate modification data (See Table 20-4) -	9600 bps 9600 bps	- OK: Echo back data Error: A1H × 3, A3H × 3, 62H × 3 (Note 1)
	5th byte 6th byte	Operation command data (90H) -	Modified baud rate Modified baud rate	- OK: Echo back data (90H) Error: A1H × 3, A3H × 3, 63H × 3 (Note 1)
	7th byte	-	Modified baud rate	OK: SUM (Upper byte) (Note 2) Error: Nothing transmitted
	8th byte	-	Modified baud rate	OK: SUM (Lower byte) (Note 2) Error: Nothing transmitted
	9th byte	(Wait for the next operation command data)	Modified baud rate	-

Note 1: “xxH × 3” indicates that the device enters the halt condition after sending 3 bytes of xxH. For details, refer to " 20.7 Error Code ".

Note 2: Refer to " 20.8 Checksum (SUM) ".

Description of the flash memory SUM output mode

1. The 1st through 4th bytes of the transmitted and received data contains the same data as in the flash memory writing mode.
2. The 5th byte of the received data contains the command data in the flash memory SUM output mode (90H).
3. When the 5th byte of the received data contains the operation command data shown in Table 1-6, the device echoes back the value which is the same data in the 6th byte position of the received data (in this case, 90H). If the 5th byte of the received data does not contain the operation command data, the device enters the halt condition after transmitting 3 bytes of operation command error code (63H).
4. The 7th and the 8th bytes contain the upper and lower bits of the checksum, respectively. For how to calculate the checksum, refer to " 20.8 Checksum (SUM) ".
5. After sending the checksum, the device waits for the next operation command data.

20.6.5 Product ID Code Output Mode (Operation Command: C0H)

Table 20-11 shows product ID code output mode process.

Table 20-11 Product ID Code Output Process

	Transfer Bytes	Transfer Data from External Controller to T5CL8	Baud Rate	Transfer Data from T5CL8 to External Controller	
BOOT ROM	1st byte 2nd byte	Matching data (5AH) -	9600 bps 9600 bps	- (Automatic baud rate adjustment) OK: Echo back data (5AH) Error: Nothing transmitted	
	3rd byte 4th byte	Baud rate modification data (See Table 20-4) -	9600 bps 9600 bps	- OK: Echo back data Error: A1H × 3, A3H × 3, 62H × 3 (Note 1)	
	5th byte 6th byte	Operation command data (C0H) -	Modified baud rate Modified baud rate	- OK: Echo back data (C0H) Error: A1H × 3, A3H × 3, 63H × 3 (Note 1)	
	7th byte		Modified baud rate	3AH	Start mark
	8th byte		Modified baud rate	0AH	The number of transfer data (from 9th to 18th bytes)
	9th byte		Modified baud rate	02H	Length of address (2 bytes)
	10th byte		Modified baud rate	1DH	Reserved data
	11th byte		Modified baud rate	00H	Reserved data
	12th byte		Modified baud rate	00H	Reserved data
	13th byte		Modified baud rate	00H	Reserved data
	14th byte		Modified baud rate	01H	ROM block count (1 block)
	15th byte		Modified baud rate	10H	First address of ROM (Upper byte)
	16th byte		Modified baud rate	00H	First address of ROM (Lower byte)
	17th byte		Modified baud rate	FFH	End address of ROM (Upper byte)
	18th byte		Modified baud rate	FFH	End address of ROM (Lower byte)
	19th byte		Modified baud rate	D2H	Checksum of transferred data (9th through 18th byte)
	20th byte	(Wait for the next operation command data)	Modified baud rate	-	

Note: “xxH × 3” indicates that the device enters the halt condition after sending 3 bytes of xxH. For details, refer to " 20.7 Error Code ".

Description of Product ID code output mode

1. The 1st through 4th bytes of the transmitted and received data contain the same data as in the flash memory writing mode.
2. The 5th byte of the received data contains the product ID code output mode command data (C0H).
3. When the 5th byte contains the operation command data shown in Table 20-6, the device echoes back the value which is the same data in the 6th byte position of the received data (in this case, C0H). If the 5th byte data does not contain the operation command data, the device enters the halt condition after sending 3 bytes of operation command error code (63H).
4. The 9th through 19th bytes contain the product ID code. For details, refer to " 20.11 Product ID Code ".

5. After sending the checksum, the device waits for the next operation command data.

20.6.6 Flash Memory Status Output Mode (Operation Command: C3H)

Table 20-12 shows Flash memory status output mode process.

Table 20-12 Flash Memory Status Output Mode Process

	Transfer Bytes	Transfer Data from External Controller to T5CL8	Baud Rate	Transfer Data from T5CL8 to External Controller	
BOOT ROM	1st byte 2nd byte	Matching data (5AH) -	9600 bps 9600 bps	- (Automatic baud rate adjustment) OK: Echo back data (5AH) Error: Nothing transmitted	
	3rd byte 4th byte	Baud rate modification data (See Table 20-4) -	9600 bps 9600 bps	- OK: Echo back data Error: A1H × 3, A3H × 3, 62H × 3 (Note 1)	
	5th byte 6th byte	Operation command data (C3H) -	Modified baud rate Modified baud rate	- OK: Echo back data (C3H) Error: A1H × 3, A3H × 3, 63H × 3 (Note 1)	
	7th byte		Modified baud rate	3AH	Start mark
	8th byte		Modified baud rate	04H	Byte count (from 9th to 12th byte)
	9th byte		Modified baud rate	00H to 03H	Status code 1
	10th byte		Modified baud rate	00H	Reserved data
	11th byte		Modified baud rate	00H	Reserved data
	12th byte		Modified baud rate	00H	Reserved data
	13th byte		Modified baud rate	Checksum 2's complement for the sum of 9th through 12th bytes 9th byte Checksum 00H: 00H 01H: FFH 02H: FEH 03H: FDH	
	14th byte	(Wait for the next operation command data)	Modified baud rate	-	

Note 1: "xxH × 3" indicates that the device enters the halt condition after sending 3 bytes of xxH. For details, refer to " 20.7 Error Code ".

Note 2: For the details on status code 1, refer to " 20.12 Flash Memory Status Code ".

Description of Flash memory status output mode

1. The 1st through 4th bytes of the transmitted and received data contain the same data as in the Flash memory writing mode.
2. The 5th byte of the received data contains the flash memory status output mode command data (C3H).
3. When the 5th byte contains the operation command data shown in Table 20-6, the device echoes back the value which is the same data in the 6th byte position of the received data (in this case, C3H). If the 5th byte does not contain the operation command data, the device enters the halt condition after sending 3 bytes of operation command error code (63H).
4. The 9th through 13th bytes contain the status code. For details on the status code, refer to " 20.12 Flash Memory Status Code ".
5. After sending the status code, the device waits for the next operation command data.

20.6.7 Flash Memory security program Setting Mode (Operation Command: FAH)

Table 20-13 shows Flash memory security program setting mode process.

Table 20-13 Flash Memory security program Setting Mode Process

	Transfer Bytes	Transfer Data from External Controller to T5CL8	Baud Rate	Transfer Data from T5CL8 to External Controller
BOOT ROM	1st byte 2nd byte	Matching data (5AH) -	9600 bps 9600 bps	- (Automatic baud rate adjustment) OK: Echo back data (5AH) Error: Nothing transmitted
	3rd byte 4th byte	Baud rate modification data (See Table 20-4) -	9600 bps 9600 bps	- OK: Echo back data Error: A1H × 3, A3H × 3, 62H × 3 (Note 1)
	5th byte 6th byte	Operation command data (FAH) -	Modified baud rate Modified baud rate	- OK: Echo back data (FAH) Error: A1H × 3, A3H × 3, 63H × 3 (Note 1)
	7th byte 8th byte	Password count storage address 15 to 08 (Note 2)	Modified baud rate Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	9th byte 10th byte	Password count storage address 07 to 00 (Note 2)	Modified baud rate Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	11th byte 12th byte	Password comparison start address 15 to 08 (Note 2)	Modified baud rate Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	13th byte 14th byte	Password comparison start address 07 to 00 (Note 2)	Modified baud rate Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	15th byte : m'th byte	Password string (Note 2) -	Modified baud rate Modified baud rate	- OK: Nothing transmitted Error: Nothing transmitted
	n'th byte	-	Modified baud rate	OK: FBH (Note 3) Error: Nothing transmitted
	n'+1th byte	(Wait for the next operation command data)	Modified baud rate	-

Note 1: "xxH × 3" indicates that the device enters the halt condition after sending 3 bytes of xxH. For details, refer to " 20.7 Error Code ".

Note 2: Refer to " 20.10 Passwords ".

Note 3: If the security program is enabled for a blank product or a password error occurs for a non-blank product, T5CL8 stops UART communication and enters the halt mode. In this case, initialize T5CL8 by the $\overline{\text{RESET}}$ pin and reactivate the serial PROM mode.

Note 4: If an error occurs during reception of a password address or a password string, T5CL8 stops UART communication and enters the halt mode. In this case, initialize T5CL8 by the $\overline{\text{RESET}}$ pin and reactivate the serial PROM mode.

Description of the Flash memory security program setting mode

1. The 1st through 4th bytes of the transmitted and received data contain the same data as in the Flash memory writing mode.
2. The 5th byte of the received data contains the command data in the flash memory status output mode (FAH).
3. When the 5th byte of the received data contains the operation command data shown in Table 1-6, the device echoes back the value which is the same data in the 6th byte position of the received data (in

this case, FAH). If the 5th byte does not contain the operation command data, the device enters the halt condition after transmitting 3 bytes of operation command error code (63H).

4. The 7th through m’th bytes of the transmitted and received data contain the same data as in the flash memory writing mode.
5. The n'th byte contains the status to be transmitted to the external controller in the case of the successful security program.

20.7 Error Code

When detecting an error, the device transmits the error code to the external controller, as shown in Table 20-14.

Table 20-14 Error Code

Transmit Data	Meaning of Error Data
62H, 62H, 62H	Baud rate modification error.
63H, 63H, 63H	Operation command error.
A1H, A1H, A1H	Framing error in the received data.
A3H, A3H, A3H	Overrun error in the received data.

Note: If a password error occurs, T5CL8 does not transmit an error code.

20.8 Checksum (SUM)

20.8.1 Calculation Method

The checksum (SUM) is calculated with the sum of all bytes, and the obtained result is returned as a word.

The data is read for each byte unit and the calculated result is returned as a word.

Example:

If the data to be calculated consists of the four bytes,
the checksum of the data is as shown below.

A1H + B2H + C3H + D4H = 02EAH
SUM (HIGH)= 02H
SUM (LOW)= EAH

The checksum which is transmitted by executing the flash memory write command, RAM loader command, or flash memory SUM output command is calculated in the manner, as shown above.

20.8.2 Calculation data

The data used to calculate the checksum is listed in Table 20-15.

Table 20-15 Checksum Calculation Data

Operating Mode	Calculation Data	Description
Flash memory writing mode	Data in the entire area of the flash memory	Even when a part of the flash memory is written, the checksum of the entire flash memory area (1000H to FFFH) is calculated. The data length, address, record type and checksum in Intel Hex format are not included in the checksum.
Flash memory SUM output mode		
RAM loader mode	RAM data written in the first received RAM address through the last received RAM address	The length of data, address, record type and checksum in Intel Hex format are not included in the checksum.
Product ID Code Output mode	9th through 18th bytes of the transferred data	For details, refer to " 20.11 Product ID Code ".
Flash Memory Status Output mode	9th through 12th bytes of the transferred data	For details, refer to " 20.12 Flash Memory Status Code "
Flash Memory Erasing mode	All data in the erased area of the flash memory (the whole or part of the flash memory)	When the sector erase is executed, only the erased area is used to calculate the checksum. In the case of the chip erase, an entire area of the flash memory is used.

20.9 Intel Hex Format (Binary)

1. After receiving the checksum of a data record, the device waits for the start mark (3AH ":") of the next data record. After receiving the checksum of a data record, the device ignores the data except 3AH transmitted by the external controller.
2. After transmitting the checksum of end record, the external controller must transmit nothing, and wait for the 2-byte receive data (upper and lower bytes of the checksum).
3. If a receiving error or Intel Hex format error occurs, the device enters the halt condition without returning an error code to the external controller. The Intel Hex format error occurs in the following case:

   When the record type is not 00H, 01H, or 02H

   When a checksum error occurs

   When the data length of an extended record (record type = 02H) is not 02H

   When the device receives the data record after receiving an extended record (record type = 02H) with extended address of 1000H or larger.

   When the data length of the end record (record type = 01H) is not 00H

20.10Passwords

The consecutive eight or more-byte data in the flash memory area can be specified to the password. T5CL8 compares the data string specified to the password with the password string transmitted from the external controller. The area in which passwords can be specified is located at addresses 1000H to FF9FH. The area from FFA0H to FFFFH can not be specified as the passwords area.

If addresses from FFE0H through FFFFH are filled with "FFH", the passwords are not compared because the product is considered as a blank product. Even in this case, the password count storage addresses and password comparison start address must be specified. Table 20-16 shows the password setting in the blank product and non-blank product.

Table 20-16 Password Setting in the Blank Product and Non-Blank Product

Password	Blank Product (Note 1)	Non-Blank Product
PNSA (Password count storage address)	1000H ≤ PNSA ≤ FF9FH	1000H ≤ PNSA ≤ FF9FH
PCSA (Password comparison start address)	1000H ≤ PCSA ≤ FF9FH	1000H ≤ PCSA ≤ FFA0 - N
N (Password count)	*	8 ≤ N
Password string setting	Not required (Note 5)	Required (Note 2)

Note 1: When addresses from FFE0H through FFFFH are filled with "FFH", the product is recognized as a blank product.

Note 2: The data including the same consecutive data (three or more bytes) can not be used as a password. (This causes a password error data. T5CL8 transmits no data and enters the halt condition.)

Note 3: *: Don't care.

Note 4: When the above condition is not met, a password error occurs. If a password error occurs, the device enters the halt condition without returning the error code.

Note 5: In the flash memory writing mode or RAM loader mode, the blank product receives the Intel Hex format data immediately after receiving PCSA without receiving password strings. In this case, the subsequent processing is performed correctly because the blank product ignores the data except the start mark (3AH ":") as the Intel Hex format data, even if the external controller transmits the dummy password string. However, if the dummy password string contains "3AH", it is detected as the start mark erroneously. The microcontroller enters the halt mode. If this causes the problem, do not transmit the dummy password strings.

Note 6: In the flash memory erasing mode, the external controller must not transmit the password string for the blank product.

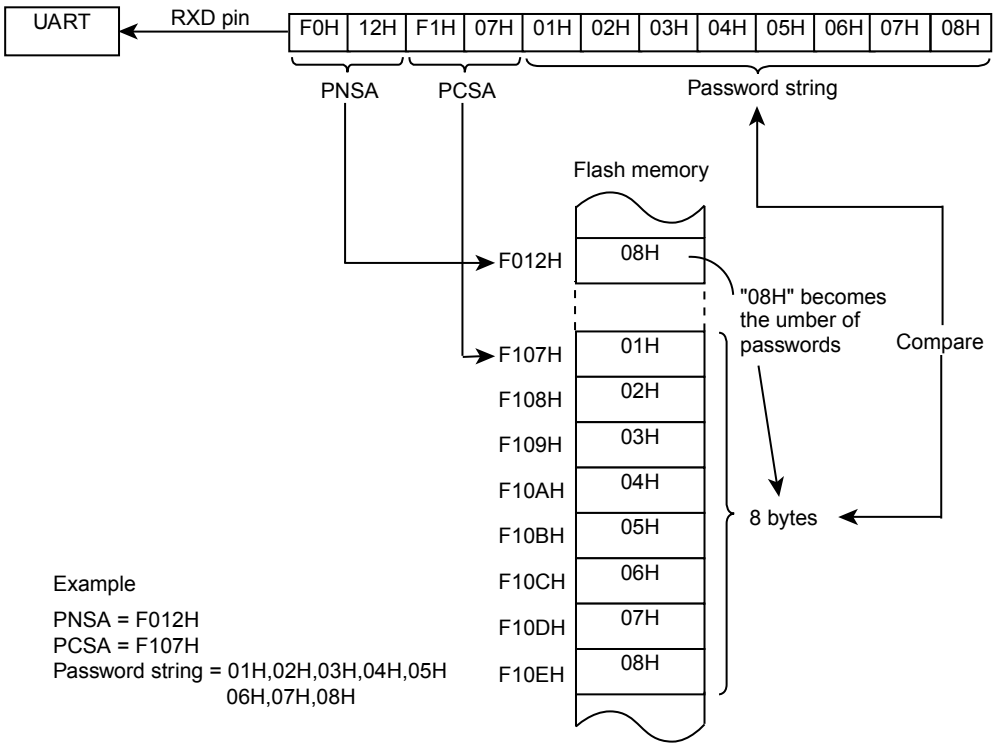


Figure 20-5 Password Comparison

20.10.1Password String

The password string transmitted from the external controller is compared with the specified data in the flash memory. When the password string is not matched to the data in the flash memory, the device enters the halt condition due to the password error.

20.10.2Handling of Password Error

If a password error occurs, the device enters the halt condition. In this case, reset the device to reactivate the serial PROM mode.

20.10.3Password Management during Program Development

If a program is modified many times in the development stage, confusion may arise as to the password. Therefore, it is recommended to use a fixed password in the program development stage.

Example :Specify PNSA to F000H, and the password string to 8 bytes from address F001H
(PCSA becomes F001H.)

```
Password Section code abs = 0F000H

        DB      08H             : PNSA definition

        DB      “CODE1234”      : Password string definition
```

20.11Product ID Code

The product ID code is the 13-byte data containing the start address and the end address of ROM. Table 20-17 shows the product ID code format.

Table 20-17 Product ID Code Format

Data	Description	In the Case of T5CL8
1st	Start Mark (3AH)	3AH
2nd	The number of transfer data (10 bytes from 3rd to 12th byte)	0AH
3rd	Address length (2 bytes)	02H
4th	Reserved data	1DH
5th	Reserved data	00H
6th	Reserved data	00H
7th	Reserved data	00H
8th	ROM block count	01H
9th	The first address of ROM (Upper byte)	10H
10th	The first address of ROM (Lower byte)	00H
11th	The end address of ROM (Upper byte)	FFH
12th	The end address of ROM (Lower byte)	FFH
13th	Checksum of the transferred data (2's compliment for the sum of 3rd through 12th bytes)	D2H

20.12Flash Memory Status Code

The flash memory status code is the 7-byte data including the security program status and the status of the data from FFE0H to FFFFH. Table 20-18 shows the flash memory status code.

Table 20-18 Flash Memory Status Code

Data	Description	In the Case of T5CL8
1st	Start mark	3AH
2nd	Transferred data count (3rd through 6th byte)	04H
3rd	Status code	00H to 03H (See figure below)
4th	Reserved data	00H
5th	Reserved data	00H
6th	Reserved data	00H
7th	Checksum of the transferred data (2's compliment for the sum of 3rd through 6th data)	3rd byte checksum 00H 00H 01H FFH 02H FEH 03H FDH

Status Code 1

7	6	5	4	3	2	1	0	
						RPENA	BLANK	(Initial Value: 0000 00**)

RPENA	Flash memory security program status	0: 1:	Security program is disabled. Security program is enabled.
BLANK	The status from FFE0H to FFFFH.	0: 1:	All data is FFH in the area from FFE0H to FFFFH. The value except FFH is included in the area from FFE0H to FFFFH.

Some operation commands are limited by the flash memory status code 1. If the security program is enabled, flash memory writing mode command and RAM loader mode command can not be executed. Erase all flash memory before executing these command.

RPENA	BLANK	Flash Memory Writing Mode	RAM Loader Mode	Flash memory SUM Output Mode	Product ID Code Output Mode	Flash Memory Status Output Mode	Flash Memory Erasing Mode		Security program Setting Mode
							Chip Erase	Sector Erase	
0	0	m	m	m	m	m	m		×
0	1	Pass	Pass	m	m	m	Pass		Pass
1	0	×	×	m	m	m	m	×	×
1	1	×	×	m	m	m	Pass	×	Pass

Note: m: The command can be executed.
Pass: The command can be executed with a password.
×: The command can not be executed.
(After echoing the command back to the external controller, T5CL8 stops UART communication and enters the halt condition.)

20.13Specifying the Erasure Area

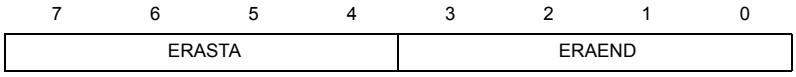
In the flash memory erasing mode, the erasure area of the flash memory is specified by n−2 byte data.

The start address of an erasure area is specified by ERASTA, and the end address is specified by ERAEND.

If ERASTA is equal to or smaller than ERAEND, the sector erase (erasure in 4 kbyte units) is executed. Executing the sector erase while the security program is enabled results in an infinite loop.

If ERASTA is larger than ERAEND, the chip erase (erasure of an entire flash memory area) is executed and the security program is disabled. Therefore, execute the chip erase (not sector erase) to disable the security program.

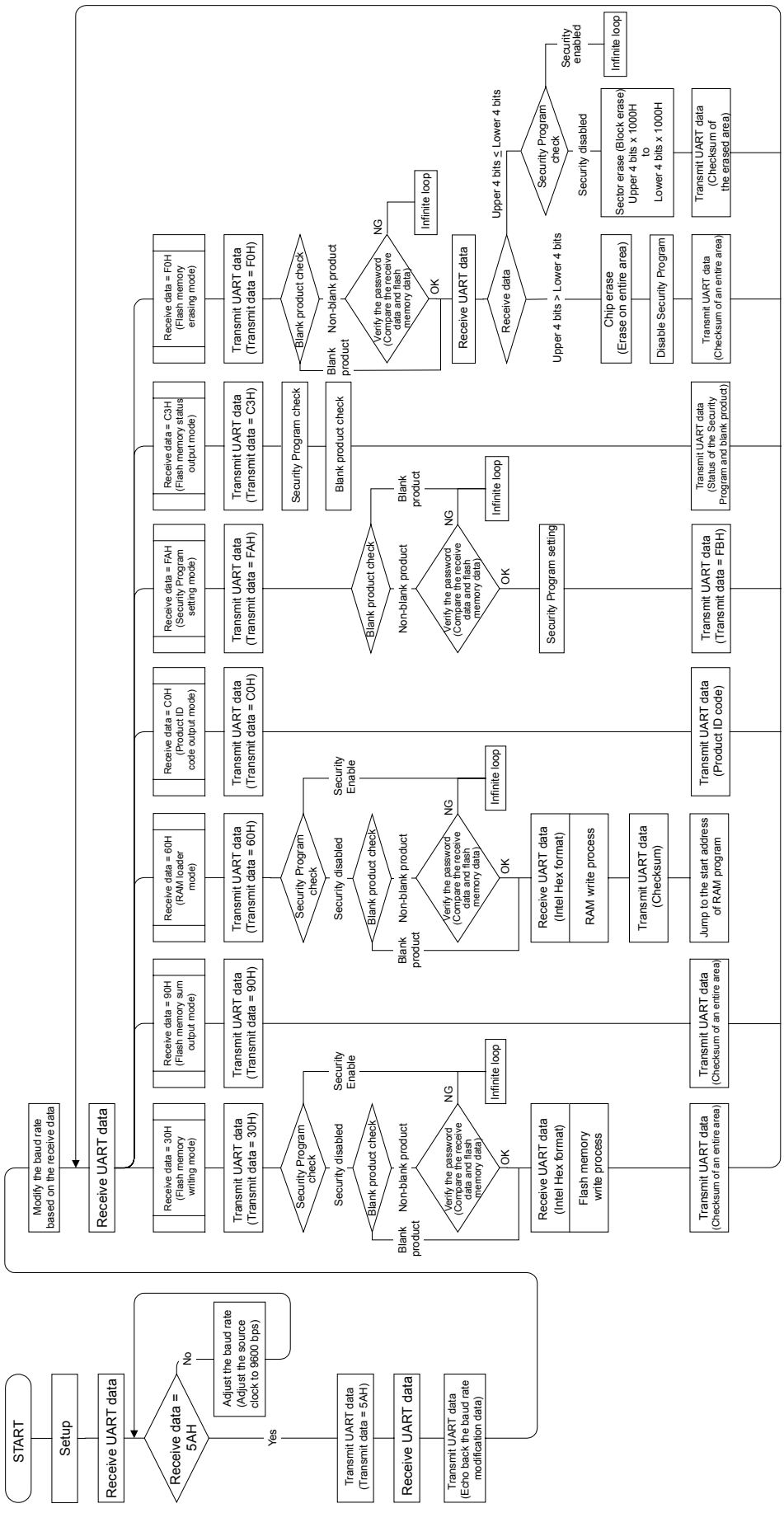
Erasure Area Specification Data (n−2 byte data)



ERASTA	The start address of the erasure area	0000: from 0000H 0001: from 1000H 0010: from 2000H 0011: from 3000H 0100: from 4000H 0101: from 5000H 0110: from 6000H 0111: from 7000H 1000: from 8000H 1001: from 9000H 1010: from A000H 1011: from B000H 1100: from C000H 1101: from D000H 1110: from E000H 1111: from F000H
ERAEND	The end address of the erasure area	0000: to 0FFFH 0001: to 1FFFH 0010: to 2FFFH 0011: to 3FFFH 0100: to 4FFFH 0101: to 5FFFH 0110: to 6FFFH 0111: to 7FFFH 1000: to 8FFFH 1001: to 9FFFH 1010: to AFFFH 1011: to BFFFH 1100: to CFFFH 1101: to DFFFH 1110: to EFFFH 1111: to FFFFH

Note: When the sector erase is executed for the area containing no flash cell, T5CL8 stops the UART communication and enters the halt condition.

20.14Flowchart


START
Setup
Receive UART data
Receive data = 5AH
No
Adjust the baud rate (Adjust the source clock to 9600 bps)
Yes
Transmit UART data (Transmit data = 5AH)
Receive UART data
Transmit UART data (Echo back the baud rate modification data)
Modify the baud rate based on the receive data
Receive UART data
Receive data = 30H (Flash memory writing mode)
Transmit UART data (Transmit data = 30H)
Security Program check
Security disabled
Security Enable
Blank product check
Non-blank product
Blank product
Verify the password (Compare the receive data and flash memory data)
NG
OK
Infinite loop
Receive UART data (Intel Hex format)
Flash memory write process
Transmit UART data (Checksum of an entire area)
Receive data = 90H (Flash memory sum output mode)
Transmit UART data (Transmit data = 90H)
Transmit UART data (Checksum of an entire area)
Receive data = 60H (RAM loader mode)
Transmit UART data (Transmit data = 60H)
Security Program check
Security disabled
Security Enable
Blank product check
Non-blank product
Blank product
Verify the password (Compare the receive data and flash memory data)
NG
OK
Infinite loop
Receive UART data (Intel Hex format)
RAM write process
Transmit UART data (Checksum)
Jump to the start address of RAM program
Receive data = C0H (Product ID code output mode)
Transmit UART data (Transmit data = C0H)
Transmit UART data (Product ID code)
Receive data = FAH (Security Program setting mode)
Transmit UART data (Transmit data = FAH)
Blank product check
Non-blank product
Blank product
Verify the password (Compare the receive data and flash memory data)
NG
OK
Infinite loop
Security Program setting
Transmit UART data (Transmit data = FBH)
Receive data = C3H (Flash memory status output mode)
Transmit UART data (Transmit data = C3H)
Security Program check
Blank product check
Transmit UART data (Status of the Security Program and blank product)
Receive data = F0H (Flash memory erasing mode)
Transmit UART data (Transmit data = F0H)
Blank product check
Non-blank product
Blank product
Verify the password (Compare the receive data and flash memory data)
NG
OK
Infinite loop
Receive UART data
Receive data
Upper 4 bits ≤ Lower 4 bits
Upper 4 bits > Lower 4 bits
Security Program check
Security enabled
Infinite loop
Security disabled
Chip erase (Erase on entire area)
Disable Security Program
Sector erase (Block erase) Upper 4 bits x 1000H to Lower 4 bits x 1000H
Transmit UART data (Checksum of an entire area)
Transmit UART data (Checksum of the erased area)

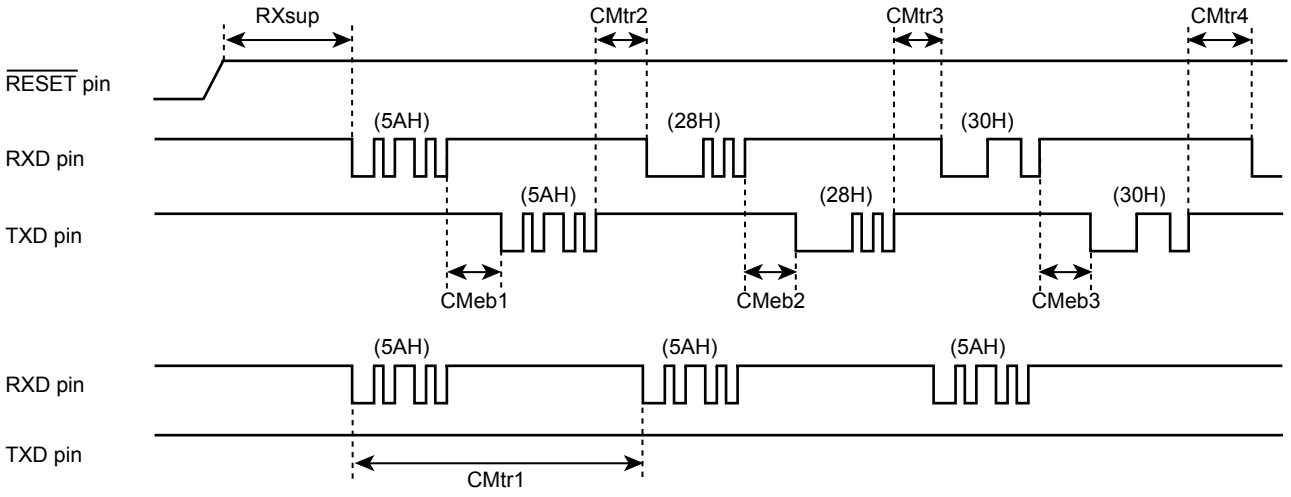
20.15UART Timing

Table 20-19 UART Timing-1 (VDD = 4.5 to 5.5 V, fc = 2 to 16 MHz, Topr = -10 to 40°C)

Parameter	Symbol	Clock Frequency (fc)	Minimum Required Time	
			At fc = 2 MHz	At fc = 16 MHz
Time from matching data reception to the echo back	CMeb1	Approx. 930	465 μs	58.1 μs
Time from baud rate modification data reception to the echo back	CMeb2	Approx. 980	490 μs	61.3 μs
Time from operation command reception to the echo back	CMeb3	Approx. 800	400 μs	50 μs
Checksum calculation time	CKsm	Approx. 7864500	3.93 s	491.5 μs
Erasure time of an entire flash memory	CEall	-	30 ms	30 ms
Erasure time for a sector of a flash memory (in 4-kbyte units)	CEsec	-	15 ms	15 ms

Table 20-20 UART Timing-2 (VDD = 4.5 to 5.5 V, fc = 2 to 16 MHz, Topr = -10 to 40°C)

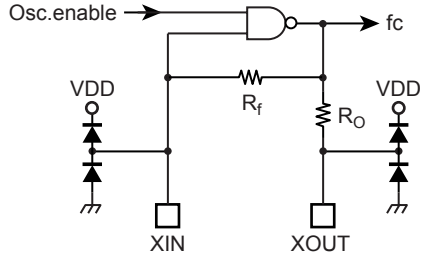
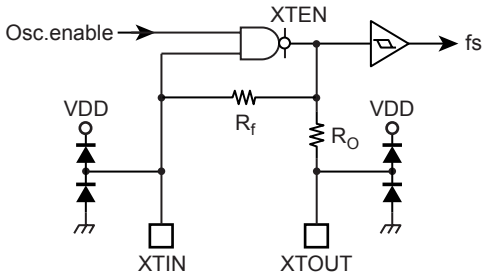
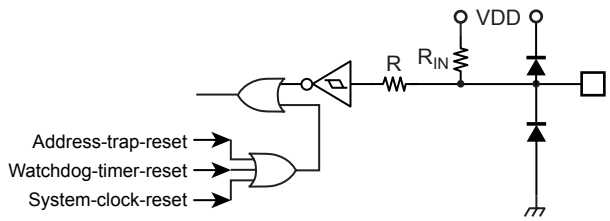
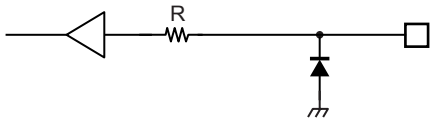
Parameter	Symbol	Clock Frequency (fc)	Minimum Required Time	
			At fc = 2 MHz	At fc = 16 MHz
Time from the reset release to the acceptance of start bit of RXD pin	RXsup	2100	1.05 ms	131.3 ms
Matching data transmission interval	CMtr1	28500	14.2 ms	1.78 ms
Time from the echo back of matching data to the acceptance of baud rate modification data	CMtr2	380	190 μs	23.8 μs
Time from the echo back of baud rate modification data to the acceptance of an operation command	CMtr3	650	325 μs	40.6 μs
Time from the echo back of operation command to the acceptance of password count storage addresses (Upper byte)	CMtr4	800	400 μs	50 μs



21. Input/Output Circuit

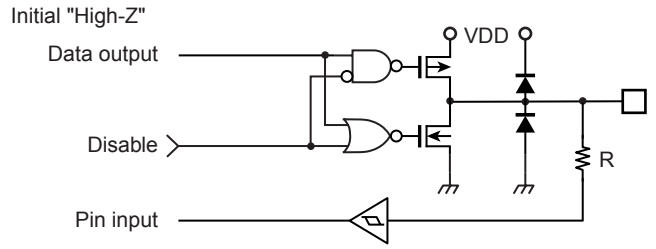
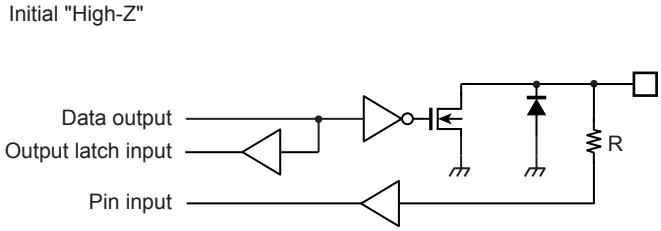
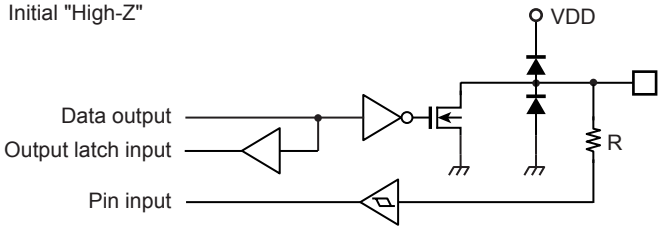
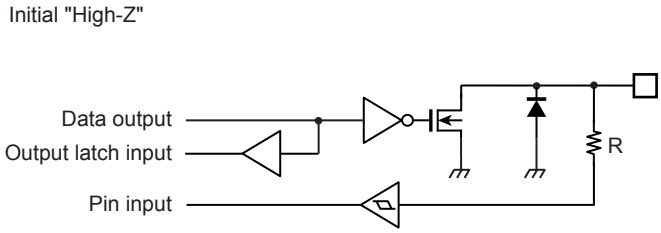
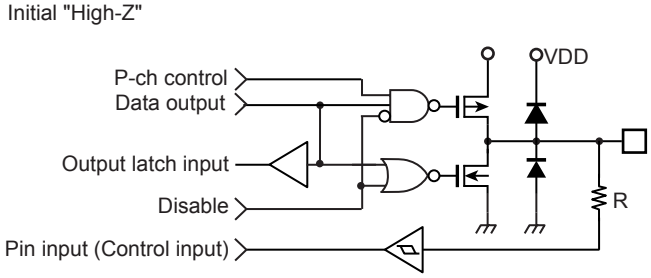
21.1 Control pins

The input/output circuitries of the T5CL8 control pins are shown below.

Control Pin	I/O	Input/Output Circuitry	Remarks
XIN XOUT	Input Output		Resonator connecting pins (high frequency) R_f = 1.2 MΩ (typ.) R_O =0.5 kΩ (typ.)
XTIN XTOUT	Input Output		Resonator connecting pins (Low frequency) R_f = 6 MΩ (typ.) R_O = 220 kΩ (typ.)
$\overline{\text{RESET}}$	Input		Hysteresis input Pull-up resistor R_{IN} = 220 kΩ (typ.) R = 100 Ω (typ.)
TEST	Input		R = 100 Ω (typ.)

Note: The TEST pin of the T5CL8 does not have a pull-down resistor and a protection diode on the VDD side. Therefore, fix the TEST pin at Low-level.

21.2 Input/Output Ports

Port	I/O	Input/Output Circuitry	Remarks
P1	I/O		Tri-state I/O Hysteresis input R = 100 Ω (typ.)
P3	I/O		Sink open drain output High current output R = 100 Ω (typ.)
P2	I/O		Sink open drain output Hysteresis input R = 100 Ω (typ.)
P5	I/O		Sink open drain output High current output Hysteresis input R = 100 Ω (typ.)
P0 P4	I/O		Sink open drain output or C-MOS output Hysteresis input R = 100 Ω (typ.)

Port	I/O	Input/Output Circuitry	Remarks
P67 P66 P65 P64	I/O	Initial "High-Z" Analog input Data output Output latch input Disable Pin input Key-on Wakeup VDD R	Tri-state I/O R = 100 Ω (typ.)
P63 P62 P61 P60 P7	I/O	Initial "High-Z" Analog input Data output Output latch input Disable Pin input VDD R	Tri-state I/O R = 100 Ω (typ.)

22. Electrical Characteristics

22.1 Absolute Maximum Ratings

The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

(VSS = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply voltage	V_{DD}		-0.3 to 6.0	V
Input voltage	V_{IN}		-0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT1}		-0.3 to V_{DD} + 0.3	V
Output current (Per 1 pin)	I_{OUT1}	P0, P1, P4, P6, P7 ports	-1.8	mA
	I_{OUT2}	P0, P1, P2, P4, P6, P7 ports	3.2	
	I_{OUT3}	P3, P5 ports	30	
Output current (Total)	ΣI_{OUT1}	P0, P1, P2, P4, P6, P7 ports	60	
	ΣI_{OUT2}	P3, P5 ports	80	
Power dissipation [Topr = 85 °C]	P_D		250	mW
Soldering temperature (time)	Tsld		260 (10 s)	°C
Storage temperature	Tstg		-55 to 125	
Operating temperature	Topr		-40 to 85	

22.2 Operating Conditions

The Operating Conditions shows the conditions under which the device be used in order for it to operate normally while maitaining its quality. If the device is used outside the range of Operating Conditions (power supply voltage, operating temperature range, or AC/DC rated values), it may operate erratically. Therefore, when designing your application equipment, always make sure its intended working conditions will not exceed the range of Operating Conditions.

22.2.1 MCU mode (Flash Programming or erasing)

(V_{SS} = 0 V, Topr = -10 to 40°C)

Parameter	Symbol	Pins	Ratings	Min	Max	Unit
Supply voltage	V_{DD}		NORMAL1, 2 modes	4.5	5.5	V
Input high level	V_{IH1}	Except hysteresis input	$V_{DD} \geq 4.5$ V	$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$		
Input low level	V_{IL1}	Except hysteresis input	$V_{DD} \geq 4.5$ V	0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$	
Clock frequency	fc	XIN, XOUT		1.0	16.0	MHz

22.2.2 MCU mode (Except Flash Programming or erasing)

(V_{SS} = 0 V, Topr = -40 to 85°C)

Parameter	Symbol	Pins	Ratings		Min	Max	Unit
Supply voltage	V_{DD}		fc = 16 MHz	NORMAL1, 2 modes IDLE0, 1, 2 modes	4.5	5.5	V
			fc = 8 MHz	NORMAL1, 2 modes IDLE0, 1, 2 modes	2.7		
			fs = 32.768 KHz	SLOW1, 2 modes SLEEP0, 1, 2 modes			
			STOP mode				
Input high level	V_{IH1}	Except hysteresis input	$V_{DD} \geq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input low level	V_{IL1}	Except hysteresis input	$V_{DD} \geq 4.5$ V		0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock frequency	fc	XIN, XOUT	V_{DD} = 2.7 to 5.5V		1.0	8.0	MHz
			V_{DD} = 4.5 to 5.5V			16.0	
	fs	XTIN, XTOUT	V_{DD} = 2.7 to 5.5V		30.0	34.0	kHz

22.2.3 Serial PROM mode

(V_{SS} = 0 V, Topr = -10 to 40 °C)

Parameter	Symbol	Pins	Condition	Min	Max	Unit
Supply voltage	V_{DD}		NORMAL1, 2 modes	4.5	5.5	V
Input high voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geq 4.5$ V	$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$		
Input low voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geq 4.5$ V	0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$	
Clock frequency	fc	XIN, XOUT		2.0	16.0	MHz

22.3 DC Characteristics

(V_{SS} = 0 V, Topr = -40 to 85 °C)

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit
Hysteresis voltage	V_{HS}	Hysteresis input	V_{DD} = 5.5 V, V_{IN} = V_{TEST} = 5.5 V/0 V	–	0.9	–	V
Input current	I_{IN1}	TEST		–	–	±2	μA
	I_{IN2}	Sink open drain, tri–state port					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input resistance	R_{IN2}	$\overline{RESET}$ pull–up	V_{DD} = 5.5 V, V_{IN} = 0 V	100	220	450	kΩ
Output leakage current	I_{LO1}	Sink open drain port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	–	–	2	μA
	I_{LO2}	Tri–state port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0 V	–	–	±2	
Output high voltage	V_{OH}	Tri–state port	V_{DD} = 4.5 V, I_{OH} = -0.7 mA	4.1	–	–	V
Output low voltage	V_{OL}	Except XOUT, P3, P5	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	
Output low curren	I_{OL}	High current port (P3, P5 Port)	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	mA
Supply current in NORMAL1, 2 modes	I_{DD}		V_{DD} = 5.5 V, V_{IN} = 5.3 V/0.2 V, V_{TEST} = 5.3 V/0.1 V, When a program operates on flash memory (Note5,6)	–	9	16	mA
Supply current in IDLE 0, 1, 2 modes			fc = 16 MHz, fs = 32.768 kHz	–	6	8	
Supply current in SLOW1 mode			V_{DD} = 3.0 V, V_{IN} = 2.8 V/0.2 V, V_{TEST} = 2.8 V/0.1 V, fs = 32.768 kHz, When a program operates on flash memory (Note5,6)	–	27	260	μA
			When a program operates on RAM	–	10	15	
Supply current in SLEEP1 mode				–	6.5	13	
Supply current in SLEEP0 mode				–	6	12	
Supply current in STOP mode			V_{DD} = 5.5 V, V_{IN} = 5.3 V/0.2 V, V_{TEST} = 5.3 V/0.1 V	–	0.5	10	
Peak current for SLOW1 mode (Note5,6)	I_{DDP-P}		V_{DD} = 5.5 V, V_{IN} = 5.3 V/0.2 V, V_{TEST} = 5.3 V/0.1 V, Topr = -10 to 40 °C	–	10	–	mA
			V_{DD} = 3.0 V, V_{IN} = 2.8 V/0.2 V, V_{TEST} = 2.8 V/0.1 V, Topr = -10 to 40 °C	–	2	–	
Write / Erase / Security program current for Flash memory (Note7,8)	I_{DDEW}		V_{DD} = 5.5 V, V_{IN} = 5.3 V/0.2 V, V_{TEST} = 5.3 V/0.1 V, Topr = -10 to 40 °C	–	26	–	mA

Note 1: Typical values show those at Topr = 25°C and V_{DD} = 5 V.

Note 2: Input current (I_{IN3}): The current through pull-up resistor is not included.

Note 3: I_{DD} does not include I_{REF}.

Note 4: The supply currents of SLOW2 and SLEEP2 modes are equivalent to those of IDLE0, IDLE1 and IDLE2 modes.

Note 5: When a program is executing in the flash memory or when data is being read from the flash memory, the flash memory operates in an intermittent manner, causing peak currents in the operation current, as shown in Figure 22-1. In this case, the supply current I_{DD} (in NORMAL1, NORMAL2 and SLOW1 modes) is defined as the sum of the average peak current and MCU current.

Note 6: When designing the power supply, make sure that peak currents can be supplied. The internal supply voltage of this device may be changed by this peak current. Thus, it needs a bypass capacitor (about 0.1μF) near its power terminal to stabilize its operation. In SLOW1 mode, the difference between the peak current and the average current becomes large.

Note 7: If a write or erase is performed on the flash memory or a security program is enabled in the flash memory, an instantaneous peak current flows, as shown in Figure 22-2.

Note 8: The circuit of a power supply must be designed such as to enable the supply of a peak current. This peak current causes the supply voltage in the device to fluctuate. Connect a bypass capacitor of about 0.1μF near the power supply of the device to stabilize its operation.

Note 9: V_{IN} is supply volage to the terminals except for TEST pin. V_{TEST}: is supply voltage for TEST pin.

Note 10:To execute the Program, Erase and Security Program commands on the flash memory, the temperature must be kept within Topr = -10 to 40 degree celsius. If this temperature range is not observed, operation cannot be guaranteed.

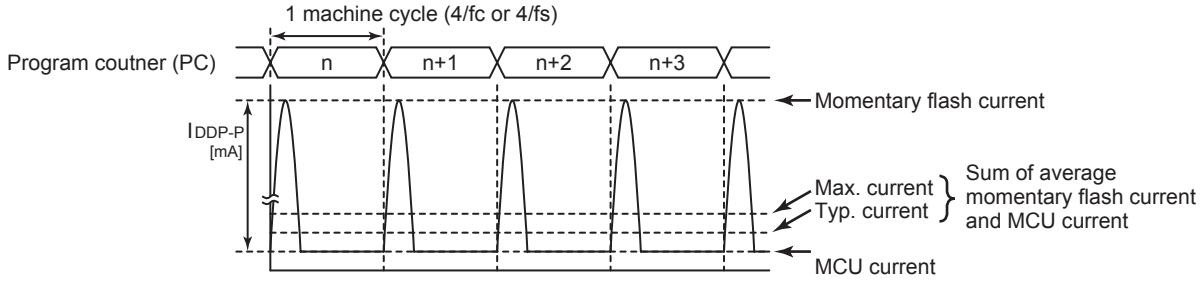


Figure 22-1 Intermittent Operation of Flash Memory

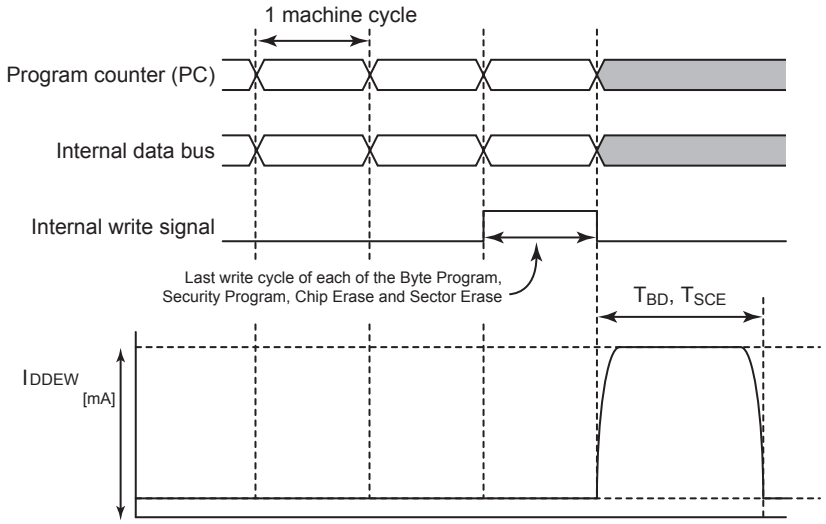

1 machine cycle
Program counter (PC)
Internal data bus
Internal write signal
Last write cycle of each of the Byte Program, Security Program, Chip Erase and Sector Erase
TBD, TSCE
IDDEW
[mA]

Figure 22-2 Current When an Erase or Program is Being Performed on the Flash Memory

22.4 AD Characteristics

(V_{SS} = 0.0 V, 4.5 V ≤ V_{DD} ≤ 5.5 V, Topr = -40 to 85 °C)

Paramete	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} - 1.0	–	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			
Analog reference voltage range (Note 4)	Δ V_{AREF}		3.5	–	–	
Analog input voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power supply current of analog reference voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 5.5 V V_{SS} = 0.0 V	–	0.6	1.0	mA
Non linearity error		V_{DD} = A_{VDD} = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.0 V	–	–	±2	LSB
Zero point error			–	–	±2	
Full scale error			–	–	±2	
Total error			–	–	±2	

(V_{SS} = 0 V, 2.7 V ≤ V_{DD} < 4.5 V, Topr = -40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage	V_{AREF}		A_{VDD} - 1.0	–	A_{VDD}	V
Power supply voltage of analog control circuit	A_{VDD}		V_{DD}			
Analog reference voltage range (Note 4)	Δ V_{AREF}		2.5	–	–	
Analog input voltage	V_{AIN}		V_{SS}	–	V_{AREF}	
Power supply current of analog reference voltage	I_{REF}	V_{DD} = A_{VDD} = V_{AREF} = 4.5 V V_{SS} = 0.0 V	–	0.5	0.8	mA
Non linearity error		V_{DD} = A_{VDD} = 2.7 V V_{SS} = 0.0 V V_{AREF} = 2.7 V	–	–	±2	LSB
Zero point error			–	–	±2	
Full scale error			–	–	±2	
Total error			–	–	±2	

Note 1: The total error includes all errors except a quanitization error, and is defined as a maximum deviation from the ideal conversion line.

Note 2: Conversion time is defferent in recommended value by power supply voltage.

Note 3: The voltage to be input on the AIN input pin must not exceed the range between V_{AREF} and V_{SS}. If a voltage outside this range is input, conversion values will become unstable and conversion values of other channels will also be affected.

Note 4: Analog reference voltage range: $\Delta V_{AREF} = V_{AREF} - V_{SS}$

Note 5: When AD converter is not used, fix the AVDD and VAREF pin on the V_{DD} level.

22.5 AC Characteristics

(V_{SS} = 0 V, 4.5 V ≤ V_{DD} ≤ 5.5 V, Topr = -40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	tcy	NORMAL1, 2 modes	0.25	–	4	μs
		IDLE0, 1, 2 modes				
		SLOW1, 2 modes	117.6	–	133.3	
		SLEEP0, 1, 2 modes				
High-level clock pulse width	t_{WCH}	For external clock operation (XIN input) fc = 16 MHz	–	31.25	–	ns
Low-level clock pulse width	t_{WCL}					
High-level clock pulse width	t_{WSH}	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low-level clock pulse width	t_{WSL}					

(V_{SS} = 0 V, 2.7 V ≤ V_{DD} < 4.5 V, Topr = -40 to 85°C)

Paramete	Symbol	Condition	Min	Typ.	Max	Unit
Machine cycle time	t_{cy}	NORMAL1, 2 modes	0.5	–	4	μs
		IDLE0, 1, 2 modes				
		SLOW1, 2 modes	117.6	–	133.3	
		SLEEP0, 1, 2 modes				
High-level clock pulse width	t_{WCH}	For external clock operation (XIN input) fc = 8 MHz	–	62.5	–	ns
Low-level clock pulse width	t_{WCL}					
High-level clock pulse width	t_{WSH}	For external clock operation (XTIN input) fs = 32.768 kHz	–	15.26	–	μs
Low-level clock pulse width	t_{WSL}					

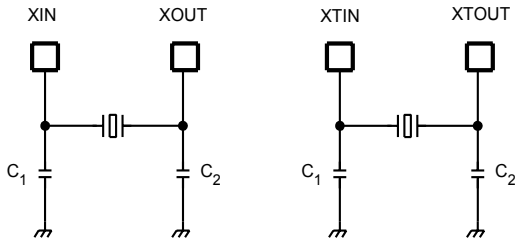
22.6 Flash Characteristics

22.6.1 Write/Retention Characteristics

(V_{SS} = 0 V)

Paramete	Condition	Min	Typ.	Max.	Unit
Number of guaranteed writes to flash memory	V_{SS} = 0 V, Topr = -10 to 40°C	–	–	100	Times

22.7 Recommended Oscillating Conditions



(1) High-frequency Oscillation (2) Low-frequency Oscillation

Note 1: To ensure stable oscillation, the resonator position, load capacitance, etc. must be appropriate. Because these factors are greatly affected by board patterns, please be sure to evaluate operation on the board on which the device will actually be mounted.

Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL:
http://www.murata.com/

22.8 Handling Precaution

- The solderability test conditions for lead-free products (indicated by the suffix G in product name) are shown below.
  1. When using the Sn-37Pb solder bath
     Solder bath temperature = 230 °C
     Dipping time = 5 seconds
     Number of times = once
     R-type flux used
  2. When using the Sn-3.0Ag-0.5Cu solder bath
     Solder bath temperature = 245 °C
     Dipping time = 5 seconds
     Number of times = once
     R-type flux used

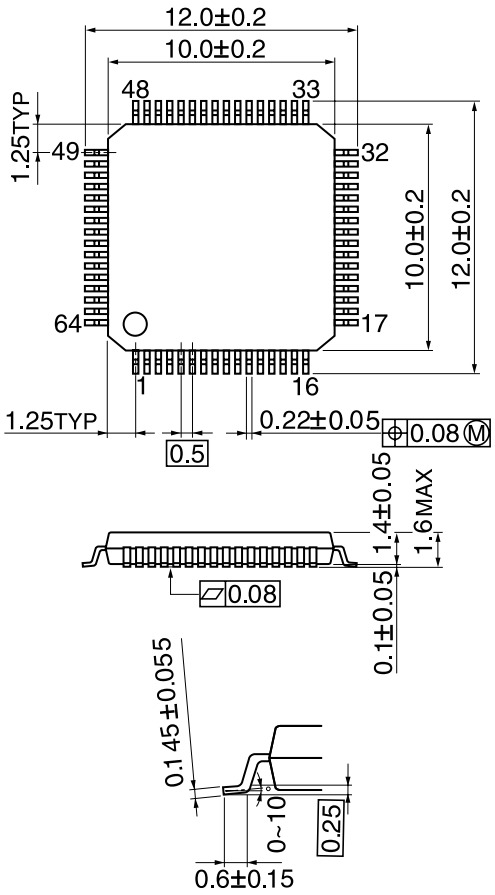
  Note: The pass criteron of the above test is as follows:
  Solderability rate until forming ≥ 95 %

- When using the device (oscillator) in places exposed to high electric fields such as cathode-ray tubes, we recommend electrically shielding the package in order to maintain normal operating condition.

23. Package Dimensions

LQFP64-P-1010-0.50D Rev 01

Unit: mm



This is a technical document that describes the operating functions and electrical specifications of the 8-bit microcontroller series TLCS-870/C (LSI).

Toshiba provides a variety of development tools and basic software to enable efficient software development.

These development tools have specifications that support advances in microcomputer hardware (LSI) and can be used extensively. Both the hardware and software are supported continuously with version updates.

The recent advances in CMOS LSI production technology have been phenomenal and microcomputer systems for LSI design are constantly being improved. The products described in this document may also be revised in the future. Be sure to check the latest specifications before using.

Toshiba is developing highly integrated, high-performance microcomputers using advanced MOS production technology and especially well proven CMOS technology.

We are prepared to meet the requests for custom packaging for a variety of application areas.
We are confident that our products can satisfy your application needs now and in the future.

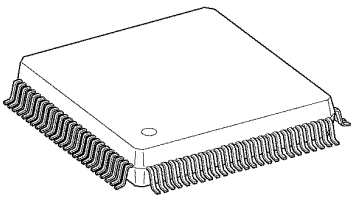
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC94B14MFG

SiP(System in Package) LSI of; Single-Chip Digital Servo Processor incorporating CD Head Amplifier/Compression
AudioDecoder and 16Mbit DRAM for ESP(Electrical Shock Proof) function.

The TC94B14MFG is a single chip processor which incorporates the following functions:
CD Head amplifier, EFM synchronous signal separation protection and interpolation, EFM demodulation, error correction, microcontroller interface, servo-use digital equalizer and servo control circuit, multi bit DA converter and Compression audio decoder firmware such as for MP3, WMA , MPEG4-AAC and 16Mbit DRAM for ESP.

The TC94B14MFG makes it possible to configure a CD-MP3 player with ESP quite easily with an adjustment-free basis.



LQFP80−P−1212−0.50F

Weight: 0.6g (typ.)

Features

[General]

Common to all sections

- Operation Supply Voltage : CD, I/O, DAC：3.0 – 3.6V,
  DSP Logic, 1MbitSRAM：1.4-1.6V
- Stand-By function：Hold the data stores in 1MbitSRAM supplying the Voltage only to 1MbitSRAM
- Operation Temperature : - 20 ~ 70 °C
- Package, LQFP-80, Pin pitch 0.5 mm
- Micro controller interface: 4bit parallel interface(6 lines),
- CMOS silicon Monolithic LSI

[Head amplifier section]

- CD-DA/R/RW : up to x2 speed.
- Built-in reference voltage (VRO) generation circuit.
- Built-in APC (auto laser power control) circuit.
- Built-in RF signal generation circuit.
- Enables the polarity of the offset voltage correction of the RF signal to be switched.
- Built-in AGC (auto gain control) circuit for the RF signal. (gain adjustment range of ±6 dB)
- Built-in RF equalizer correction circuit.
- Built-in focus error signal and tracking error signal circuits.
- Built-in signal generation circuit for track counting(RFRP).
- Built-in circuit for generating a sub beam addition signal or an RFDC signal, whichever is selected, as a defect. detection signal. (Note that the RFDC signal is supported only when the RFO signal is positive.)
- Supports DC offset correction functions (for focus, tracking, and RF sections).
- Supports both CD-DA and CD-R/RW modes.
- Supports a voltage output type pickup.

[Digital servo processor section]

- Capable of decoding text data (CD-TEXT mode 4).
- Capable of performing sync pattern detection, sync signal protection and interpolation securely.
- Built-in EFM demodulation circuit and sub code demodulation circuit
- Has a jitter absorbing capacity be switched among ±6 frames and ±22 frames.
- Capable of making double C1 correction and quadruple C2 correction, using CIRC correction logical expressions.
- Built-in 64Kbit RAM
- Built-in digital attenuators
- Enables audio outputs to be switched among 32 fs, 48 fs, and 64 fs.
- Capable of reading sub code Q data at any time and outputting it in synchronization with audio data.
- Built-in data slice circuit (analog/digital slicing) and compensation circuit
- Built-in analog PLL (with an adjustment-free VCO)
- Uses an active wide-range PLL system.
- Supports variable-speed playback.
- Supports CLV modes (for up to ×2 speed)
- Supporting automatic loop gain, offset, and balance adjustments for focus and tracking servo sections.
- Built-in RF gain automatic adjustment circuit
- Built-in digital equalizer
- Built-in digital equalizer coefficient RAM, supporting various pickup types
- Built-in focus and tracking servo control circuits
- Supports all search control modes, thus realizing high-speed stable searches.
- Uses speed-controlled lens kick and feed kick.
- Built-in AFC and APC circuits for disc motor CLV servo control
- Built-in anti-defect and anti-shock circuits
- Support Stepper Motor

[Audio DSP section]

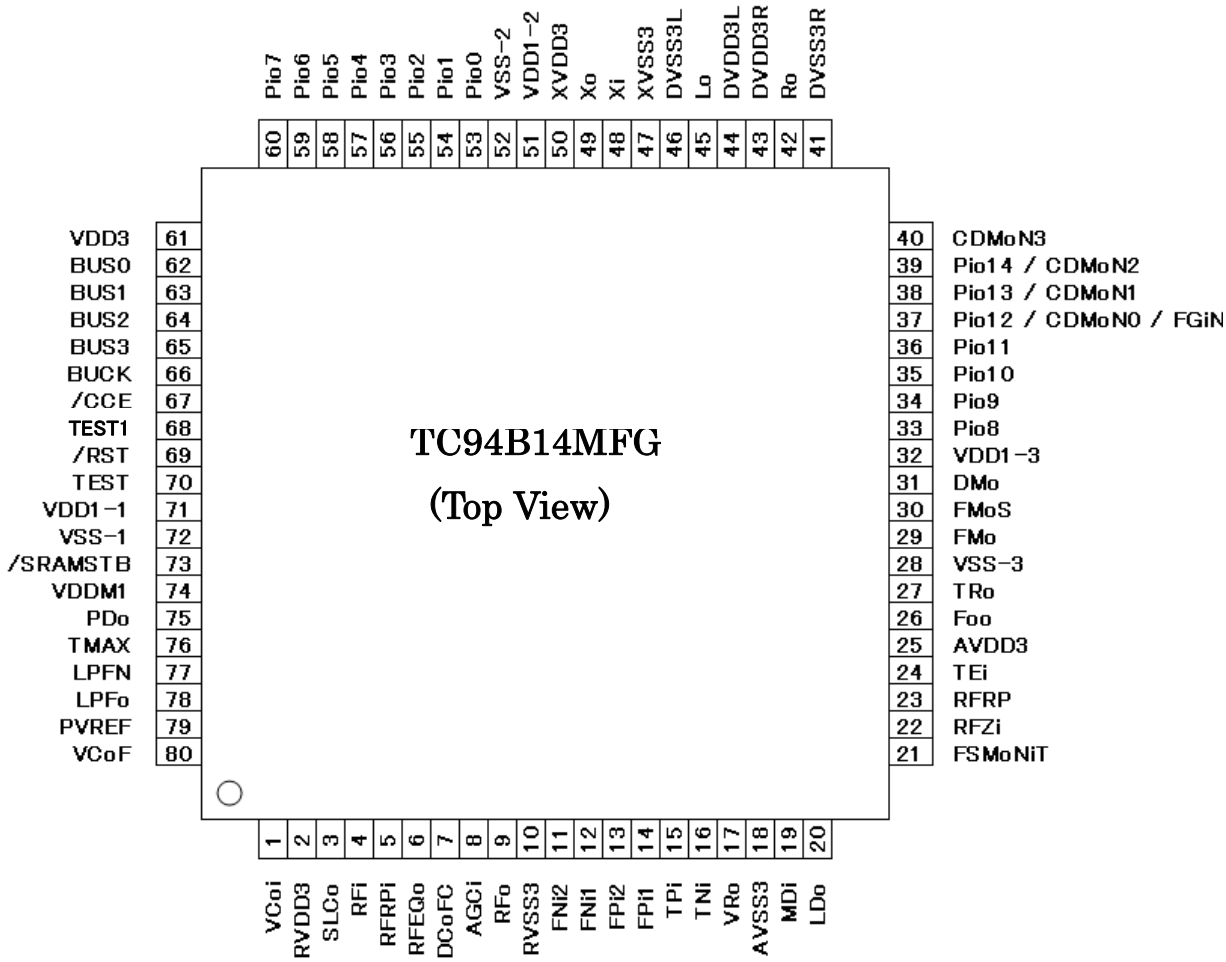
- Incorporating firmware for processing signals in various audio compression formats such as MP3, WMA, and MPEG4-AAC.
- Incorporating 1 Mbit of SRAM (128 Kwords × 8 bits)
- Operation Clock : Built-in PLL for generating clock pulses for operation of the DSP block; any frequency can be specified for clock pulses to be generated
- Operating speed : 87.5MIPS
- DSP block having the following specifications:
  Operation block: 24 bits × 24 bits + 51-bit multiplier, and 51-bit ALU
  Data buss : 24 bits × 3
  Data RAM : 12 Kwords
  Coefficient ROM : 44 Kwords
  Program RAM : 1 Kwords
  Program ROM : 36 Kwords
- Audio Input port : 2 (Supports 3line PCM and I2S, 32/48/64fs)
- Audio Output port : 1 (Support 3 line PCM and I2S, 32/48/64fs)
- SPDIF Output

[Audio DAC section]

- Supports externally input BCKi, LRCKi, Ai signals.
- Built-in 24-bit FIR digital filter for lower in-band ripple(less than +/- 0.025dB and high attenuation(less than -60dB) on out of the band
- Built-in ×8 over-sampling digital filter

Pin Layout and Block Diagram (Top View)

Pin Layout (Top View)



Pin Descriptions

1.1 Pin Descriptions

Pin No.	Symbol	I/O	Description	Default	Remarks
1	VCOI	O 3AI/F	DSP VCO - EFM and PLCK Phase difference signal output pin. (DSP VCO control voltage inputr pin.)	O	3 state output
2	RVDD3	-	CD-DSP-Power supply for 3.3V RF amplifier core and PLL circuit	-	
3	SLCo	O 3AI/F	EFM slice level output pin	O	Connect capacitor according with servo frequency band.
4	RFi	I 3AI/F	RF signal input pin	I	Selectable Zin 20/10 kΩ
5	RFRPi	I 3AI/F	RF ripple signal input pin	I	
6	RFEQo	O 3AI/F	RF equalizer circuit output pin.	O	Connect to RFRPi by 0.1uF, to RFi by 4700pF.
7	DCOFC	O 3AI/F	RFEQo offset compensation LPF output	O	Connect to Vro by more than 0.015uF
8	AGCi	I 3AI/F	RF signal AGC amplifier input pin	I	
9	RFo	O 3AI/F	RF signal generation amplifier output pin	O	
10	RVSS3	-	Grounding pin for 3.3 RF amplifier core and PLL circuit	-	
11	FNI2	I 3AI/F	Main beam signal input pin. To be connected to PIN diode C.	I	
12	FNI1	I 3AI/F	Main beam signal input pin. To be connected to PIN diode A.	I	
13	FPI2	I 3AI/F	Main beam signal input pin. To be connected to PIN diode D.	I	
14	FPI1	I 3AI/F	Main beam signal input pin. To be connected to PIN diode B.	I	
15	TPi	I 3AI/F	Sub beam signal input pin. To be connected to PIN diode F.	I	
16	TNi	I 3AI/F	Sub beam signal input pin. To be connected to PIN diode E.	I	
17	VRo	O 3AI/F	1.65 V reference voltage output pin.	O	Connected to PVREF, And connect to GNG by 0.1uF+100uF.
18	AVSS3	-	Grounding pin for 3.3V CD analog circuits.	-	
19	MDi	I 3AI/F	Monitor photodiode amplifier input pin.	I	Reference Voltage=178mVtyp.
20	LDo	O 3AI/F	Laser diode amplifier output pin	O	

Pin No.	Symbol	I/O	Description	Default	Remarks
21	FSMONIT	O 3AI/F	Focus Error signal / Sub beam add signal output pin(monitor pin/GND)	O	
22	RFZi	I 3AI/F	RF ripple zero-cross signal Input pin	I	
23	RFRP	O 3AI/F	RF ripple signal output pin.	O	
24	TEi	O 3AI/F	Tracking error signal output pin.	O	Bulit-in serises R=500Ω. Connect to VRo by capacitor.
25	AVDD3	-	Power supply pin for 3.3 V CD analog circuits.	-	
26	FOo	O 3AI/F	Focus servo equalizer output pin.	O	Bulit-in serises R=3.3 kΩ
27	TRo	O 3AI/F	Tracking servo equalizer output pin.	O	Bulit-in output R=3.3 kΩ
28	VSS	-	Grounding pin for 1.5V Decoder-DSP CD circuit	-	
29	FMo	O 3AI/F	Feed servo equalizer output pin.	O	Bulit-in output R=3.3 kΩ
30	FMoS	O 3AI/F	Feed servo equalizer output pin. （Stepper motor application）	O	Bulit-in output R=3.3 kΩ
31	DMo	O 3AI/F	Disc servo equalizer output pin	O	Bulit-in output R=3.3 kΩ
32	VDD1-3	I/O 3I/F	Power supply pin for 1.5V Decoder-DSP /CD circuit	-	
33	Pio8 / TxD/Dout	I/O 3I/F	Port 8（General Input/Output Port ） / HS UART (Out) / Dout(SPDIF)	I	CMOS Port Schmitt input
34	Pio9 / RxD/Aout	I/O 3I/F	Port 9（General Input/Output Port ） / HS UART (In) /Aout)	I	CMOS Port Schmitt input
35	Pio10 / RTS/BCKo	I/O 3I/F	Port 10（General Input/Output Port ） / HS UART (Out) / BCKo	I	CMOS Port Schmitt input
36	Pio11 / CTS/LRCKo	I/O 3I/F	Port 11（General Input/Output Port ） / HS UART (In) / LRCKo	I	CMOS Port Schmitt input
37	Pio12/ CDMON0/ AiN2	I/O 3I/F	Port 12（General Input/Output Port ） / Monitor 0 / Audio data input 2	I	CMOS Port Schmitt input
38	Pio13/ CDMON1/ BCKi2	I/O 3I/F	Port 13（General Input/Output Port ） / Monitor1 / Bitclock input 2	I	CMOS Port Schmitt input
39	Pio14/ CDMON2/ LRCKi2	I/O 3I/F	Port 14（General Input/Output Port ） / Monitor 2 / LR Clock input 2	I	CMOS Port Schmitt input
40	CDMON3	O 3I/F	Monitor3 output （SBSY)	O	CMOS Port

Pin No.	Symbol	I/O	Description	Default	Remarks
41	DVSS3R	-	Grounding pin for 3.3V Muiti-Bit DAC circuit	-	
42	Ro	O 3AI/F	R channel audio output pin of Audio DAC.	O	
43	DVDD3R	-	Power supply pin for 3.3V Audio DAC circuit.	-	
44	DVDD3L	-	Power supply pin for 3.3V Audio DAC circuit.	-	
45	Lo	O 3AI/F	L channel audio output pin of Audio DAC	O	
46	DVSS3L	-	Grounding pin for 3.3V Muiti-Bit DAC Circuit	-	
47	XVSS3	-	Grounding pin for 3.3V clock oscillator circuit	-	
48	Xi	I 3AI/F	System clock Input pin	I	Xtal oscillation circuit. Connect feedback resistor 1 MΩ between Xo and Xi
49	Xo	O 3AI/F	System clock Output pin	O	
50	XVDD3	-	Power Supply pin for 3.3V clock oscillator circuit	-	
51	VDD1-2	-	Power Supply pin for 1.5V Digital circuit	-	
52	VSS	-	Grounding pin for 1.5V digital circuit	-	
53	Pio0	I/O 3I/F	Port 0（General Input/Output Port ）	I	CMOS Port Schmitt input
54	Pio1	I/O 3I/F	Port 1（General Input/Output Port ）	I	CMOS Port Schmitt input
55	Pio2	I/O 3I/F	Port 2（General Input/Output Port ）	I	CMOS Port Schmitt input
56	Pio3	I/O 3I/F	Port 3（General Input/Output Port ）	I	CMOS Port Schmitt input
57	Pio4 / AiN 1	I/O 3I/F	Port 4（General Input/Output Port ） / Audio data Input 1	I	CMOS Port Schmitt input
58	Pio5 / BCKi1	I/O 3I/F	Port 5（General Input/Output Port ） / Bit Clock Input 1	I	CMOS Port Schmitt input
59	Pio6 / LRCKi1	I/O 3I/F	Port 6（General Input/Output Port） / LR Clock input 1	I	CMOS Port Schmitt input
60	Pio7	I/O 3I/F	Port 7（General Input/Output Port ）	I	CMOS Port Schmitt input

Pin No.	Symbol	I/O	Description	Default	Remarks
61	VDD3	-	Power Supply pin for 3.3V Digital circuit	-	Connect to GND by 0.1uF
62	BUS0	I/O 3I/F	Microprocessor I/F data input/output pin 0	I	CMOS Port Schmitt input
63	BUS1	I/O 3I/F	Microprocessor I/F data input/output pin 1	I	CMOS Port Schmitt input
64	BUS2	I/O 3I/F	Microprocessor I/F data input/output pin 2	I	CMOS Port Schmitt input
65	BUS3	I/O 3I/F	Microprocessor I/F data input/output pin 3	I	CMOS Port Schmitt input
66	BUCK /	I 3I/F	Microprocessor I/F BUS clock Input pin	I	Schmitt input
67	/CCE	I 3I/F	Microprocessor I/F chip enable input pin	I	Schmitt input
68	Test1	I 3I/F	Test pin(“H” input)	I	Pull up
69	/RST	I 3I/F	Reset Input pin	I	Schmitt input
70	Test	I 3I/F	Test pin （”L” input ）	I	
71	VDD1-1	-	Power Supply pin for 1.5V Digital circuit	-	
72	VSS	-	Grounding pin for 1.5V Digital circuit	-	
73	/SRAMSTB	I 3I/F	1Mbit SRAM stand by pin（/SRAMSTB="L"）	I	
74	VDDM1	-	Power Supply for 1.5V 1Mbit SRAM circuit	-	
75	PDo	O 3AI/F	EFM and PLCK Phase difference signal output pin.	O	4-state output (RVDD3, RVSS3,PVREF, Hiz)
76	TMAX	O 3AI/F	TMAX detection result output pin	O	3-state output (RVDD3, RVSS3, Hiz)
77	LPFN	I 3AI/F	PLL circuit LPF amplifier inversion input pin	I	
78	LPFo	O 3AI/F	PLL circuit LPF amplifier Output pin	O	
79	PVREF	-	PLL circuit 1.65 V reference voltage pin.	-	Connected to VRO. Connect to GND by 0.1uF and 100uF.
80	VCOF	O 3AI/F	VCO filter pin	O	Connect to GND by 0.01uF

*: 3A I/F : 3 V analog circuit input/output pin.
1.5 I/F : 1.5Vdigital input/output pin.
3 I/F : 3 V digital input/output pin.

Note1: The servo output pins (FOO, TRO, FMO, and DMO) become undefined or GND level under the following conditions:

- /RST pin = Low
- Crystal oscillation stopped according to the instructions by the Stop crystal oscillation command
- Power supply for CD is OFF.
- SRAMSTB pin = Low

To prevent the undefined pin states from affecting the servo circuitry or any other mechanical blocks in the system, appropriate measures should be taken, such as using a driver IC supporting a standby feature to place the system in standby mode while either of the above conditions is satisfied.

Note 2:

This IC does not have a power-on reset circuit.

Keep the /RST pin low until crystal oscillation becomes sufficiently stable with the voltage on each power supply pin risen to a level within the rated range. Once crystal oscillation is stable, keep /RST low for another 10 or more crystal oscillation cycles before driving /RST high. To prevent the undefined pin states from affecting the servo circuitry or any other mechanical blocks in the system, appropriate measures should be taken, such as using a driver IC supporting a standby feature to place the system in standby mode before /RST is driven high.

Note 3:

Attach bypass capacitors of 0.1uF and 10uF between VDD pins and VSS pins to reduce noise from power supply lines. Place the bypass capacitors as close to the device pins as possible.

1.2 Pin Assinment Table

1) Audio DSP

Pin No	Symbol	Audio DSP						CD	Note
		IO	AUDIO -OUT	AUDIO -IN	MCKo	IRQ	ZDET		
53	Pio0	Pio0	–	–	–	–	–	–	
54	Pio1	Pio1	–	ST_REQ	–	–	–	–	
55	Pio2	Pio2	–	GATE	–	–	–	–	
56	Pio3	Pio3	DoUT	–	–	–	–	–	
57	Pio4	Pio4	–	AiN	–	–	–	–	
58	Pio5	Pio5	–	BCKi	–	–	–	–	
59	Pio6	Pio6	–	LRCKi	–	–	–	–	
60	Pio7	Pio7	–	–	MCKo	IRQ	ZDET	–	
33	DoUT	Pio8	DoUT	–	–	–	–	–	
34	AoUT	Pio9	AoUT	–	–	–	–	–	
35	BCKo	Pio10	BCKo	–	–	–	–	–	
36	LRCKo	Pio11	LRCKo	–	–	–	–	–	
37	CDMON0	Pio12	AoUT	AiN2	–	–	(ZDET)	See 2)	Priority on CDMON
38	CDMON1	Pio13	BCKo	BCKi2	–	–	(ZDET)		
39	CDMON2	Pio14	LRCKo	LRCKi2	–	–	(ZDET)		
40	CDMON3	–	–	–	–	–	(ZDET)		

() Set up by PINMN command

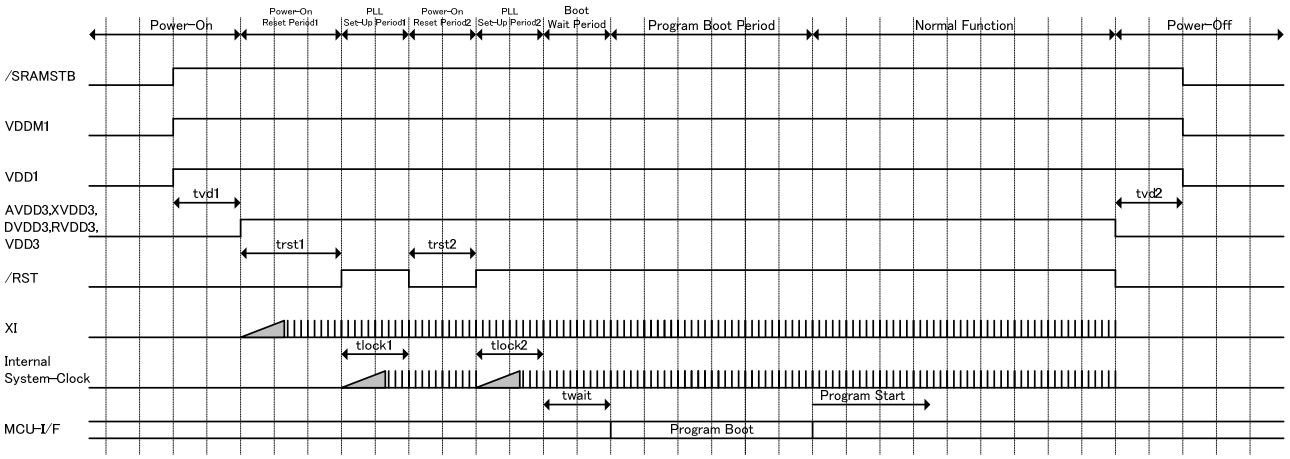
2) CD

Pin No	Symbol	CD				Audio DSP	Note
		CDMON CMD:PINMN	FGIN CMD:BRKFG	CD-G CMD:CLCKIEN	CD TEXT CMD:TEXTO		
37	CDMON0	CDMON0	FGIN	CLCKi	–	See 1)	Priority on CDMON
38	CDMON1	CDMON1	–	(DATA)	TXSRCKi		
39	CDMON2	CDMON2	–	(SFSY)	TEXTD		
40	CDMON3	CDMON3	–	(SBSY)	SBSY		

() Set up by PINMN command

2. Initialization method

Figure 2-1 shows the power-on and initialization sequences of the TC94B14MFG.



(Note) /SRMSTB,VDDM1 and VDD1 should be supplied at the same time within 100ms.

Characteristics	Symbol	Min	Typ.	Max
VDD3 rise time 1	tvd1	0 ms	—	100ms
VDD1 fall time 2	tvd2	0 ms	—	100ms
Power-on reset period 1	Trst1	5 ms	—	—
PLL setup period 1	tlock1	5 ms	—	—
Power-on reset period 2	Trst2	1 μs	—	—
PLL setup period 2	Tlock2	5 ms	—	—
Program boot waite period	twait	0 ms	—	—

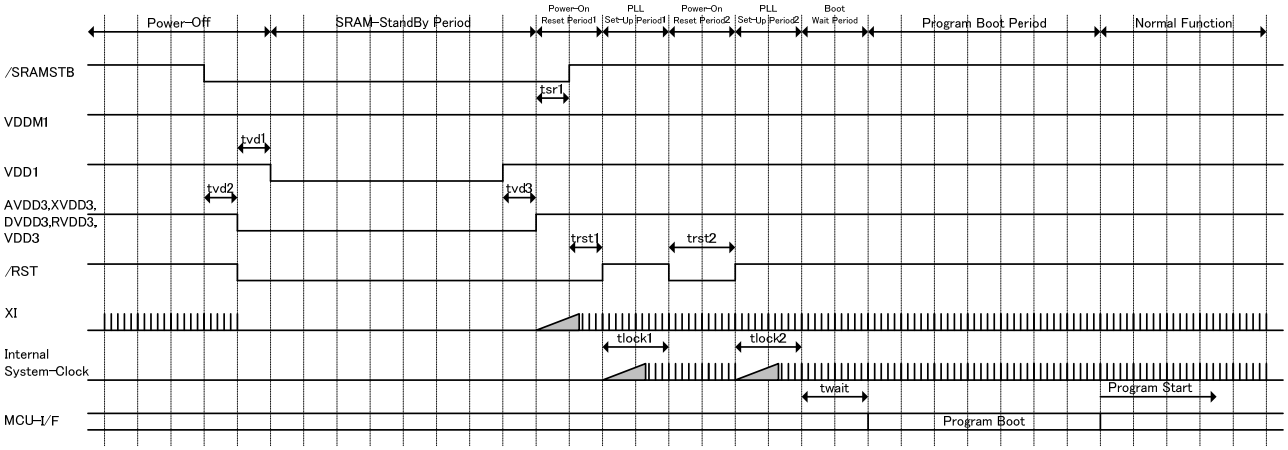
Figure 2-1 Power-on and initialization sequences

3. Standby Functions

The TC94B14MFG supports SRAM standby modes. When portable or in-vehicle units are on standby, using this mode can reduce waste in battery power consumption.

3-1. Standby mode

After shutting down all supply voltages except for VDDM1 (pin 74), making the /SRAMSTB pin (pin 73) low makes it possible to put the built-in 1 Mbit SRAM alone on standby. The data in the 1 Mbit SRAM is preserved, so the SRAM standby mode is useful to implement a resume function to be used after the standby mode is exited. Figure 3-1 shows the sequence of the SRAM standby mode**.**



Characteristics	Symbol	Min	Typ.	Max
VDD fall time 1	tvd1	0 ms	—	100ms
VDD fall time 2	tvd2	1 μs	—	—
VDD rise time 1	tvd3	0 ms	—	100ms
HW reset period 1	trst 1	5 ms	—	—
PLL setup period 1	tlock1	5 ms	—	—
HW reset period 2	trst 2	1 μs	—	—
PLL setup period 2	tlock 2	5 ms	—	—
Boot wait period	twait	0 ms	—	—
SRAM standby off setup time	tsr1	1 μs	—	—

Figure 3-1 Standby mode

note: All input terminals other than SRMSTB terminal are given as 'opening' or 'L' fixation at the time of SRAM standby mode.

4. Absolute Maximum rating

(Unless otherwise specified, Reference=Ground, Ta=25 °C)

Characteristics	Symbol	Rating	Unit	Characteristics
Supply voltage	VDD3	-0.3~3.8	V	--
	VDD1	-0.3~2.0		--
Input voltage	VIN3	-0.3~VDD3 + 0.3	V	--
	VIN1	-0.3~+3.9		--
Power Dissipation	P_D	2674	mW	--
Operating temperature	Topr	-20~85	°C	--
Storage temperature	Tstg	-55 ~ 150	°C	--

5. Electrical characteristics

5-1 RF core section

(Unless otherwise specified, VDD3 =RVDD3 = AVDD3 = XVDD3 = DVDD3L = DVDD3R = 3.3 V, VDD1-2 = VDDM1 = 1.5V , Ta = 25°C)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Power supply voltage									
	Guaranteed-operation supply voltage	V_{DD3}	—	—		3.0	3.3	3.6	V
Reference voltage									
	Reference voltage	VRo	—	—		—	1.65	—	V
	Output drain current	I_{OH}	—	$\Delta V = -0.1$ V		3	—	—	mA
	Output sink current	I_{OL}		$\Delta V = +0.1$ V		3	—	—	
APC section (MDi → LDo)									
	Voltage gain 1	G_{VAPC1}	—	f = 1 kHz, normal-polarity LDO(APCG=L)		—	200	—	V/V
	Voltage gain 2	G_{VAPC2}	—	f = 1 kHz, normal-polarity LDO(APCG=H)		—	100	—	V/V
	Operation reference voltage 1	V_{MDI1}	—	$V_{LDO} = V_{DD} - 1.3$ V, normal-polarity LDO(APCG=L)		160	178	196	mV
	Operation reference voltage 1	V_{MDI1}	—	$V_{LDO} = V_{DD} - 1.3$ V, normal-polarity LDO(APCG=H)		150	178	206	mV
	LD-off voltage 1	V_{LDOP1}	—	VDD reference,CMD: LD-OFF, PNP		—	−0.2	—	V
	Input bias current	I_{APC}	—	$V_{MDI1/2}$ = 178 mV		−1	—	1	μA
RF section (FPi1/FPi2 (FNi1/FNi2) → RFo)									
	Voltage gain & variable range 1 (CD-DA mode)	G_{VA11RF}	—	f = 100 kHz, CMD: GVSW = 1	RFOGAINi = 0000	—	−4	—	dB
		G_{VA12RF}			RFOGAINi = 1111	—	14	—	
	Voltage gain & variable range 2 (CD-RW mode)	G_{VA21RF}		f = 100 kHz, CMD: GVSW = 0	RFOGAINi = 0000	—	8	—	
		G_{VA22RF}			RFOGAINi = 1111	—	26	—	
	Frequency characteristic 1 (CD-DA mode) (Note 1)	f_{C1RF}	—	−3dB point, CMD: GVSW = 1, RFOGAINi = 1000		—	16	—	MHz
	Frequency characteristic 2 (CD-RW mode) (Note 1)	f_{C2RF}		−3 dB point, CMD: GVSW = 0, RFOGAINi = 1000		—	6	—	
	Output slew rate	SR_{RF}	—	C_{RFO} = 20 pF		10	20	—	V/μs
	Output upper-limit voltage	V_{OHRF}	—	GND reference		2.9	3.1	—	V
	Output lower-limit voltage	V_{OLRF}		GND reference		—	0.3	0.5	
	Permissible load resistance	R_{LMRF}	—	—		5	10	—	kΩ

Note 1:Design guarantee.

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
AGC+RFEQ section (AGCi → RFEQo)									
	Voltage gain 1(Note 2)	G_{V1AGC}	—	f = 100 kHz	RFGC = 80h	—	—	−0.7	V/V
	Voltage gain 2(Note 2)	G_{V2AGC}			RFGC = B0h	—	1.0	—	
	Voltage gain 3(Note 2)	G_{V3AGC}			RFGC = 7Fh	2.2	—	—	
	Peak frequency 1 (×1 speed mode)	f_{C1EQ}	—	CMD: D7C01E (Boost Max), RFGC = 00h		0.9	—	1.8	MHz
	Peak frequency 2 (×2 speed mode)	f_{C2EQ}		CMD: D7C11E (Boost Max), RFGC = 00h		1.7	—	3.4	
	Group delay difference 11(×1 speed mode) (Note 3)	GD_{1EQ}	—	CMD: D7001E, RFGC = 00h, f = 100-700 kHz/100kHz step		—	—	100	ns
	Peak gain difference 11(×1 speed mode) (Note 4)	fV_{1EQ}	—	f = 100 kHz (reference), RFGC = B0h, CMD: D7C01E (Boost Max)		—	5	—	dB
	Peak gain difference 21(×2 speed mode) (Note 4)	fV_{2EQ}		f = 100 kHz (reference), RFGC = 00h, CMD: D7C11E (Boost Max)		—	5	—	
	Output slew rate	SR_{AGC}	—	C_{RFEQO} = 20 pF		10	20	—	V/us
	Output upper-limit voltage	V_{OHAGC}	—	GND reference		2.9	3.1	—	V
	Output lower-limit voltage	V_{OLAGC}		GND reference		—	0.3	0.5	
	Permissible load resistance	R_{LMAGC}	—	—		5	10	—	kΩ

Note 2: These values were measured in the AGC-AMP section.

Note 3: Group delay difference of Peak-Bottom in 100 to 700KHz at x1 speed mode.

Note 4: These values were measured in the RFEQ section. Design guarantee.

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
FE section (FPi1/FPi2 (FNi1/FNi2) → FEi)									
	Voltage gain & variable range 1 (CD-DA mode)	G_{VA11FE}	—	f = 1kHz, CMD: GVSW = 1	FEOGAINi = 0000	—	−0.5	—	dB
		G_{VA12FE}			FEOGAINi = 1111	—	23.5	—	
	Voltage gain & variable range 2 (CD-RW mode)	G_{VA21FE}		f =1kHz, CMD: GVSW = 0	FEOGAINi = 0000	—	11.5	—	
		G_{VA22FE}			FEOGAINi = 1111	—	34.5	—	
	Gain balance 1 (CD-DA mode)	GB_{1FE}	—	ΔG_{VA1*FE}		−1	0	+1	dB
	Gain balance 2 (CD-RW mode)	GB_{2FE}		ΔG_{VA2*FE}		−1	0	+1	
	Frequency characteristic 1 (CD-DA mode)	f_{C1FE}	—	−3dB point, CMD: FEBW = 0, CMD: GVSW = 1		—	29	—	kHz
	Frequency characteristic 2 (CD-RW mode)	f_{C2FE}		−3dB point, CMD: FEBW = 0, CMD: GVSW=0		—	29	—	
	Output offset voltage 1 (CD-DA mode) (Note 5)	V_{OF1FE}	—	VRO reference, FPI1/FPI2/FNI1/FNI2 open FEBC = 00h, CMD: GVSW = 1		−50	—	+50	mV
	Output offset voltage 2 (CD-RW mode) (Note 5)	V_{OF2FE}		VRO reference, FPI1/FPI2/FNI1/FNI2 open FEBC = 00h, CMD: GVSW = 0		−50	—	+50	
	Output upper-limit voltage	V_{OHFE}	—	GND reference		2.9	3.1	—	V
	Output lower-limit voltage	V_{OLFE}		GND reference		—	0.3	0.5	
	Permissible load resistance	R_{LMFE}	—	—		10	15	—	kΩ

Note 5: These values are those for which offset correction is completed.

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
TE section (TPi (TNi) → TEi)									
Voltage gain & variable range 1 (CD-DA mode)		G_{VA11TE}	—	f = 1 kHz, TEBC = 00h, CMD: GVSW = 1	TEOGAINi = 0000	—	7.5	—	dB
		G_{VA12TE}			TEOGAINi = 1111	—	32	—	
Voltage gain & variable range 2 (CD-RW mode)		G_{VA21TE}		f = 1 kHz, TEBC = 00h, CMD: GVSW = 0	TEOGAINi = 0000	—	19.5	—	
		G_{VA22TE}			TEOGAINi = 1111	—	44	--	
Gain balance adjustment width	H (DA)	ΔR_{T1TE}	—	TEBC = 7Fh, GVSW=1		+50	+60		%
	L (DA)	ΔR_{T2TE}		TEBC = 80h, GVSW=1		—	−60	−50	
Gain balance 1 (CD-DA mode)		GB_{1TE}	—	ΔG_{VA1*TE}		−1	0	+1	dB
Gain balance 2 (CD-RW mode)		GB_{2TE}		ΔG_{VA2*TE}		−1	0	+1	
Frequency characteristic 1 (CD-DA mode)		f_{C1TE}	—	−3dB point, CMD: GVSW = 1		—	33	—	kHz
Frequency characteristic 2 (CD-RW mode)		f_{C2TE}		−3dB point, CMD: GVSW = 0		—	33	—	
Output offset voltage 1 (CD-DA mode) (Note 6)		V_{OF1TE}	—	VRO reference, TPI/TNI open, TEBC = 00h CMD: GVSW = 1		−50	—	+50	mV
Output offset voltage 2 (CD-RW mode) (Note 6)		V_{OF2TE}		VRO reference, TPI/TNI open, TEBC = 00h CMD: GVSW = 0		−50	—	+50	
Output upper-limit voltage		V_{OHTE}	—	GND reference		2.9	3.1	—	V
Output lower-limit voltage		V_{OLTE}		GND reference		—	0.3	0.5	
Permissible load resistance		R_{LMTE}	—	—		10	15	—	kΩ

Note 6: These values are those for which offset correction is completed.

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
RFRP section (RFRPi → RFRP)									
	Voltage gain 1	G_{V1RP}	—	RFRPI input amp gain	RFRPGi = 00	—	2.7	—	dB
	Voltage gain 2	G_{V2RP}			RFRPGi = 01	—	3.8	—	
	Voltage gain 3	G_{V3RP}			RFRPGi = 10	—	4.8	—	
	Voltage gain 4	G_{V4RP}			RFRPGi = 11	—	5.7	—	
	Detection frequency 1 (Note 7)	f_{1RP}	—	−3dB point with reference to low-frequency side on the assumption that RFRPI = 1.2 Vpp for V_{OP1RP} and output amplitude = 0dB for a 700 kHz sine wave input.		—	50	—	kHz
	Detection constant 1	T_{1RP}	—	RFRPI = 1.2 Vpp for V_{OP1RP} and slew rate (Cin > 1 μF) for a 5 kHz rectangular wave input.		—	90	—	V/ms
	Operating reference voltage 1	V_{OP1RP}	—	VRO reference, no input		−1.15	—	−0.75	V
	Operating reference voltage 2	V_{OP2RP}		VRO reference, RFRPI = 1.2Vpp/700 kHz		0.3	—	1.0	
	Output upper-limit voltage	V_{OHRP}	—	GND reference		2.9	3.1	—	V
	Permissible load resistance	R_{LMRP}	—	—		10	15	—	kΩ
RFDC section (FPi1/FPi2 (FNi1/FNi2) → RFDC)									
	Detection frequency 1 (Note 7)	f_{1DC}	—	−3dB point with reference to low-frequency side on the assumption that RFDCI = 1.2 Vpp for V_{OP1DC} and output amplitude = 0dB for a 700 kHz sine wave input.		—	20	—	kHz
	Detection constant 1	T_{1DC}	—	RFDCI = 1.2 Vpp for V_{OP1DC} and slew rate (Cin > 1 μF) for a 5 kHz rectangular wave input.		—	14	—	V/ms
	Operating reference voltage 1	V_{OP1DC}	—	VRO reference, FPI1/FPI2/FNI1/FNI2 open, CMD: RFOOLDi = 00		−1.15	—	−0.75	V
	Operating reference voltage 2	V_{OP2DC}		VRO reference, RFDCI = 1.2Vpp/350 kHz, CMD: RFOOLDi = 00		0.2	—	0.55	
	Output upper-limit voltage	V_{OHDC}	—	GND reference		2.7	3.0	—	V
	Output lower-limit voltage	V_{OLDC}		GND reference		—	0.5	0.8	
	Permissible load resistance	R_{LMDC}	—	—		20	25	—	kΩ

Note 7: The detection frequency values are for only reference purposes.

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
SBAD section (TPi (TNi) → SBAD)									
	Voltage gain 1 (CD-DA mode)	G_{V1SB}	—	f = 1kHz, TEBC = 00h CMD: GVSW = 1	SBADGAINi = 0000	—	−2.5	—	dB
					SBADGAINi = 1111	—	22.0	—	
	Voltage gain 2 (CD-RW mode)	G_{V1SB}		f = 1kHz, TEBC = 00h CMD: GVSW = 0	SBADGAINi = 0000	—	9.5	—	
					SBADGAINi = 1111	—	34.0	—	
	Frequency characteristic	f_{CSB}	—	−3dB point		—	44	—	kHz
	Operating reference voltage 1 (CD-DA mode)	V_{OP1SB}	—	VRO reference No input SBADINV = 0		−1.1	−0.8	−0.5	V
	Operating reference voltage 2 (CD-RW mode)	V_{OP2SB}				−1.1	−0.8	−0.5	
	Output upper-limit voltage	R_{OHSB}	—	GND reference		2.9	3.1	—	V
	Output lower-limit voltage	R_{OLSB}		GND reference		—	0.3	0.5	
	Permissible load resistance	R_{LMSB}	—	—		10	15	—	kΩ

5.2 DSP core section

5-2-1 DC characteristics

(Unless otherwise specified, VDD3 =AVDD3 = DVDD3L/R = XVDD3 = RVDD3 = 3.3 V, VDD1 = VDDM1 = 1.5V , Ta = 25°C)

Characteristics		Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Oprating Power Supply Voltage		VDD3	--	--		3.0	3.3	3.6	V
		RVDD3							
		AVDD3							
		DVDD3L/R							
		XVDD3							
		VDD1	--	--		1.4	1.5	1.6	V
		VDDM1							
Oprating frequency range		fopr	--	Ta = -20～70℃, VDD1/VDDM1=1.4V		--	--	87.5	MHz
Operating power supply current	×1 speed	IDD3		XI = 16.9344 MHz fopr = 85 MHz (Note 8) @ CDMP3 opration(MP3 Stream fs=48kHz/320 kbps) Ta=-20℃～70℃ (Includs current for CD servo)		--	80	100	mA
		IDD1				--	30	36	
		IDDM				--	0.6	1	
	×2 speed	IDD3				--	80	100	
		IDD1				--	32	38	
		IDDM				--	0.6	1	
Input Voltage	"H" level	VIH3	--	CMOS input pins (3 V circuits) excluding analog input pins		VDD3 x 0.7	--	--	V
	"L" level	VIL3				--	--	VDD3 x 0.3	
	"H" level	VIH1	--	/SRMSTB pin		VDDM1 x 0.8	--	--	
	"L" level	VIL1				--	--	VDDM1 x 0.2	
Input current	"H" level	IIH3	--	VIH3 = VDD3		--	--	2.0	μA
	"L" level	IIL3		VIL3 = VSS		−1.0	--	--	
Output current	"H" level	IOH3	--	VOH3 = 2.9 V	Pins listed at (#1) in the following table.	--	--	−4.0	mA
	"L" level	IOL3		VOL3 = 0.4 V		4.0	--	--	
	"H" level	IOH3		VOH3 = 2.9 V	Pins listed at (#2) in the following table.	--	--	-2.0	
	"L" level	IOL3		VOL3 = 0.4 V		2.0	--	--	

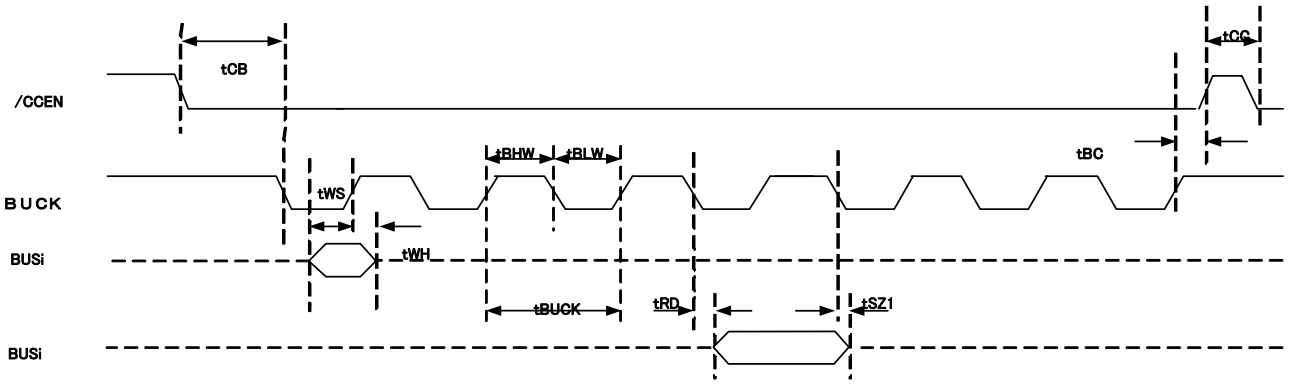
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output resistance integrated at pin	RO1	--	Pins listed at (#3) in the following table.	--	10	--	kΩ
	RO2		Pins listed at (#4 and #5) in the following table.	--	3.3	--	
Standby current	I_{STBM}		V_{DD1},V_{DD3} OFF,V_{DDM} = 1.6 V, /SRMSTB (73pin) = "L" Ta=-20℃～70℃	—	—	20	μA

	Terminal
#1	BUS3, BUS2, BUS1, BUS0, CDMON 0-3, Pio6,Pio7
#2	Pio 0-5, Pio 8-11
#3	PDo
#4	FMo, DMo,FMoS
#5	Foo, TRo

Note 8: Power supply current of operation is changed with a speed of operation or application. The value of table is reference value when operating CDMP3 standard application (of operation speed:85MHz, MP3 stream condition : fs=48kHz / 320kbps).

5.3 AC Characteristic

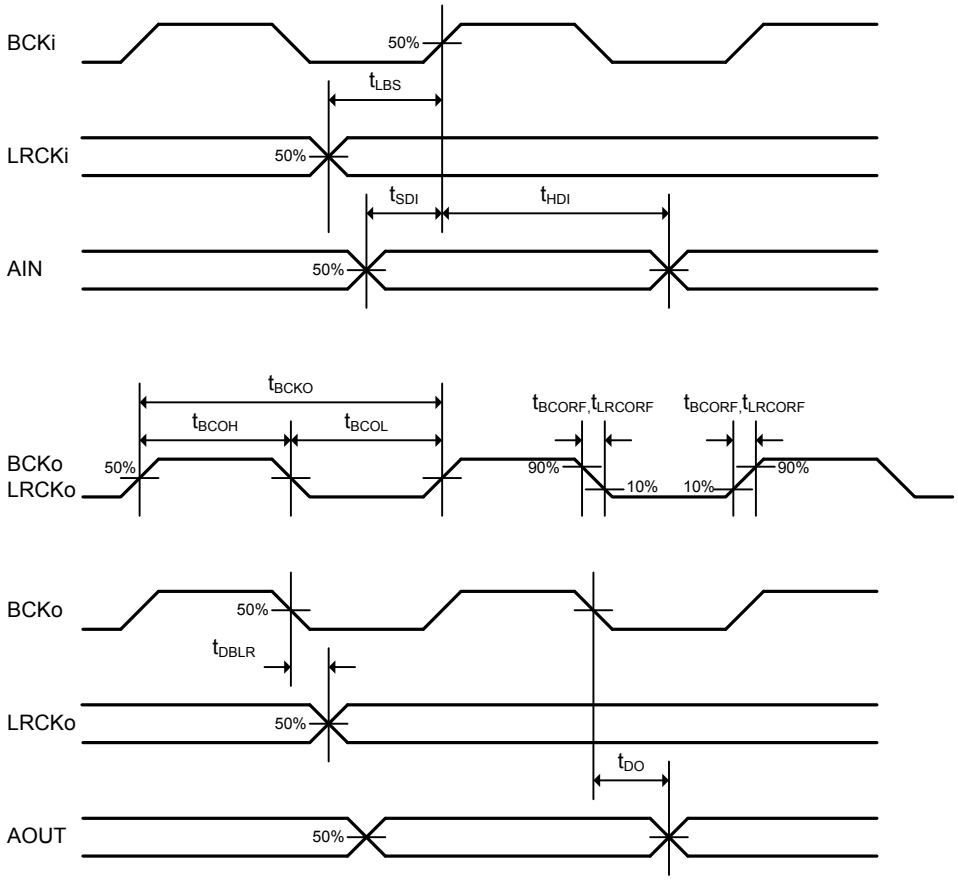
5-3-1 MCU I/F Pararell Mode



Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
/CCE = “H” pulse width	tCC	--		150	--	--	ns
Data disable time	tSZ1	--		0	--	--	
/CCE, BUCK delay time	tCB	--		150	--	--	
BUCK-to-/CEE delay time	tBC	--		150	--	--	
BUCK cycle time	tBUCK	--		800	--	--	
BUCK = “L” pulse width	tBLW	--		400	--	--	
BUCHK = “H” pulse width	tBHW	--		400	--	--	
Write data set-up time	tWS	--		150	--	--	
Write data hold time	tWH	--		150	--	--	
Read data access time	tRD	--		--	--	150	

5-3-3 Audio I/F(LRCKi/o,BCKi/o,AIN/OUT)

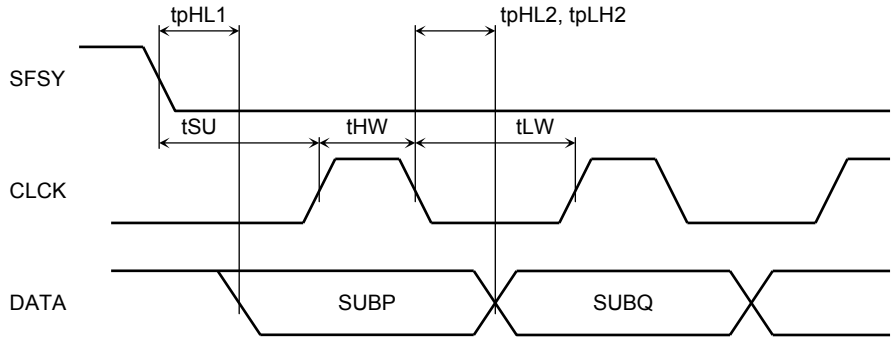
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
LRCKi Setup time	t_{LBS}	--	fs = 44.1 kHz, BCKi = 64 fs	20	--	--	ns
AIN Setup time	t_{SDI}	--	fs = 44.1 kHz, BCKi = 64 fs	20	--	--	
AIN Holdtime	t_{HDI}	--	fs = 44.1 kHz, BCKi = 64 fs	20	--	--	
BCKo Clock cycle	t_{BCKO}	--	C_L = 8 pF, fs = 44.1 kHz, BCKo = 64 fs	354	--	--	
BCKo Clock "H" Term	t_{BCOH}	--	C_L = 8 pF, fs = 44.1 kHz, BCKo = 64 fs	170	--	--	
BCKo Clock "L" Term width	t_{BCOL}	--	C_L = 8pF, fs = 44.1kHz, BCKo = 64fs	170	--	--	
BCKo standup / falling term 1	t_{BCORF1}	--	BCKo(35pin), C_L ・ 8pF	--	--	15	
BCKo standup / falling term 2	t_{BCORF2}	--	BCKo(38pin), C_L ・ 8pF	--	--	8	
LRCKo standup / falling term 1	$t_{LRCORF1}$	--	LRCKo(36pin), C_L=8pF	--	--	15	
LRCKo standup / falling term 2	$t_{LRCORF2}$	--	LRCKo(39pin), C_L=8pF	--	--	8	
AOUT Output delay time	t_{DO}	--	C_L = 8 pF, fs = 44.1 kHz, BCKo = 64 fs	-10	--	10	
LRCKo Output delay time	t_{DBLR}	--	C_L = 8 pF, fs = 44.1 kHz, BCKo = 64 fs	-10	--	10	



5-3-3 DATA, CLCK Input/Output timing

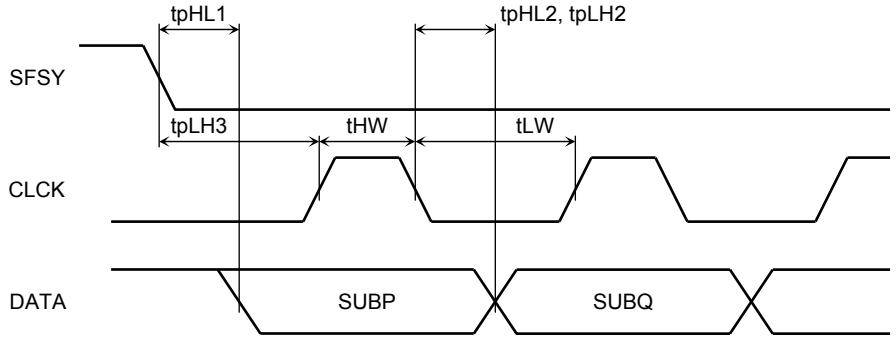
(1) CLCK input mode

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock pulse width	"H" level	tHW	--	CLCK Input mode	300	--	--	ns
	"L" level	tLW			300	--	--	
Input set-up time		tSU	--		400	--	--	
Transfer time (1)	"L" level	tpHL1	--		--	--	70	
Transfer time (2)	"H" level	tpLH2	--		--	--	220	
	"L" level	tpHL2			--	--	220	



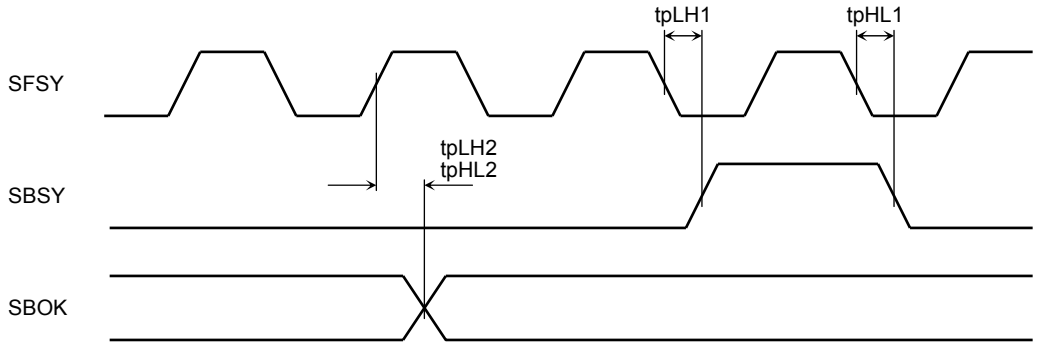
(2)CLCK output mode (only for tHW, tLW, and tpLH3, ×n speed × 1/n)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clock pulse width	"H" level	tHW	--	CLCK Output mode	--	--	950	ns
	"L" level	tLW			--	--	950	
Transfer time (1)	"L" level	tpHL1	--		--	--	70	
Transfer time (2)	"H" level	tpLH2	--		--	--	70	
	"L" level	tpHL2			--	--	70	
Transfer time (3)	"H" level	tpLH3	--		--	--	960	



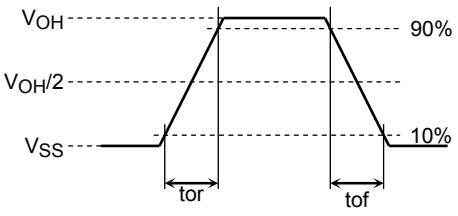
5-3-4 SBSY, SBOK Input/Output timing

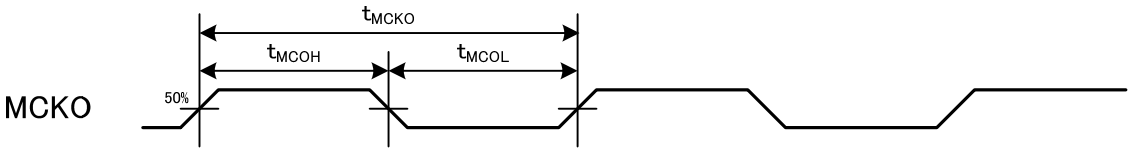
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Transfer time (1)	"H" level	tpLH1	--	SBSY	--	--	500	ns
	"L" level	tpHL1			--	--	500	
Transfer time (2)	"H" level	tpLH2	--	SBOK	--	--	500	
	"L" level	tpHL2			--	--	500	



5-3-5 Output pin timing

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Rising time (1)	tor1	--	Pio0-5, 8-11	--	--	15	ns
Falling time (1)	tof1	--	CL=8pF	--	--	15	
Rising time (2)	tor2	--	Pio6-7, 12-15	--	--	8	
Falling time (2)	tof2	--	CL =8pF	--	--	8	
MCKo Clock time	T_{BCO}	--	CL =8pF,fs=44.1kHz, MCKo=384fs(=Xi)	58	--	--	
MCKo Clock "H" time	T_{BCOH}	--		25	--	--	
MCKo Clock "H" time	T_{BCOL}	--		25	--	--	





5.4 Analog Circuit Characteristics

5-4-1 AD Converter

Characteristics		Test Circuit	Test Condition	Min	Typ.	Max	Unit
Resolution		--	--	--	10	--	bit
Sampling frequency	FE	--	--	--	176.4	--	kHz
	TE			--	176.4	--	
	SBAD(RFDC)			--	88.2	--	
	RFRP			--	176.4	--	
Conversation input range		--	AV_{SS} = 0 V AV_{DD3} = 3.3 V	0.15 × AV_{DD3}	--	0.85 × A_{VDD3}	V

5-4-2. DA Converter (Focus and Tracking Sections)

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Bit number	--	--	--	5	--	bit
Sampling frequency	--	--	--	5.6	--	MHz
Output signal range	--	AV_{SS} = 0 V, AV_{DD3} = 3.3 V	AV_{SS3}	--	AV_{DD3}	V

5-4-3. PLL Section Filter Amp

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input/output signal range	--	--	RV_{SS3}	--	RV_{DD3}	V
Frequency characteristic	--	−3dB point (Gain = 1)	--	1.7	--	MHz

5-4-4. VCO (PLL)

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Oscillation center frequency	--	LPFO = V_{REF}	--	69	--	MHz
Frequency variation range	--	--	--	±25	--	%

5-4-5. TEZI Signal Comparator

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input range	--	--	AV_{SS3}	--	AV_{DD3}	V
Hysteresis voltage	--	V_{REF} reference	--	±50	--	mV

5-4-6. RFZI Signal Comparator

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input range	--	--	AV_{SS3}	--	AV_{DD3}	V
Hysteresis voltage	--	V_{REF} reference	--	±50	--	mV

5-4-7. Data Slicer Circuit

(1) Comparator

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input amplitude	--	V_{REF} reference	0.6	1.2	2.0	V_{pp}

(2) R-2R DAC (DAC for digital slicer)

Characteristics	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output conversation range	--	SLCOG=0	3/4 V_{REF}	--	5/4 V_{REF}	V
Output conversation range	--	SLCOG=1	1/2 V_{REF}	--	3/2 V_{REF}	V
Output impedance	--	SLCOG=0	--	2.5	--	kΩ
Output impedance	--	SLCOG=1	--	5	--	kΩ

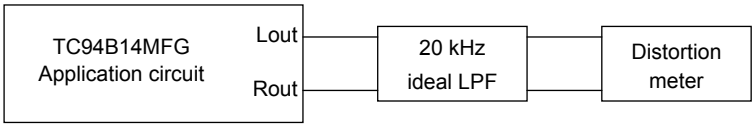
5-4-10 Audio DAC Characteristics

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Lo,Ro pin output impedance	Zo	-		—	2	—	kΩ
Noise distortion factor	THD + N (1)	1	1 kHz sine wave, full scale input.	—	−88	−80	dB
	THD + N (2)		10 kHz sine wave, full scale input.	—	−93	−78	
S/N ratio	S/N (1)	1	Internal zero detection on	93	101	—	dB
Dynamic range	DR	1	1 kHz sine wave, −60 dB input conversion	90	98	—	dB
Crosstalk	CT	1	1 kHz sine wave, full scale input.	—	−97	−90	dB
Analog output amplitude	DACout	1	1 kHz sine wave, full scale input.	780	820	860	mVrms

Stop band Attenuation = -60dB, In band ripple = below +/- 0.025dB

This characteristic is the characteristic at the time of 1x Playback mode.

Test circuit 1: The application circuit shown in the following example is used.

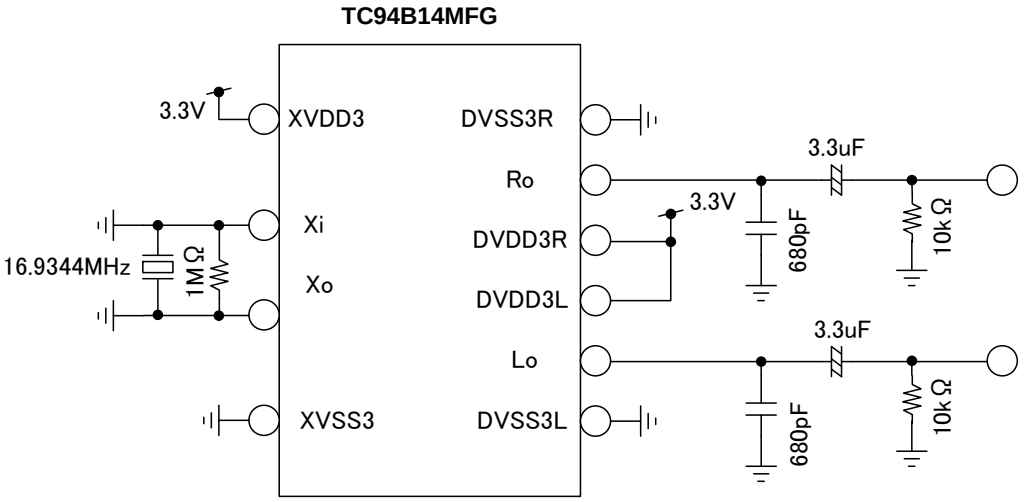


LPF: Filter incorporated in the SHIBASOKU distortion meter 725D.
Distortion meter: SHIBASOKU 725D or equivalent.

Characteristics	Distortion Filter Setting: A-weight
THD + N, CT	OFF
S/N, DR	ON

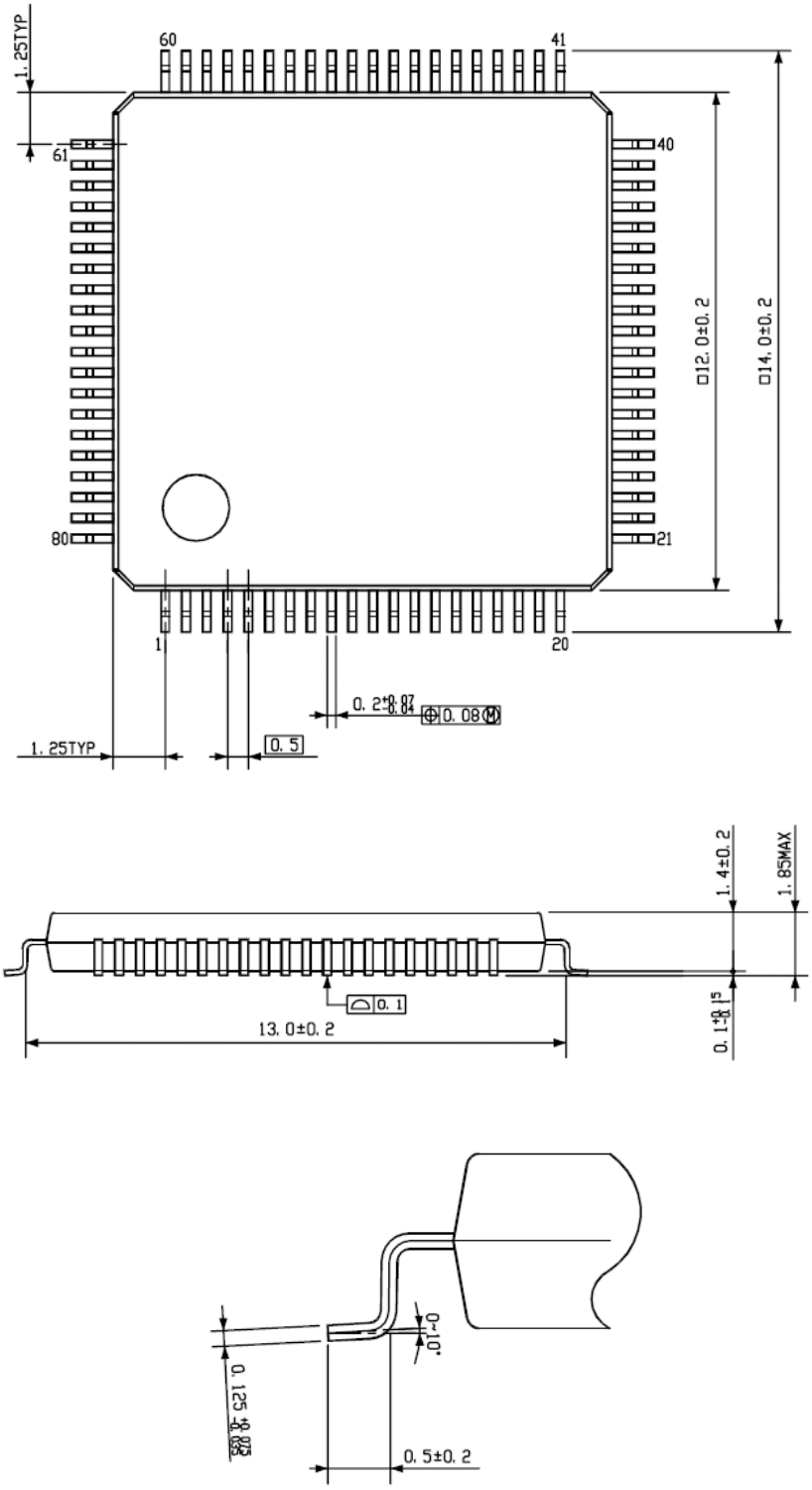
A-weight: IEC-A or equivalent

Application circuit example



Package

LQFP80-P-1212-0.50F



Weight : 0.6 g (Typical)

About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-37Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

RESTRICTIONS ON PRODUCT USE

- Toshiba Corporation, and its subsidiaries and affiliates (collectively “TOSHIBA”), reserve the right to make changes to the information in this document, and related hardware, software and systems (collectively “Product”) without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA’s written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product’s quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before creating and producing designs and using, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the “TOSHIBA Semiconductor Reliability Handbook” and (b) the instructions for the application that Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS’ PRODUCT DESIGN OR APPLICATIONS.**
- Product is intended for use in general electronics applications (e.g., computers, personal equipment, office equipment, measuring equipment, industrial robots and home electronics appliances) or for specific applications as expressly stated in this document. Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact (“Unintended Use”). Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for Unintended Use unless specifically permitted in this document.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. TOSHIBA assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.